

Assembly Guidelines for QFN and DFN Packages

1 Introduction

This application note provides guidelines for the handling and assembly of Freescale QFN and DFN packages during printed circuit board (PCB) assembly, and guidelines for PCB design and rework, and package performance information (such as Moisture Sensitivity Level rating, board level reliability, mechanical and thermal resistance data).

This application note seeks to address {describe the essential goal to be realized}.

2 Scope

Contains generic information for various Freescale QFN and DFN packages assembled internally (or at external subcontractors). Specific information about each device is not provided. To develop a specific solution, actual experience and development efforts are required to optimize the assembly process and application design per individual device requirements, industry standards (such as IPC and JEDEC), and prevalent practices in the assembly environment. For more details about the specific devices contained in this note, visit www.freescale.com or contact the appropriate product application team.

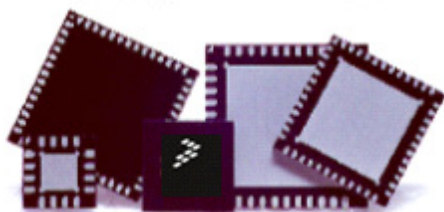
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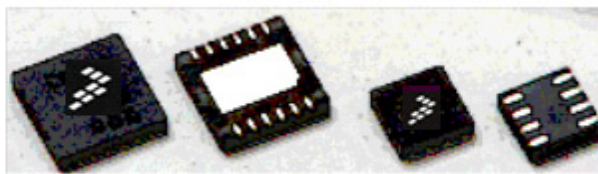
3 DFN and QFN Packages

3.1 Package Descriptions

The Dual Flat No-Lead (DFN) / Quad Flat No-Lead (QFN) packages are lead-less, near Chip Scale Packages (CSP) with a low profile, moderate thermal dissipation, and good electrical performance. The DFN / QFN is a surface mount plastic package with leads located at the bottom of the package, with the DFN having leads on two sides of the package versus on four sides for the QFN. A thermally enhanced DFN / QFN with an exposed die pad is available and is denoted as DFN-EP / QFN-EP. The suffix "EP" stands for exposed pad. EIAJ and JEDEC have their respective design guidelines and structure description for this package. Freescale adopted the DFN-EP / QFN-EP package design rules under JEDEC, document MO-229 and MO-220, respectively^[2, 3].



QFN/QFN-EP Packages









DFN/DFN-EP Packages

Figure 1. QFN/QFN-EP (Left) and DFN/DFN-EP (Right) Packages from Freescale

3.2 Package Dimensioning

Available packages range from 2.0 x 1.5 mm to 9.0 x 9.0 mm in size (Table 1). The dimensional tolerance and positioning accuracy affects subsequent processes as the package size shrinks and the lead count increases. In subsequent processes, the PCB layout and stencil designs are critical to ensure sufficient solder coverage between the package and the Printed Circuit Board (PCB). When designing the PCB layout, refer to the Freescale case outline drawing to obtain the package dimensions and tolerances. These benefits are illustrated in the figure below.

Table 1. Freescale DFN/QFN Package Dimensions

																
	Punch							Sawn		wetttable flank (WF)	Cavity QFN - Sensor	flip chip	chip-on-lead			
	DFN/QFN single row - sawn/punch							QFN WF		Cavity QFN	FCQFN	DFN/QFN-COL				
	Lead Pitch (mm)															
Body Size	1.27p	1.0p	0.95p	0.80p	0.65p	0.50p	0.40p	1.00p	0.50p	0.80p	0.65p	0.50p	0.50p	065p	0.40p	
2x1.5						6										
2x2						8							8		10	
2x3						8										
3x2												10				
3x3			6			12/16	20						10/16	12	20	
3x4						20										
4x4				8	16	20/24										
4x5																
5x5				16	24	26/32										
6x6		16				20/40		16		20						
7x7					32	48	56		48							
8x8						56										
9x9					44	64					32					
Thickness	V: 0.8 - 1.0mm thickness. Sensor only 1.45 - 2.08mm							1.98mm	0.9mm	1.98mm	2.33mm	0.60mm to 1.20mm				
Color Code Key:																
Black font - sawn only																
Blue font - both in punch and sawn																
Orange font - punch only																

Part interchangeability is a concern when primary and secondary suppliers both provide production parts. The optimized PCB layout for the primary supplier may have issues (manufacturing yield and/or solder joint life) with the secondary supplier, especially when two styles of the QFN packages are selected. (See [Table 3.3.2](#) and [Table 3.3.3](#).) When more than one package source is expected, the PCB layout should be designed for robustness. Also see [Table 4](#).

3.3 DFN/QFN Package Design

3.3.1 Cross Sections

- [Figure 2](#) shows a cross-section of a typical sawn DFN / QFN, a lead-frame-based package with wire-bonding technology.
- [Figure 3](#) shows a punch QFN.
- [Figure 4](#) shows a sawn DFN Chip-on-Lead.

The singulation method is discussed in the following section. The die is usually epoxy-attached to die pad (or flag) with an option for the die pad exposure (EP version) external to the package.

For Chip-on-Lead (CoL) packages, the die attach pad is removed and the die is placed on extended lead fingers (using a B-stage electrically insulating but thermally conductive adhesive). This allows a larger die to be assembled in the same package using conventional wire bonding.

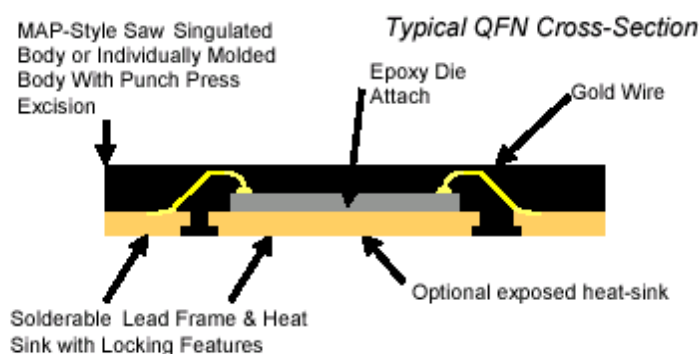


Figure 2. Sawn DFN/QFN (Cross-Section View)

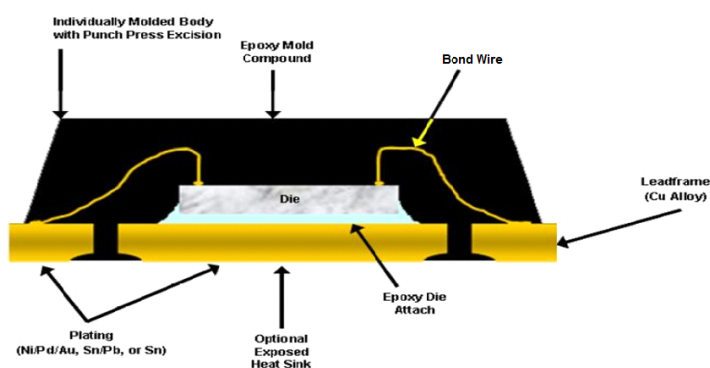


Figure 3. Punch QFN (Cross-Section View)

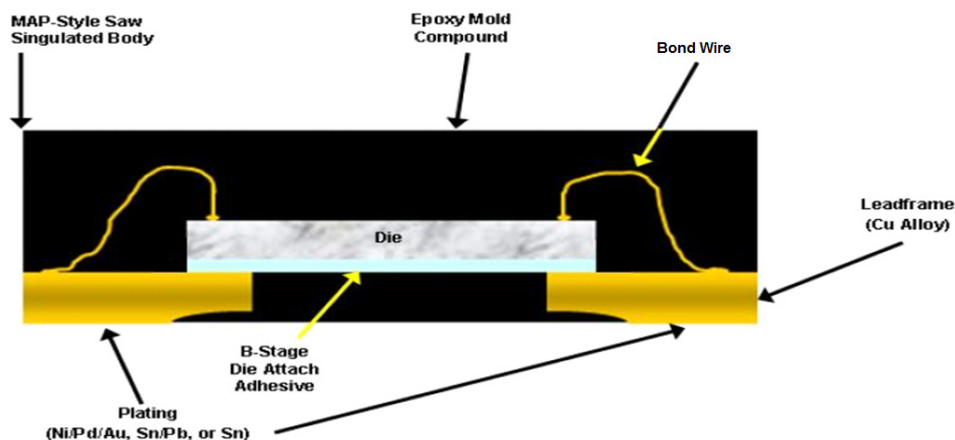


Figure 4. Sawn DFN - Chip-on-Lead (CoL, Cross-Section View)

3.3.2 Singulation Method: Saw and Punch

There are two singulation methods for DFN / QFN packages: punch and saw.

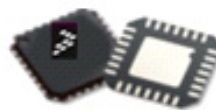
- Punch singulation is used on individually molded packages.
- Saw singulation is performed on Molded Array Packages, similar to wafer singulation.

The cross-sectional profiles for each are different and are shown in [Figure 2](#) to [Figure 4](#). In this section, both styles of QFN are discussed. In subsequent sections, guidelines or information related to a specific style of DFN / QFN is stated as such; otherwise, the material applies to both styles.

The punch singulated QFN is also a JEDEC-compliant design. The bottom lead portion of the package protrudes outwards compared to the top portion, leaving a ledge (see [Figure 5](#)). Punch singulation process is not used for DFN packages.



Sawn



Punch

Figure 5. Singulated QFN

3.3.3 Lead Terminal Types

For DFN / QFN packages, Freescale offers three different lead terminal types: "E", "S" and "D" (Dimple pad).

3.3.3.1 MAP DFN/QFN: "E" Style

E-type lead frames are half-etched from the top, where the lead posts are exposed all the way to the edge of the package (viewed from the bottom of the package, see left photo in [Figure 6](#)). "E" version follows JEDEC MO-220 (QFN) and MO-229 (DFN) design guidelines. The lead extends to the package perimeter, where the lead ends are fully exposed to the side of the package. A solder fillet is expected to form and should be visible on the PCB after the solder reflow process. However, a solder fillet is not guaranteed and depends upon the board and stencil design, solder paste flux composition/volume, and assembly process conditions. Follow the guidelines in section "[PCB Pad Design](#)", on page 8 to get optimal results. **E-type lead frames are considered standard Freescale design.**

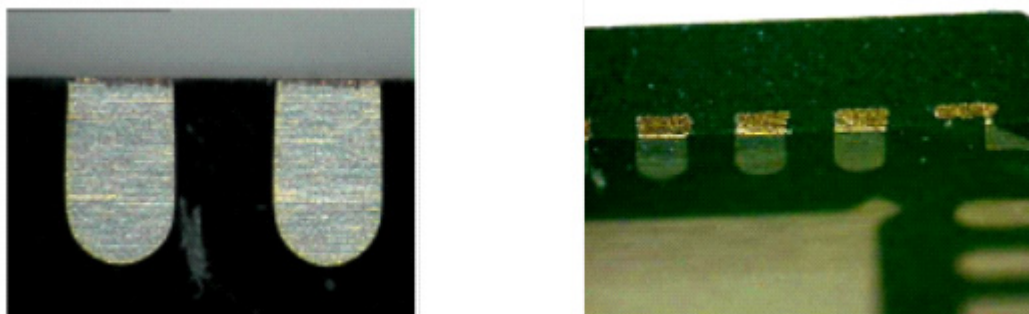


Figure 6. DFN/QFN "E" Version

3.3.3.2 MAP DFN/QFN: "S" style

The "S" style is a Freescale version based on JEDEC MO-220/MO-229, with an exception in the lead end feature. The S-type lead frames (see right photo in [Figure 7](#)) are half etch from the bottom where there is mold compound between the edge of the lead post to the edge of the package. The lead end is slightly recessed from the package perimeter due to a ½ etched lead frame. No solder fillet is expected after the solder reflow process. Freescale still supports S-type lead frames in production, but all new products will be using the E-type lead frames.

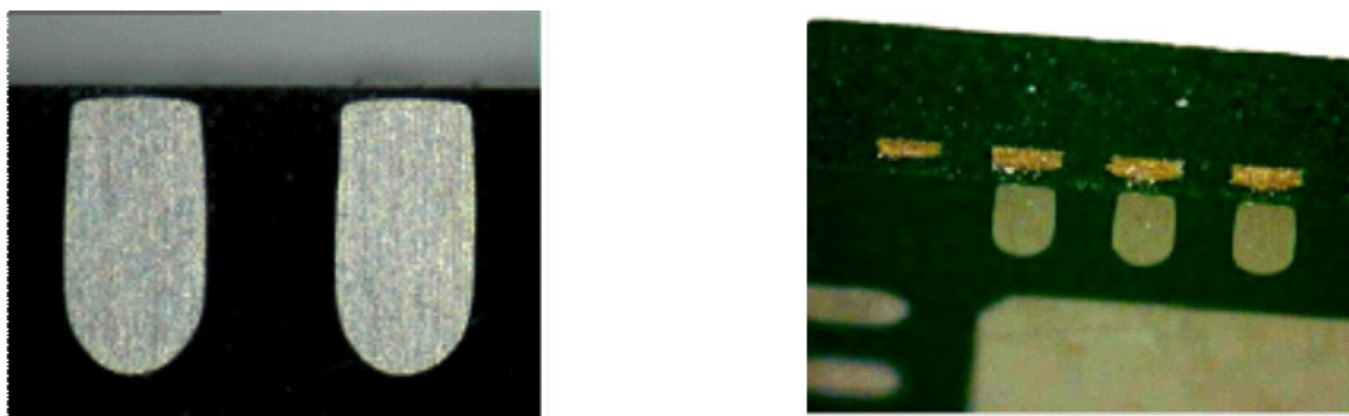


Figure 7. DFN/QFN "S" Version

3.3.3.3 MAP QFN: Dimpled Pad

Freescal QFN wettable flanks (WF) are mechanical modifications to the exposed surface of QFN lead ends that are formed during the half-etching step of the lead frame fabrication process. One version of the WF solutions is dimpled pad (**Figure 8**). Used with an optimized board mount process, dimpled pad improves the ability to inspect the solder joints and promotes formation of the inspectable solder joints (ISJ). The ISJ can be formed and should be visible on the PCB after the solder reflow process, shown in **Figure 9**. However, Freescale will not guarantee the forming of ISJ for QFN WF packages in a board mount process. Fillet size and shape are highly dependent upon solder paste, stencil opening, board layout, and reflow profile. To get optimal results, follow the guidelines in section "**PCB Pad Design**," on page 8.

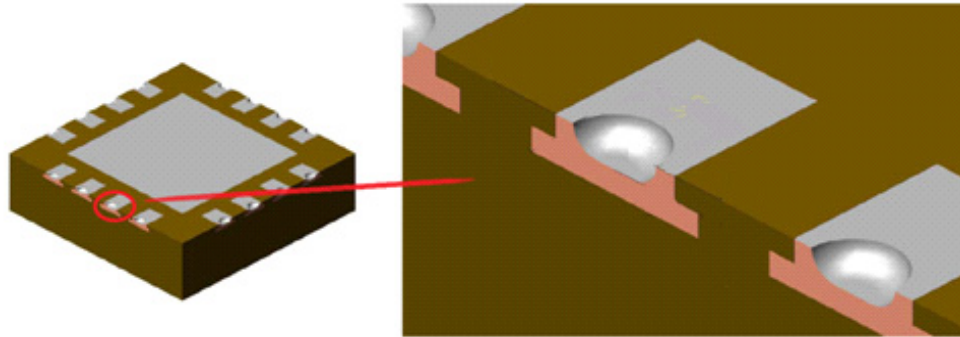


Figure 8. 16-lead QFN Dimpled Pads (6 x 6 mm)

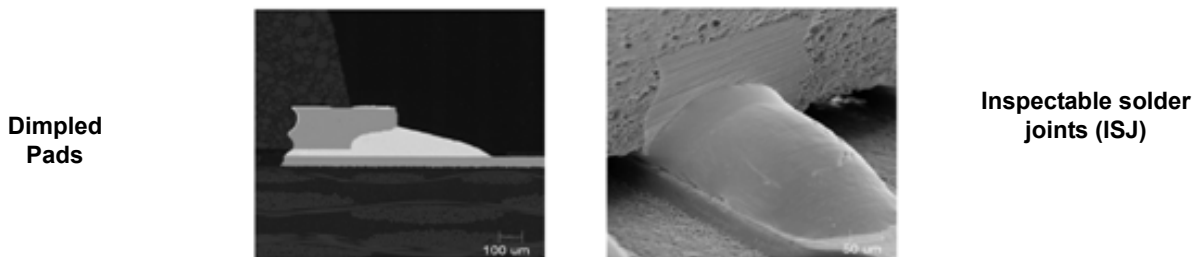


Figure 9. SEM Images of Dimpled Pads and Inspectable Solder Joints (ISJ)

4 Printed Circuit Board Guidelines

4.1 PCB Design Guidelines

As the package size shrinks and the lead count increases, the dimensional tolerance and positioning accuracy affects subsequent processes. Part interchangeability is also a concern when two separate suppliers provide production parts for the PCB. The optimized PCB layout for one supplier may have issues (manufacturing yield and/or solder joint life) with the other supplier's parts. When more than one source is expected, the PCB layout should be optimized for both parts. Additional information of this topic is provided in this section.

A proper PCB footprint and stencil designs are critical to surface mount assembly yields and subsequent electrical and mechanical performance of the mounted package. The design starts with obtaining the correct package drawing. Package Case Outline drawings are available at www.freescale.com. Follow the procedures in section "**Downloading the**

4.2 PCB Pad Design

4.2.1 General Pad Guidelines

Freescall follows the Generic Requirements for Surface Mount Design and Land Pattern Standards from the Institute for Printed Circuits (IPC), IPC-7351B.

- The document and an accompanying land pattern calculator can be purchased from the IPC's web site landpatterns.ipc.org, and include guidelines for a large number of DFN/QFN's, based on assumed package dimensions.
- Freescale also recommends considering the guidelines given IPC-7093 (Design and Assembly Process Implementation for Bottom Termination Components) for DFN/QFN PCB and process design.

Some general guidelines for a perimeter pad on DFN/QFN footprints are:

- All PCB pad calculation should be based on the nominal size of the package pad.
- The PCB pad should extend ~0.05 mm towards the center of the package.
- For customers seeking the ISJ packages to form the inspectable toe fillets, PCB Cu pad lengths exterior to the package edge should be at least 0.4 mm long.
- The PCB pad should not extend beyond the package edge for s-style packages.
- The PCB pad width should be approximately the same as the nominal package pad width. See [Table 2](#), "Recommended pad widths as a function of lead pitch," on page 10.
- Pitch needs to be designed in metric, using the exact dimensions of 0.40, 0.50, 0.65, 0.80, and 1.00 mm.
- No insertion components (THT or Through Hole Technology) or PCB vias should be placed at a distance less than 2 mm from the package land area.
- For perimeter PCB pads, it is recommended to use NSMD (Non-Solder Mask-Defined), because they provide significant advantages over SMD (Solder Mask-Defined) pads in terms of dimensional tolerances and registration accuracy. The NSMD has a solder mask opening that is larger than the copper pad, and the PCB pad area is controlled by the size of the copper pad. Since the copper pad etching process is capable and stable, a smaller size copper pad can be defined more accurately. The clearance around the copper pad and solder mask should be at least 75 μm , to account for the registration tolerance of the solder mask. [Table 12](#) shows the pad design concepts.



Figure 12. NSMD and SMD Pad Designs

Table 2. Recommended Pad Widths as a Function of Lead Pitch

Lead Pitch (mm)	Pad Width (mm)
0.40	0.20
0.50	0.25
0.65	0.37
0.80	0.40
1.00	0.50

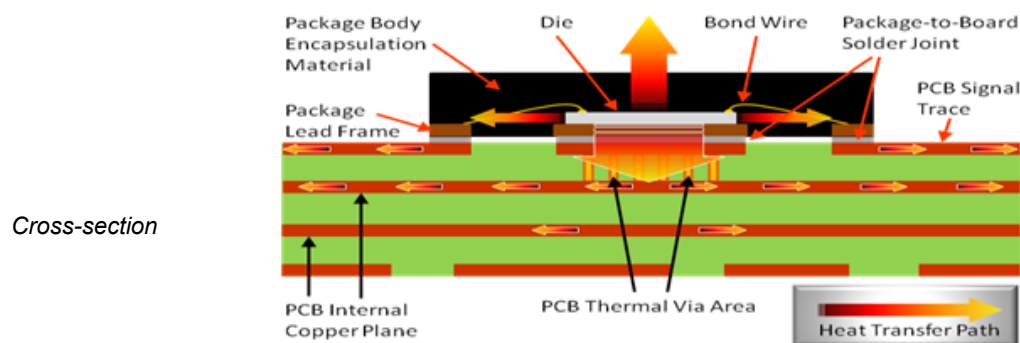
Notes

1. Some legacy products may have alternate pitches.

For applications using the 16QFN 6x6 stacked die sensor package, use Freescale application note AN3111, “Soldering the QFN Stacked Die Sensors to a PC Board” (download from www.freescale.com).

4.2.2 Thermal/Electrical Pad Guidelines

The majority of DFN/QFN packages are base on thermally/electrically enhanced lead-frame technology; the bottom of the package provides the primary heat removal path, as well as excellent electrical grounding to the PCB through an exposed pad (EP). In a DFN/QFN-EP package, the die attach paddle is at the same level as the perimeter pads within the package, such that the pad is exposed during the mold process, as shown in [Figure 13](#). To optimize thermal performance, the PCB design should include a thermal plane.

**Figure 13. DFN/QFN-EP Package Showing Heat Transfers**

Although the land pattern design of the perimeter pads for exposed pad attachment on the PCB should be the same as that for conventional, non-thermally/electrically enhanced packages, extra features are required during the PCB design and assembly stage, for effectively mounting thermally/electrically enhanced packages. In addition, repair and rework of assembled packages may involve some extra steps, depending upon the current rework practice within the company.

4.2.3 Exposed Pad Design, Spacing between PCB Perimeter Pads and EP

The design of land pattern and the size of the thermal pad depends strongly on the thermal characteristics and power dissipation of the specific product and application. To maximize both removal of heat from the package and electrical performance, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad (as shown in [Figure 14](#)).

The size of the land pattern can be larger, smaller, or even take on a different shape than the exposed pad on the package. However, the area that can be soldered (which should be defined by the solder mask) should be approximately the same size/shape as the exposed pad area on the package, to maximize the thermal/electrical performance. A clearance of at least

0.25 mm should be designed on the PCB between the outer edges of the exposed pad land pattern and the inner edges of perimeter pad pattern, to avoid any shorts. This topic is discussed in more detail in section “[Solder stencil/solder paste](#),” on page 12.

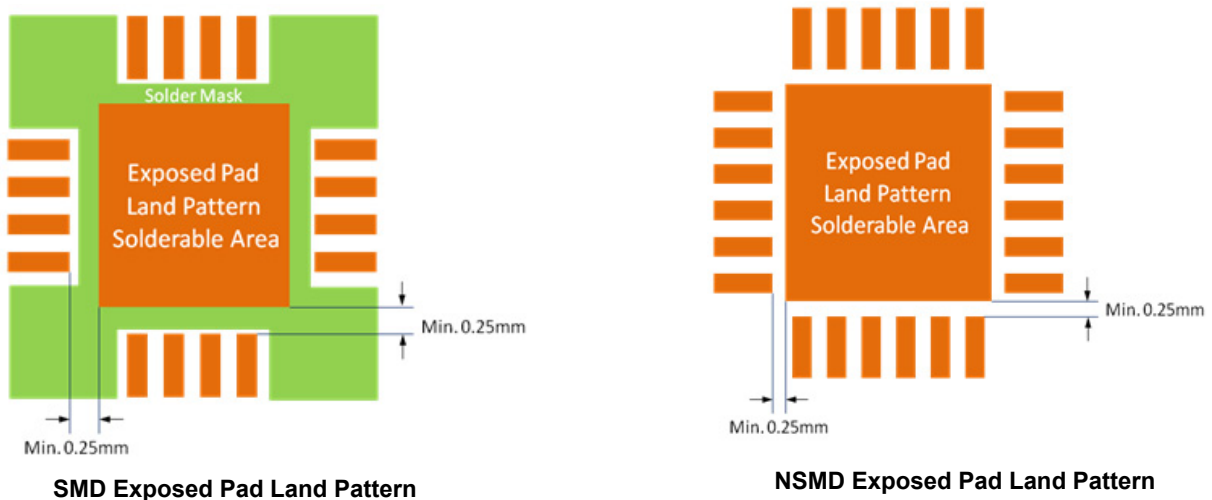


Figure 14. Minimum Clearance between Perimeter Pad and Exposed Pad Land Pattern (SMD, NSMD)

4.2.3.1 Alternative exposed pad design

Alternatively, the exposed pad solder land can be segmented into a symmetric pad array, as shown in Figure 15. The pad array can be created either by segmentation of a full copper area by solder mask, or by copper-defined outlines using NSDM defined pads.

- Recommended edge length of a matrix pad is between 1–2 mm.
- Recommended distance between the pads should be 0.4 mm.

The segmented PCB design facilitates the solder paste flux outgassing during reflow, thereby promoting a lower voiding level of the completed solder joint. At the same time, the maximum size of a single solder void is limited by the dimensions of a single matrix segment.

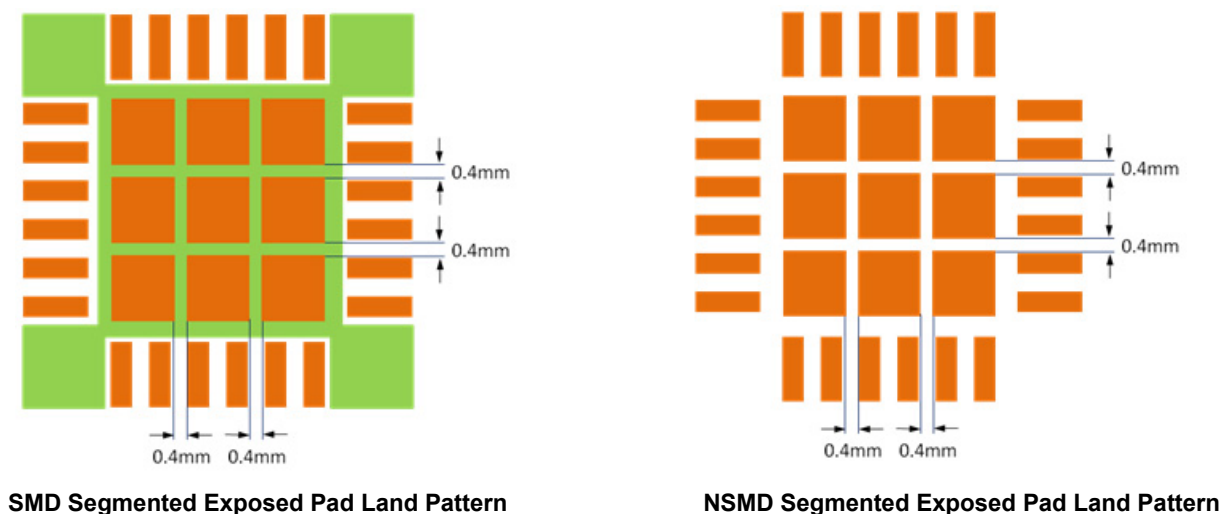


Figure 15. Alternative Exposed Pad Design, EP Segmented by Matrix Pad Design

4.2.4 Vias in the PCB-Exposed Pad Land Pattern

While the land pattern on the PCB provides a means of heat transfer/electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). These vias act as “heat pipes”. The number of vias is application-specific and depends upon the package power dissipation and electrical conductivity requirements. Thus, **thermal and electrical analysis and/or testing are recommended to determine the minimum number of vias required**. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern at a 1.2 mm grid, as shown in [Figure 16](#).

It is recommended that the via diameter be 0.30 to 0.33 mm with 1.0 ounce copper via barrel plating. This is desirable to avoid any solder-wicking inside the via during the soldering process, which may result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, then the thermal vias can be “tented” with solder mask on the top surface of the PCB, to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 0.1 mm (4.0 mils) larger than the via diameter.

NOTE: These recommendations are only to be used as guidelines.

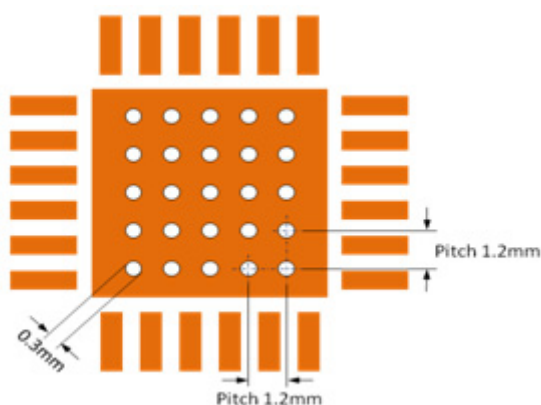


Figure 16. PCB-Exposed Pad Land Pattern via Grid

4.2.5 Pad Surface Finishes

Almost all PCB finishes are compatible with DFN/QFNs, including Organic Solderability Protectant (OSP), Electroless Nickel Immersion Gold (ENIG), Immersion Sn and Immersion Ag. Hot Air Solder Leveled (HASL) may cause uneven surface issues and extra caution is required.

4.2.6 Solder Mask Opening for PCB Area

Usually solder mask should be pulled away from the perimeter pads. The solder mask opening around the PCB pads can be as large as the spacing between pads. The area in between the pads may be too thin for the solder mask, resulting in the solder mask lifting off from the PCB.

- Minimum solder mask width will strongly depend on PCB manufacturer capabilities. FSL does not recommend any values (for minimum solder mask width), because they may not be compatible with the individual PCB supplier's technology.
- A potential solution is modification of the solder mask along the pad-to-pad spacing, so that only the “toes” of the pads are covered with solder mask (for better PCB strength).

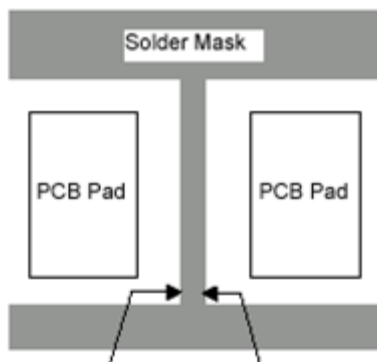


Figure 17. Pad and Solder Mask with Thin Webbing

5 Board Assembly

5.1 Assembly Process Flow

Figure 18 shows a typical Surface Mount Technology (SMT) process flow. **Use of standard pick and place process and equipment is recommended and manual or hand soldering should be avoided.**

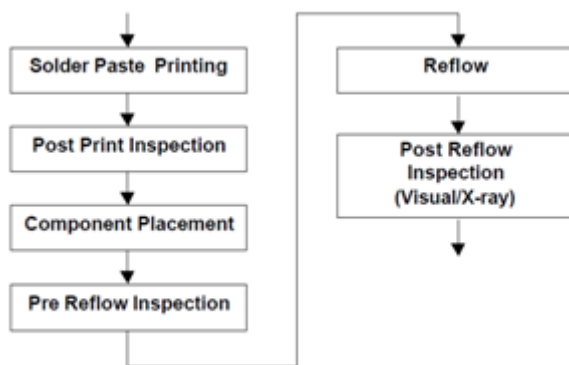


Figure 18. SMT Process Flow

5.2 Solder stencil/solder paste

For maximum thermal/electrical performance, it is required that the exposed pad on the package be soldered to the land pattern on the PCB. This can be achieved by applying solder paste on both the pattern for lead attachment, as well as on the land pattern for the exposed pad.

- For DFN/QFN without exposed pads (non-thermally/electrically enhanced), the stencil thickness depends on the lead pitch.
- On DFN/QFN with exposed pads, the EP stencil aperture openings should be 0.25 mm smaller than the copper pads on PCB, as shown in **Figure 19**. This will allow for proper registration of the stencil to the pad pattern.

A large stencil opening may result in poor release. To overcome this, the aperture opening should be subdivided into an array of smaller openings, similar to the thermal land pattern shown in **Figure 20**. These guidelines will result in the solder joint area to be about 80 to 90% of the exposed pad area.

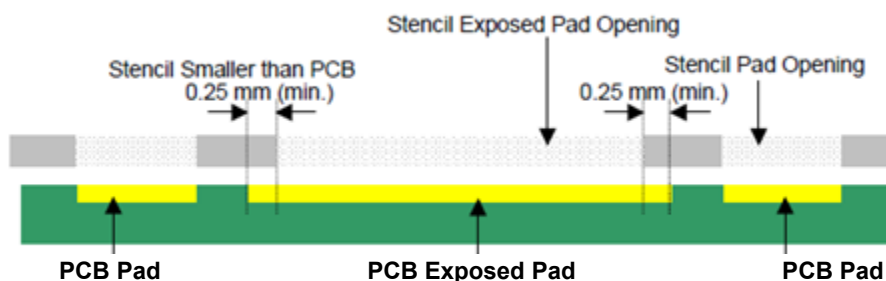


Figure 19. Reduced Solder Stencil Aperture for Exposed Pad

An array design pattern is recommended in the stencil opening for the large thermal pad region. A large opening or aperture in the thermal region allows "scooping" to occur during screen printing shown in Figure 20.1. Other reasons for segmenting the thermal regions include minimizing solder voids in the thermal region, and minimizing chances of bridging with terminal pads.

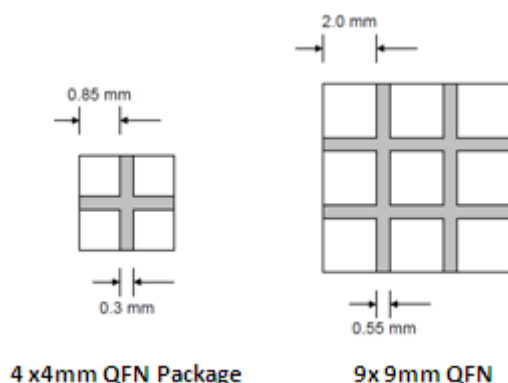


Figure 20. Stencil Array Design Examples (from a Freescale DFN/QFN Study)

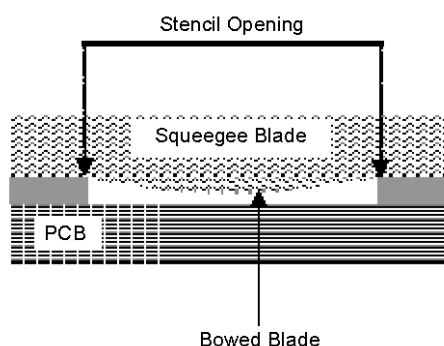


Figure 21. "Scooping" effect

Smaller DFN/QFN package sizes do not require any thermal pad pattern on the PCB and stencil, except to minimize solder voids. On larger packages, stencil thermal openings should be segmented in smaller regions. Examples are shown in [Figure 22](#). The spacing between segments either on the stencil or on the PCB should be 0.15 mm or more. Narrower spacing between segments can become a manufacturing issue.

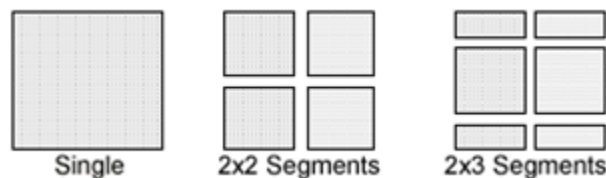


Figure 22. Segmented Stencil Openings

The stencil opening should be approximately 50 – 80% of the total PCB thermal pad area. This stencil-PCB thermal pad ratio ensures proper coverage of the thermal pad area with fewer voids, and minimizes the possibility of overflow bridging to the adjacent lead.

5.2.1 Stencil thickness

The thickness of the stencil determines the amount of solder paste deposited onto the printed circuit board land pattern. Due to the fine pitch and small terminal geometry used, care must be taken when printing the solder paste on to the PCB. A 0.127 mm (5.0 mil) thick stainless steel stencil is recommended for 0.50 mm pitch packages. Package pitches ≥ 0.65 mm can accommodate a 0.150 mm (6 mil) thick stencil.

Since DFN / QFN are (most likely) not the only package on the actual production PCB, the recommended stencil thickness for this package may be thinner than desired. For such a case, a step-down stencil is recommended, where most of the stencil for the PCB has a typical thickness, but the area for the DFN / QFN would be reduced to 0.127 to 0.150 mm (5 to 6 mils), depending on the package pitch.

5.2.2 Solder paste properties

Solder paste is one of the most important materials in the SMT assembly process. It is a homogenous mixture of metal alloy, flux, and viscosity modifiers. The metal alloy particles are made in specific size and shape. Flux has a direct effect on soldering and cleaning, and it is used to precondition the surfaces for soldering (by removing minor surface contamination and oxidation).

There are two different flux systems commonly available:

- The first type of flux system requires cleaning such as standard rosin chemistries and water-soluble chemistries. Standard rosin chemistries are normally cleaned with solvents, semi-aqueous solutions or aqueous/saponifier solutions, while the water-soluble chemistries are cleaned with pure water.
- The second type of flux system type requires no cleaning, but normally a little residue will remain on the PCB after soldering. In general, it is recommended to use a no-clean solder paste, because the cleaning of flux residues from underneath the package is not feasible for a DFN/QFN-style package (due to the low package stand-off). However, you should evaluate your entire process and usage to ensure desired results.

The spread of solder paste during reflow partially depends upon the solder paste alloy. Given the same reflow temperature, SnPb solder alloys spread significantly better than the many lead-free pastes (like SnAgCu, SnAgBiCu, and others).

5.3 Component placement

Increased package pad interconnection and insertion density requires precise and accurate placement tools. To meet this tight requirement, the placement machine should be equipped with optical recognition systems (like a vision system), for the centering of the PCB and the components during the pick-and-place motion. A placement accuracy study is recommended to calculate compensations required. Freescale follows the EIA-481-D standard for tape-and-reel orientation, as shown in [Figure 23](#). One exception for the orientation is that for the 2x2, pin #1 is at quadrant #1.

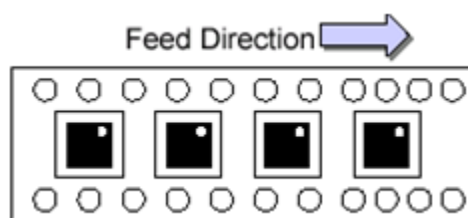


Figure 23. DFN/QFN Orientation in Tape-and-Reel (example)

The identification of pin 1 on the bottom side of the DFN/QFN package varies from supplier to supplier. If parts are supplied by more than one DFN/QFN supplier, then it is necessary to create equipment recipes for each DFN/QFN supplier. The lead frame finish of each supplier may reflect differently in the vision system, especially between NiPdAu and SnPb.

5.4 Soldering

A typical profile band is shown in [Figure 24](#). The actual profile parameters depend upon the solder paste used; the recommendations from paste manufacturers should be followed. The temperature profile is the most important control in reflow soldering, and it must be fine tuned to establish a robust process. In most cases, thermocouples should be placed under the heaviest thermal mass device on the PCB, to monitor the reflow profile. Generally, when the heaviest thermal mass device reaches reflow temperatures, all other components on the PCB will have reached reflow temperatures as well.

Nitrogen reflow is recommended to improve solderability and to reduce defects (like solder balls). It is also recommended to monitor the temperature profile of package top surfaces, to validate that the package peak temperature does not exceed the MSL classification of individual devices.

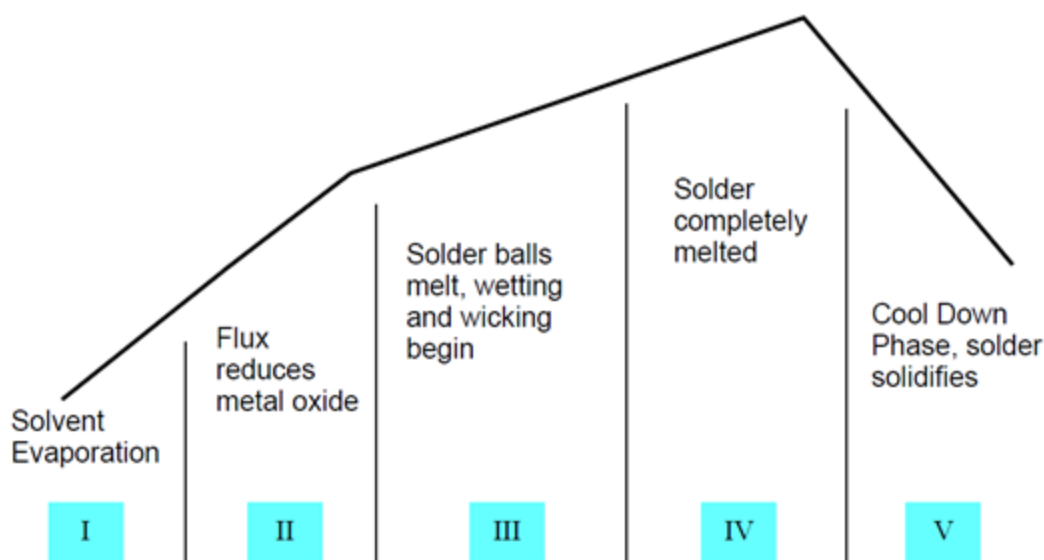


Figure 24. General Solder Reflow Phases

For all devices on the PCB, the solder paste needs to be taken into account for the reflow profile. Every paste has a flux, and the flux dominates the reflow profile for steps (like soak time, soak temperature, and ramp rates). Peak reflow temperature is the melting temperature of the metals in the paste, plus a “safety” margin to ensure that all solder paste on the PCB reflows. The reflow profile for exposed pad packages need not be any different than the one used for non-thermally/electrically enhanced packages.

The reflow profile should follow the paste supplier's "recommended" profile. Deviation from the recommended profile should be evaluated first using a copper (Cu) coupon test. The horizontal size for a typical solder paste volume is measured as either a diameter or as "x" and "y" lengths. The Cu coupon is then subject to reflow and the solder paste volume is measured for either diameter or "x" and "y". The goal is have a reflow profile with the most horizontal spread. For best results, the Cu coupon should be lightly sanded before use (to remove Cu-oxide build-up). PCB should be rated for multiple reflow of MSL classification. Cross referencing with the device data sheet is recommended for any additional board assembly guidelines specific to the exact device used.

5.5 Inspection

Unlike traditional leaded components, the solder joints of DFN/QFN are formed primarily *underneath the package*. To verify any open or short circuits (bridging) after reflow, optical inspection and x-ray inspection are recommended. Micro-Sectioning is another method of inspecting solder joint quality during process optimizations, but it is less suitable to production inspection (due to slow processing).

Figure 25 shows the expected x-ray image of an soldered component. The voids under the paddle are not regarded as defective.

Assembled 44QFN 9x9 with segmented exposed pad solder land, thermal vias in the exposed pad land, and a daisy-chain wire bond configuration

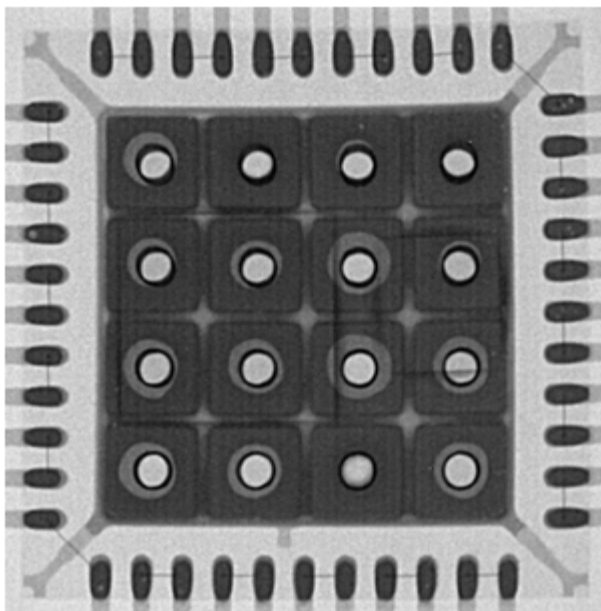


Figure 25. Inspection X-ray of a QFN package

5.6 Additional precaution

Following special care for accelerometer QFN is recommended.

- Avoid screwing down the PCB near the accelerometer to fix it into an enclosure as this may cause the PCB to bend.
- Avoid using Hot Air Solder Leveling (HASL) may cause uneven surface issue.
- For consumer parts avoid soldering the exposed pad.

5.7 Common DFN/QFN defects

Shorts and Bridging
on Perimeter Pads

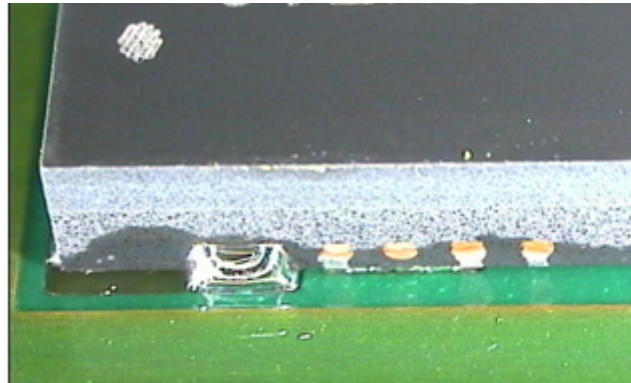
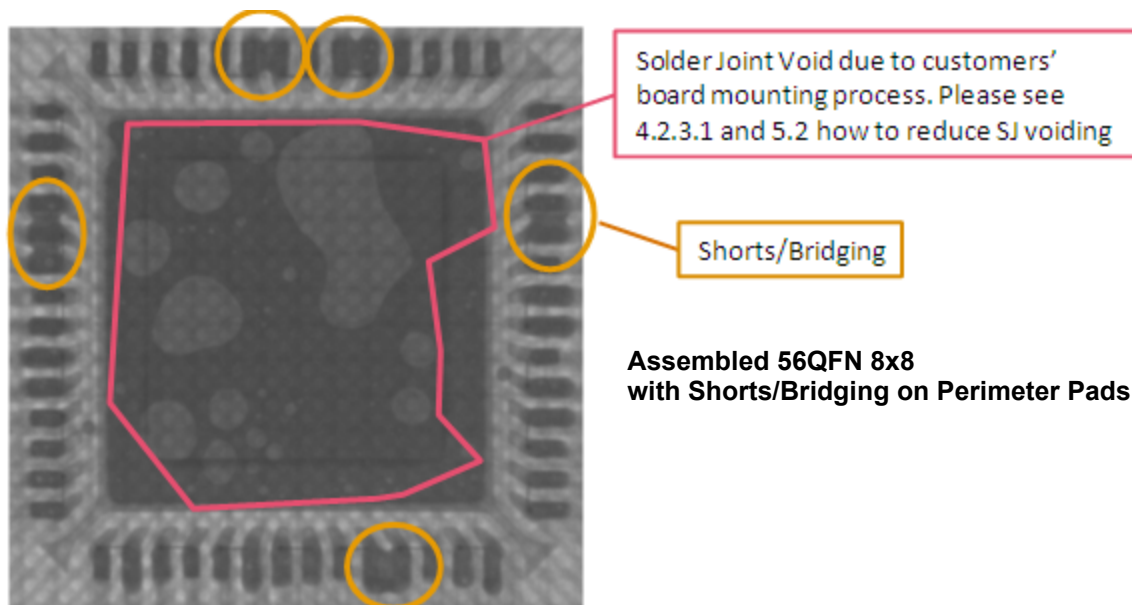


Figure 26. Assembled DFN/QFN with Shorts/Bridging Defects



Assembled 56QFN 8x8
with Shorts/Bridging on Perimeter Pads

Figure 27. X-ray of QFN Package with Shorts/Bridging Defects

6 Repair and Rework Procedures

6.1 Repairing

Repairing a single solder joint of DFN/QFN or the soldered exposed die pad is not recommended, because the joint/pin or EP is *underneath the package*.

6.2 Reworking

If a defective component is observed after board assembly, the device can be removed and replaced by a new one. This rework can be performed using the heating methods described in this section.

When performing the rework:

- The influence of the heating on adjacent packages must be minimized. Do not exceed the temperature rating of the adjacent package.
- Heating conditions will differ due to differences in the heat capacities of the PCB (board thickness, number of layers) and mounted components used; thus, the conditions must be set to correspond to the actual product and its mounted components.
- Freescale follows industry-standard component level qualification requirements, which include three solder reflow passes. The three reflow passes simulate board level attach to a double-sided board and includes one rework pass. The removed DFN/QFN package should be properly disposed of, so that they will not mix in with new components.

A typical DFN/QFN rework flow process comprises seven stages:

1. **Tooling Preparation**
2. **Package Removal**
3. **Site Redressing**
4. **Solder Paste Printing**
5. **Package Remount**
6. **Reflow Soldering**
7. Visual check

NOTE: Freescale product quality guaranty/warranty does not apply to products that have been removed, thus, component reuse should be avoided.

In any rework, the PCB will be heated. The thermal limits of PCB and components (e.g., MSL information) must be followed. During heating, the combination of rapid moisture expansion, materials mismatch, and material interface degradation can result in package cracking and/or delamination of critical interfaces within the components and PCB. In order to prevent moisture induced failures, it is recommended that the PCBs and components have had strict storage control with a controlled environment (such as dry air or nitrogen). In addition, a pre-bake (e.g., 125°C for 24 hours for boards with SMT components, or 95°C for 24 hours for boards with temperature sensitive components) is recommended to remove the moisture from components and the PCB prior to removal of the DFN/QFN package, if the maximum storage time out of the dry pack (see label on packing material) is exceeded after board assembly.

Individual process steps for reworking a DFN/QFN package are described in subsequent sections:

6.2.1 Tooling Preparation

Various rework systems are available on the market. In general, the rework station should have a split light system, an XY table for alignment, and a hot air system (with a top and bottom heater for component removal). For processing DFN/QFN packages, a system should meet the following requirements:

- **Heating** – Controlled hot air transfer (temperature and air flow) to both the DFN/QFN package and its mounted PCB is strongly recommended. The heating should be appropriate for the correct package size and thermal mass. PCB preheating from beneath is recommended. Infrared heating can be applied, especially for preheating the PCB from the underside, but it should only augment the hot air flow from the upper side (component side). Nitrogen can be used instead of air. Also see section “**Package Removal**”, on page 19.
- **Vision system** – The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of the package to PCB, a split light system should be implemented. Microscope magnification and resolution should be appropriate for the pitch of the device.
- **Moving and additional tools** – Placement equipment should have good accuracy. In addition, special vacuum tools may be required to remove solder residue from PCB pads.

6.2.2 Package Removal

If a component is suspected to be defective and is returned, no further defects must be introduced to the device during removal of the component from the PCB, because this may interfere with subsequent failure analysis. The following recommendations are intended to reduce the chances of damaging a component during removal:

- **Moisture removal** – Dry bake components before removal at 125°C for 16 – 24 hours for boards with SMT components, or at 95°C for 16 – 24 hours for boards with temperature-sensitive components.
- **Temperature profile** – During de-soldering, ensure that the package peak temperature is not higher and that the temperature ramps are not steeper than the standard assembly reflow process.
- **Mechanics** – Do not to apply high mechanical forces for removal. High force can damage the component and/or the PCB, which may limit failure analysis of the package.
 - For large packages, pipettes can be used (implemented on most rework systems).
 - For small packages, tweezers may be more practical.

If suspected components are fragile, then it is especially necessary to determine if they can be electrically tested directly after de-soldering, or if these components have to be preconditioned prior to testing. In this case, or if safe removal of the suspected component is not possible (or too risky), the whole PCB (or the part of the PCB containing the defective component) should be returned.

An air nozzle of correct size should be used to conduct the heat to the DFN/QFN component leads, so that a vacuum pick up tool can properly remove the component. The temperature setting for the top heater and the bottom heater depends on the component rating. See [Figure 28](#). Many assembly sites have extensive in-house knowledge on rework, and their experts should be consulted for further guidance.



Figure 28. Package Removal Process

If the PCB is large, then it is important to avoid bending of the printed circuit material due to thermal stress, so a bending prevention tool must be placed on the bottom of the printed circuit board, and a bottom heater installed (to allow heating of the entire printed circuit board, in order to raise work efficiency).

6.2.3 Site Redressing

After the component is removed, the PCB pads must be cleaned to remove solder residue, in order to prepare for the new component placement. This may be completed by vacuum de-soldering, solder sucker, solder wick braid, etc., after applying flux. Remaining solder residue and projections can cause the solder stencil to not closely adhere to the substrate during solder paste printing, leading to improper solder paste supply during component mount.

Moreover, when the solder residue flows all the way to an adjacent through-hole, the solder paste printed on the pad can be transfer via suction, to the through-hole during reflow, which may cause improper connection. A solvent may be necessary to clean the PCB of flux residue. A de-soldering station can be used for solder dressing. It should be noted that the applied temperature should not exceed 245°C, which can contribute to PCB pad peeling from the PCB. This is typically a manual operation that is directly attributed to experience and skill.

Non-abrasive or soft bristle brushes should be used as abrasive brushes can contribute to bad solder joints (e.g., steel brushes). Before placing a new component on the site, solder paste should be applied to each PCB pad (by printing or dispensing). A no-clean solder paste is recommended.

6.2.4 Solder Paste Printing

Solder supply during rework is done using specialized templates and tools. A mini-stencil with the same stencil thickness, aperture opening, and pattern as the normal stencil are placed in the component site. A mini-metal squeegee blade deposits solder paste in the specific area. See [Figure 29](#). The printed pad should be inspected, to ensure even and sufficient solder paste before component placement.

If neighboring parts are so close to the DFN/QFN components that the mini-stencil method is not an option, then apply solder paste carefully on each pad using a paste dispensing system. The volume of solder paste must be controlled, to prevent shorting on the component and/or neighboring components.

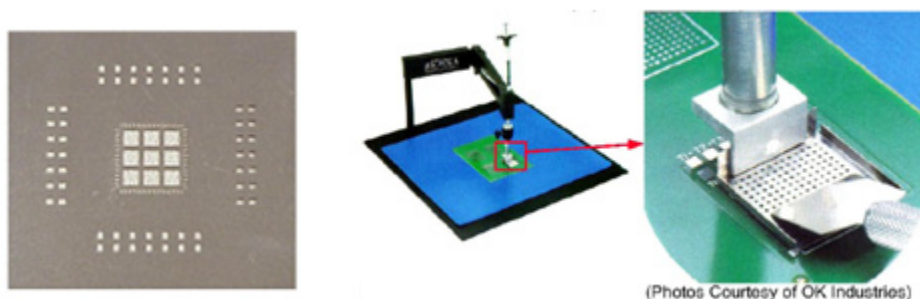


Figure 29. Mini-Stencil and Mini-Squeegee

6.2.5 Package Remount

After preparing the site, the new package can be placed onto the PCB. When remounting the package, consider using rework equipment that has good optical or video vision capability. A split light system displays images of both package leads and PCB pads by superimposing two images. Alignment of the leads and pads is completed with an adjusting XY which enables correct soldering. See [Figure 30](#).

Regular lead array DFN/QFN exhibits self-alignment in any direction, including X-axis shift, Y-axis shift, and rotational misplacement. Exposed pads may not exhibit a strong self-alignment capability, so precise placement of the component on the PCB is required.

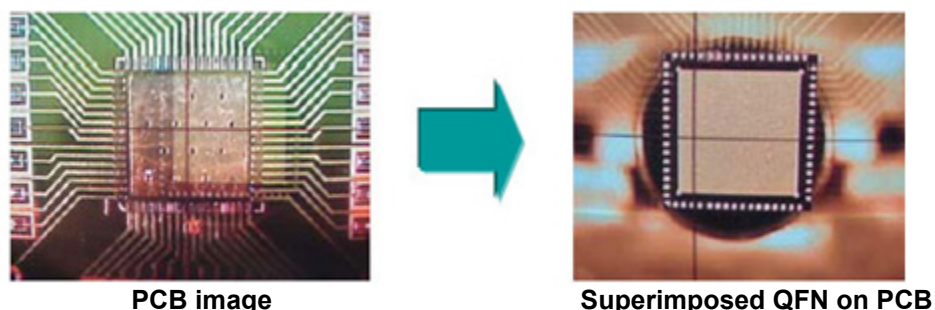


Figure 30. Split Light Placement Images

6.2.6 Reflow Soldering

The new component is soldered to the PCB using the same temperature profile as the normal reflow soldering process (section “[Soldering](#)”, on page 15). During soldering, the package peak temperature and temperature ramps must not exceed those of the standard assembly reflow process.

In IR or convection processes, the temperature can vary greatly across the PC board, depending on the furnace type, size and mass of components, and the location of components on the assembly. Profiles must be carefully tested to determine the hottest and coolest points on the assembly. The hottest and coolest points should fall within recommended temperatures in the reflow profile. To monitor the process, thermocouples must be carefully attached with very small amounts of thermally conductive grease (or epoxy) directly to the solder joint interface between the package and board.

The materials used in rework do have a higher potential to create conductive traces, corrosion, etc., compared to standard materials, and the PCB might need to be cleaned if they do not get clean in the “normal” process, or if the rework was not done using “no clean” materials.

7 Board Level Reliability

7.1 Solder joint reliability testing

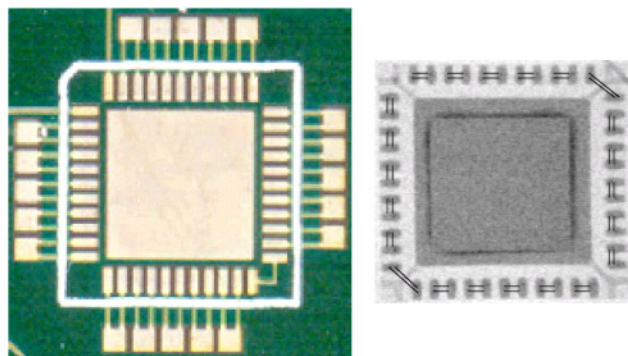
Solder Joint Reliability (SJR) testing is performed to determine a measure of board level reliability when exposed to thermal cycling. The information provided here is based on experiments performed on a DFN/QFN device using a daisy-chain bond configuration. Actual surface mount process and design optimizations are recommended to develop an application specific solution.

- For automotive grade product applications, Freescale typically prefers to reach a minimum of 2000 cycles before first solder joint failure in SJR experiments. The widely accepted temperature range for testing is -40°C to +125°C.
- Consumer SJR temperature cycling conditions may vary widely, depending on the application and specific user. Typically, Freescale consumer SJR testing is performed from 0°C to +100°C.

Table 3 shows the Freescale standard test set-up for performing board-level solder joint reliability testing. Example of daisy-chain test PCB and QFN package is shown in [Figure 31](#).

Table 3. Board-Level Reliability Test Set-Up

Board Level Reliability Testing: Material and Test Setup	
PCB Board	<ul style="list-style-type: none"> • 1.58 mm thickness • Four Cu layer • OSP surface finish
Test Board Assembly	<ul style="list-style-type: none"> • Pb-free solder paste SAC387 • Reflow peak temperature for SAC assembly ~ 240 °C • Pb solder paste Sn63Pb37 • Reflow peak temperature for SnPb assembly ~ 220 °C • 0.100 - 0.150 mm thickness (depending on the device pitch), Ni plated, laser cut and electro-polished stainless steel stencil
Cycling conditions	<ul style="list-style-type: none"> • Continuous in-situ daisy chain monitoring per IPC-9701A • Air-Temperature Cycling (ATC) for Automotive <ul style="list-style-type: none"> — -40 °C / +125 °C — 15 minute ramp/ 15 minute dwell — 1.0 hour cycle time • Air-Temperature Cycling (ATC) for Commercial & Industrial <ul style="list-style-type: none"> — 0 °C / +100 °C — 10 minute ramp/ 20 minute dwell — 1.0 hour cycle time
Package Test Vehicle	<ul style="list-style-type: none"> • Production BOM package including die (die mechanically present, without wire bond connection) • Daisy chain bond pattern on lead frame to allow continuous monitoring



Daisy chain test PCB

Daisy chain test PCB

Figure 31. Daisy-Chain Test PCB and QFN Package

7.2 Solder Joint Reliability Results

Freescall experimentally gathers board-level reliability data for a variety of packages. To get results from these experiments (including Weibull plots), contact the Freescall sales team.

8 Thermal Characteristics

8.1 General Thermal Performance

Since the thermal performance of the package in the final application will depend on a number of factors (like board design, power dissipation of other components on the same board, ambient temperature), the thermal package properties provided by Freescall should only serve as a guideline for the thermal application design. In applications where the thermal performance is considered to be critical, Freescall recommends to run application-specific thermal calculations in the design phase, to confirm the on-board thermal performance.

Exposed pad packages may require the exposed pad to be connected to the PCB for thermal and/or electrical measurement. For optimized thermal performance, it is recommended to form a thermal pass into the PCB, by connecting the exposed pad to the top and/or bottom and/or inner copper layers of the PCB. The PCB copper area and number of thermal vias connected to the exposed pad required to achieve the proper thermal performance on the PCB is application-specific, and will depend on the package power dissipation and the individual board properties (thermal resistance of the application PCB).

8.2 Package Thermal Characteristics

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

Additional factors to be considered in PCB design and the thermal rating of the final application (amongst others) are:

- Thermal resistance of the PCB (thermal conductivity of PCB traces, number of thermal vias, thermal conductivity of thermal vias)
- Quality and size of PCB solder joints (effective PCB pad size, potential solder voiding in the thermal path solder joints that may reduce the effective solder area)

The thermal characteristics of the package provide the thermal performance of the package when there are no nearby components dissipating significant amounts of heat. The stated values are meant to define the package thermal performance in a standardized environment.

Thermal properties of the individual products are usually given in the Freescale product data sheets as appropriate. Product data sheets are available at www.freescale.com. For more detailed thermal properties, contact Freescale.

8.3 Package Thermal Properties—Definition

The thermal performance of DFN/QFN packages with and without exposed pads is typically specified by thermal properties such as $R_{\theta JA}$, $R_{\theta JMA}$, $R_{\theta JB}$, $R_{\theta JC}$ and Ψ_{JT} (in $^{\circ}\text{C}/\text{W}$). Thermal characterization is performed by physical measurement and by running complex simulation models under the following conditions:

- Two thermal board types:
 - Single-layer board (1s), per JEDEC JESD51-3 & JESD51-5 (exposed pad packages only)
 - Four-layer board (2s2p), per JEDEC JESD51-7 and JESD51-5 (exposed pad packages only)
- Four boundary conditions:
 - Natural convection (still air), per JEDEC JESD51-2
 - Forced convection, per JEDEC JESD51-6
 - Thermal test board on ring style cold plate method, per JEDEC JESD51-8
 - Cold plate method, per MIL SPEC-883 method 1012.1

8.3.1 $R_{\theta JA}$: Theta Junction-to-Ambient Natural Convection (Still Air)

Junction-to-ambient thermal resistance (Theta-JA or $R_{\theta JA}$ per JEDEC JESD51-2) is a one-dimensional value that measures the conduction of heat from the junction (of the hottest temperature on die) to the environment (ambient) near the package in a still air environment. The heat that is generated on the die surface reaches the immediate environment along two paths:

- Convection and radiation off the exposed surface of the package, and
- Conduction into-and-through the test board, followed by convection and radiation off the exposed board surfaces.

8.3.2 $R_{\theta JMA}$: Theta Junction-to-Moving-Air Forced Convection

Junction-to-Moving-Air (Theta-JMA or $R_{\theta JMA}$ per JEDEC JESD51-6) is similar to $R_{\theta JMA}$, but it measures the thermal performance of the package mounted on the specified thermal test board, when it is exposed to moving air (at 200 feet/minute) environment.

8.3.3 $R_{\theta JB}$: Theta Junction-to-Board

Junction-to-board thermal resistance (Theta-JB or $R_{\theta JB}$ per JEDEC JESD51-8) measures the horizontal spreading of heat between the junction and the board. The board temperature is measured on the top surface of the board near the package. The measurement is done using a high effective thermal conductivity four-layer test board (2s2p) per JEDEC JESD51-7 and JESD51-5 (exposed pad packages only) on a ring style cold plate.

$R_{\theta JB}$ is frequently used by customers to create thermal models considering both package and application board thermal properties.

8.3.4 $R_{\theta JC}$: Theta Junction-to-Case

Junction-to-Case thermal resistance (Theta-JC or $R_{\theta JC}$ per MIL SPEC-883 Method 1012.1) indicates the average thermal resistance between the die and the case top surface, as measured by the cold plate method per MIL SPEC-883 Method 1012.1, with the cold plate temperature used for the case temperature. The case temperature is defined as

- either the temperature at the top of the package (for non-exposed pad packages),
- or the temperature at the bottom of the exposed pad surface (for exposed pad packages).

For exposed pad packages where the pad would be expected to be soldered, the junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance. $R_{\theta JC}$ can be used to estimate the thermal performance of a package when the board is adhered to a metal housing or heat sink, or when a complete thermal analysis is done.

8.3.5 Ψ_{JT} (Psi JT): Junction-to-Package Top

Junction-to-Package top (Psi JT or Ψ_{JT}) indicates the temperature difference between the package top and the junction temperature, optionally measured in a still air condition (per JEDEC JESD51-2) or in a forced convection environment (per JEDEC JESD51-6). Ψ_{JT} must not be confused with the parameter $R_{\theta JC}$: $R_{\theta JC}$ is the thermal resistance from the device junction to the external surface of the package, with the package surface held at a constant temperature, while Ψ_{JT} is the value of the temperature difference between the package surface and the junction temperature, usually in natural convection.

8.4 Package Thermal Properties: An Example

Table 4 shows an example of the thermal characteristics typically shown in a Freescale product data sheet. The example applies to a package size 7mm x 7mm x 1mm, 5.1mm x 5.1mm exposed pad, pitch 0.5 mm, and die size ~ 4.7mm x 4.7mm.

Freescale gathers all thermal data for a variety of packages. To obtain thermal properties (such as $R_{\theta JA}$, $R_{\theta JMA}$, $R_{\theta JB}$, $R_{\theta JC}$, and Ψ_{JT}) for your specific package, contact the Freescale sales team.

Table 4. Thermal Parameters of a Package (7 mm x 7 mm x 1 mm)

Rating	Board Type	Parameter	Value	Unit	Notes
Junction-to-Ambient (Natural Convection)	Single Layer board (1s)	$R_{\theta JA}$	74	°C/W	(2) (3)
Junction-to-Ambient (Natural Convection)	Four-layer board (2s2p)	$R_{\theta JA}$	28	°C/W	(2) (4)
Junction-to-Ambient (at 200 ft/min)	Four-layer board (2s2p)	$R_{\theta JMA}$	23	°C/W	(2) (4)
Junction-to-Board		$R_{\theta JB}$	7	°C/W	(5)
Junction-to-Case		$R_{\theta JC}$	0.8	°C/W	(6)
Junction-to-Package-Top	Natural Convection	Ψ_{JT}	14.4	°C/W	(7)

Notes

- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board temperature) ambient temperature air flow power dissipation of other components on the board, and the thermal resistance.
- Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
- Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- Thermal resistance between the die and the exposed pad surface as measured by the cold plate method (MIL Spec-883 Method 1012.1).
- Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT

9 Case Outline Drawing, MCDS and MSL Rating

9.1 Downloading the Information from Freescale

The complete case outline drawing and the Material Composition Declaration Sheet (MCDS, in IPC-1752 reporting format) can be downloaded from the Freescale website as PDF files. Information on product specific Moisture Sensitivity Level (MSL) is also available on the website.

To download the documents:

1. Go to www.freescale.com
2. In the orange box on the upper right of the screen, click “Orderable Part”.
3. In the upper right entry box “Enter Part Number”, enter the Freescale product part number.



Figure 32. The www.freescale.com Main Page

4. The next screen will be a return of search results, and will list all formal and existing part numbers related to the search term. On the search results screen, identify the row that contains the desired part number. In the “Package Description and Diagram” column, click the package description link on the row of the part number that you are interested in.

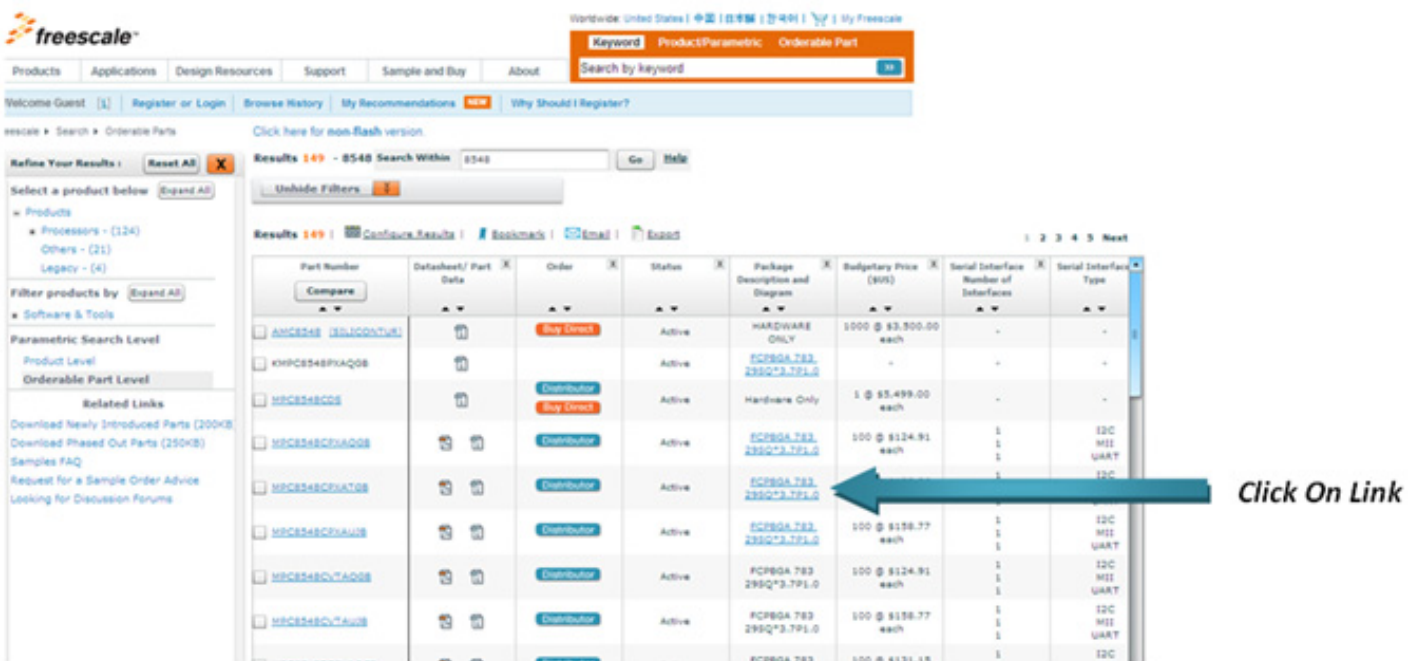


Figure 33. View of Search Results

5. The next screen should show the “Product Summary Page”.
 - To open the case outline PDF file, click the package description link in the “Package Information” table (FCPBGA 783 29SQ*3.7P1.0 in the example),
or
 - To open the MCDS PDF file, click the “Download IPC-1752 Report” link in the “Environmental and Compliance Information” table,
or
 - To see the moisture sensitivity level (MSL) and the maximum allowed peak package body temperature (PPT), look in the related columns.

Parameter	Value
Package Description and Mechanical Drawing	FCPBGA 783 29SQ*3.7P1.0
Device Weight (g)	11.52000
Pin/Lead/Ball Count	783
Package Material	Plastic
Mounting Style	Surface Mount
Package Length (nominal) (mm)	29.000
Package Width (nominal) (mm)	29.000
Package Thickness (nominal) (mm)	3.380
Tape & Reel	No

Parameter	Value
Pb-Free	No
RoHS Compliant	No
RoHS technical exemptions	NA
Material Composition Declaration (MCD)	Download IPC-1752 Report
RoHS Certificate of Analysis (CoA)	Contact CS
Moisture Sensitivity Level (MSL)	3
Floor Life	598 HOURS
Peak Package Body Temperature (PPT)(°C)	200
Maximum Time at Peak Temperature (s)	40
Number of Reflow Cycles	3
REACH SVHC	Freescall REACH Statement

Figure 34. Product Summary Page

9.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) indicates the floor life of the component, its storage conditions, and handling precautions after the original container has been opened. The permissible time (from opening the moisture barrier bag until the final soldering process) that a component can remain outside the moisture barrier bag is a measure of the sensitivity of the component to ambient humidity.

In many cases, **moisture absorption leads to moisture concentrations in the component that are high enough to damage the package during the reflow process**. The expansion of trapped moisture can result in interfacial separation, known as delamination, of the mold compound from the die or lead-frame, wire bond damage, die damage, and internal cracks. In the most severe cases, the component will bulge and pop, which is known as the "popcorn" effect.

Therefore, it is necessary to dry moisture-sensitive components, seal them in a moisture barrier antistatic bag (with a desiccant and a moisture indicator card), which is then vacuum sealed according to IPC/JEDEC J-STD-033. You should only remove them (the moisture-sensitive components) immediately prior to assembly onto the PCB.

Table 5 presents the MSL definitions per IPC/JEDEC's J-STD-20. Also refer to the “Moisture Sensitivity Caution Label” on the packing material, which contains information about the moisture sensitivity level of Freescale products. Components must be mounted and reflowed within the allowable period of time (floor life out of the bag), and the maximum reflow temperature that shall not be exceeded during board assembly at the customer's facility.

Table 5. MSL Descriptions

Level Rating	Floor Life	
	Time	Conditions
1	Unlimited	30°C/85% RH
2	1 Year	30°C/60% RH
2a	4 Weeks	30°C/60% RH
3	168 Hours	30°C/60% RH
4	72 Hours	30°C/60% RH
5	48 Hours	30°C/60% RH
5a	24 Hours	30°C/60% RH
6	TOL	30°C/60% RH

TOL = Time on Label

If moisture-sensitive components have been exposed to ambient air for longer than the specified time according to their MSL rating, or if the humidity indicator card indicates too much moisture after opening a Moisture Barrier Bag (MBB), then the components are required to be baked prior to the assembly process. To determine allowable maximum temperature, see the imprints/labels on the respective packing.

The lower the MSL value is, the less care is needed to store the components. The DFN/QFN package MSL reliability depends upon the different supplier material set and package size. [Figure 6](#) depicts the best case MSL for each package size at the time of this document's release. Freescale packages use JEDEC standard IPC/JEDEC J-STD-020 for the classification of its package.

Table 6. MSL Capability of DFN/QFN Packages

Package Type	Body Size L X W	IO Count	MSL	PPT
DFN	2x2	10	3	260
	3x3	10	3	245
DFN-EP	2x2	8	1	260
	2x3	8	1	260
	3x3	6/12	1 ~ 3	260
	4x4	8	3	260
QFN	4x4	24	2	220
	9x9	64	2	260
QFN-EP	3x3	12/16/20	1 ~ 3	260
	3x4	20	3	260
	4x4	16/20/24/28/32	1 ~ 3	260
	5x5	16/20/24/32/40	3	260
	6x6	16/40	3	260
	7x7	32/48	3	260
	7x7 Dual	76	3	250
	8x8	56	3	250
	9x9	64	3	260
	5x5	32	3	260
Punch QFN-EP	6x6	40	2A	250
	7x7	32/48	3	260
	9x9	44	3	260

8. This table and application note list all of the Freescale packages that this application note applies to, but some types of packages here may not be available now. Check with the Freescale sales team.

10 Package Handling

10.1 Handling ESD Devices

Semiconductor Integrated Circuits (ICs) and components are Electrostatic-Discharge-Sensitive devices (ESDS), so proper precautions are required for handling and processing them. Electrostatic Discharge (ESD) is one of the significant factors leading to damage and failure of semiconductor ICs and components, and comprehensive ESD controls to protect ESDS during handling and processing should be considered.

The following industry standards describe detailed requirements of proper ESD controls; Freescale recommends meeting the standards before handling and processing ESDS. Detailed ESD specifications of devices are available in each device data sheet.

- JESD615-A, *Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices*
- IEC-101/61340-5, *Specification for the Protection of Electronic Devices from Electrostatic Phenomena*

10.2 Handling Moisture-Sensitive SMD Devices

DFN/QFNs are moisture/reflow-sensitive Surface Mount Devices (SMD) and proper precautions are required for handling, packing, shipping and use. Moisture from atmospheric humidity enters permeable packaging materials by diffusion. Assembly processes (which are used to solder SMD packages to PCBs) expose the entire package body to temperatures higher than 200°C. As noted in section “**Moisture Sensitivity Level**”, on page 26, during solder reflow the combination of rapid moisture expansion, materials mismatch, and material interface degradation can result in package cracking and/or delamination of critical interfaces within the package. Cracking and/or delamination can lead to failure and reliability problems, and proper handling of SMDs should be considered.

Dried moisture-sensitive SMDs are placed in tray or tape-and-reel, and dry packed for proper transportation and storage. SMDs are sealed with a desiccant material and a Humidity Indicator Card inside of a Moisture Barrier Bag (MBB). The shelf life of dry-packed SMDs are 12 months from the dry pack seal date (when stored in $\leq 40^{\circ}\text{C}/90\%\text{RH}$ environment).

Proper use and storage of moisture-sensitive SMDs are required after a MBB is opened. Improper use and storage will increase various quality and reliability risks. SMDs *that will be subjected to reflow solder or other high temperature process* must be mounted within the period of floor environment specified by MSL, or stored per the J-STD-033B standard.

The baking of SMDs is required before mounting if any of following events occur:

- SMDs are exposed to a specified floor environment greater than specified period.
- The Humidity Indicator Card shows $>10\%$ for level 2a – 5a, or shows $>60\%$ for level 2 devices when read at $23 \pm 5^{\circ}\text{C}$ environment.
- SMDs are not stored according to the J-STD-033B standard.

The baking procedure, and more detailed requirements and procedures of handling moisture-sensitive SMDs can be found in:

- IPC/JEDEC J-STD-033B, *Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices*

10.3 Packing of Devices

DFN/QFN devices are contained in Tray or Tape-and-Reel configurations; both Trays and Tape-and-Reel are dry packed for transportation and storage. Packing media are design to protect devices from electrical, mechanical and chemical damages (as well as moisture absorption), but proper handling and storage of dry packs are recommended. Improper handling and storage (dropping dry packs, storage exceeding 40°C/90%RH environment, excessive stacking of dry packs, etc.) will increase various quality and reliability risks.

- Tray
 - Freescale complies with standard JEDEC tray design configuration – See [Figure 35](#).
 - Pin 1 of devices will be oriented with lead 1 toward the chamfered corner of the tray.
 - Trays are designed to be baked for moisture-sensitive SMDs, but the temperature rating of tray should NOT be exceeded when the devices are baked. The temperature rating can be found on the end-tab of the tray. The recommended baking temperature of trays is 125°C.
 - Trays are typically banded together with 5+1 (5 fully loaded trays and 1 cover tray) stacking, and dry packed in a Moisture Barrier Bag (MBB). Partial stacking (1+1, 2+1, etc.) is also available, depending on individual requirements.

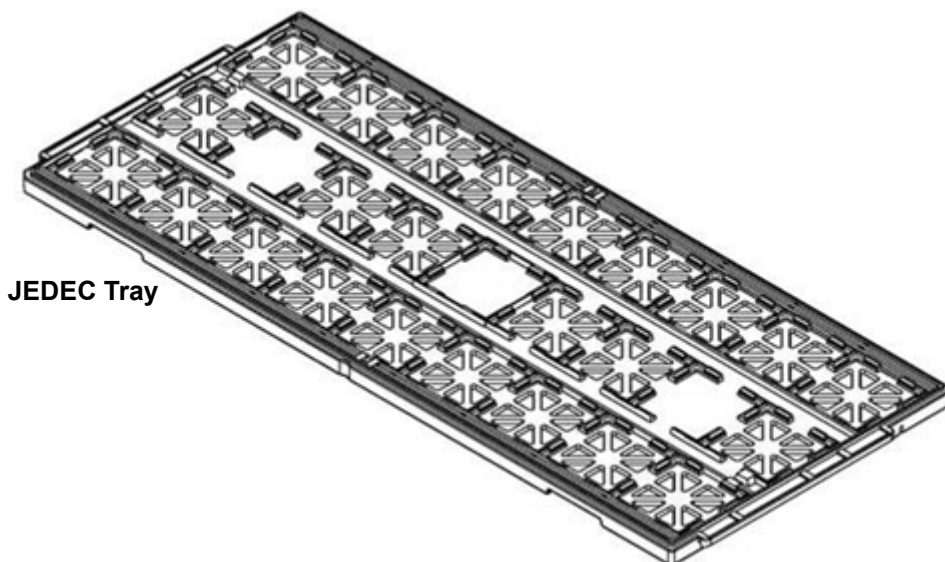


Figure 35. JEDEC Tray Example

- Tape-and-Reel
 - Freescale complies with EIA-481D for carrier Tape-and-Reel configuration. See [Figure 36](#).
 - Freescale complies to Pin 1 orientation of devices with EIA-481D.
 - Tape-and-Reels are NOT designed to be baked at high temperatures.
 - Each Tape-and-Reel is typically dry packed in a Moisture Barrier Bag.

CARRIER TAPE SPECIFICATIONS

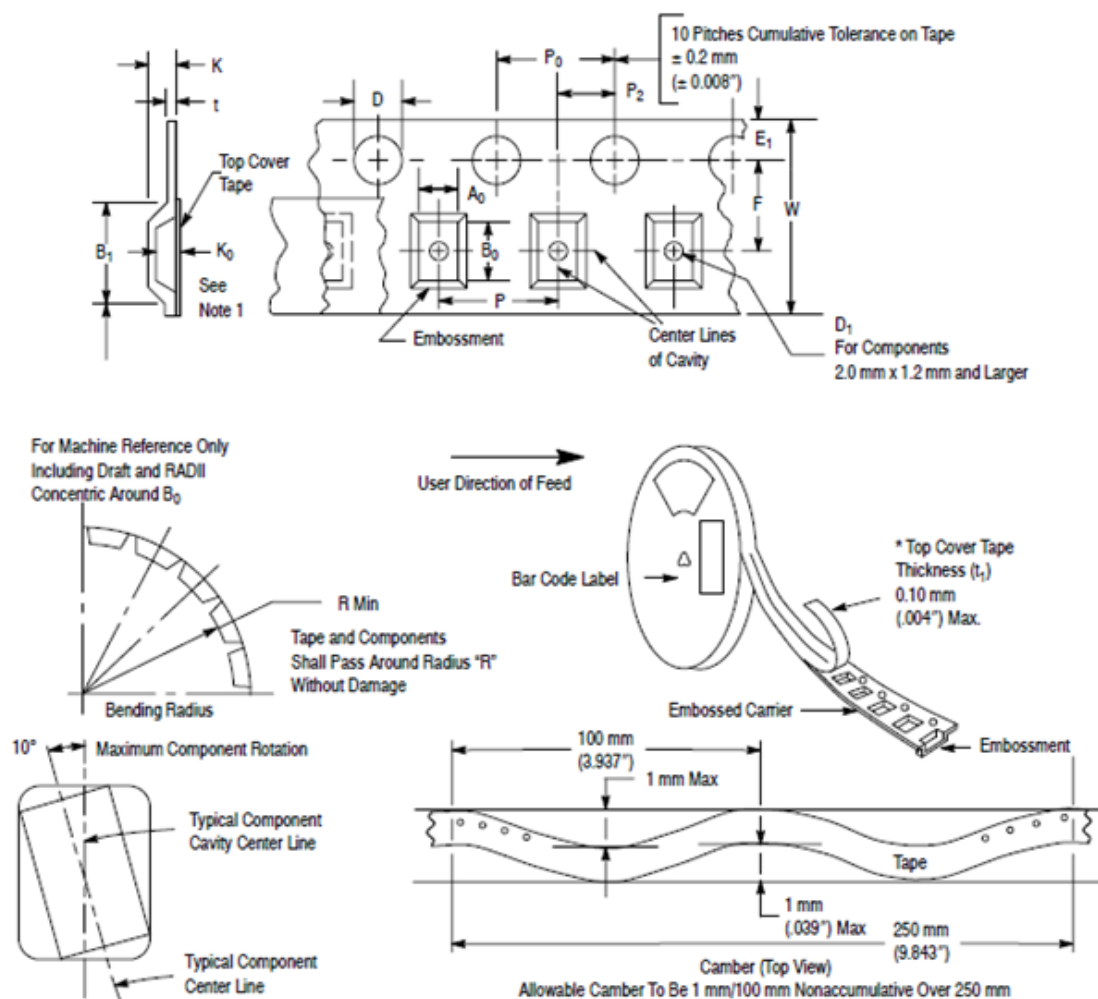


Figure 36. Tape-and-Reel Example

- Dry Packing
 - Trays and Tape-and-Reels (loaded with devices) are sealed in a Moisture Barrier Bag, which are labeled and packed in dedicated boxes with dunnage (packing materials) for the final shipment.
 - Each dry pack bag contains a desiccant pouch and a Humidity Indicator Card.
 - Freescale encourages the recycling and reuse of materials whenever possible.
 - Freescale will not use packing media items processed with or containing class 1 ozone-depleting substances.
 - Whenever possible, Freescale shall design its packing configurations to optimize volumetric efficiency and package density, to minimize the amount of packing (dunnage) and packaging that enters the industrial waste stream.
 - Freescale shall comply with following Environmental Standards Conformance guidelines / directives:
 - ISPM 15, *Guidelines for Regulating Wood Packaging Material in International Trade*
 - European Parliament and Council Directive 94/62/EC of 20 December 1994, packaging and packaging waste.

11 References

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- [4] EIA-783, *Guideline Orientation Standard for Multi-Connection Package (Design Rules for Tape and Reel Orientation)*, November 1998.
- [5] EIA/JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)*, December 1995.
- [6] EIA/JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*, August 1996.
- [7] EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*, February 1999.
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- [13] MIL SPEC-883, *Method 1012.1 Thermal Characteristics*, February 2006
- [14] IPC-7351B, *Generic Requirements for Surface Mount Design and Land Pattern Standards*, June 2010.
- [15] IPC-7093, *Design and Assembly Process Implementation for Bottom Termination SMT Components*, March 2011
- [16] EIA-481, *Standards Excerpts used to assure complete alignment*

12 Revision History

Revision	Date	Description
4.0	9/2008	• Initial release
5.0	11/2013	• Complete document update

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Document Number: AN1902
Rev. 5.0
11/2013

