**Digital Design and Computer Organization Laboratory**

**UE19CS206**

**3rd Semester, Academic Year 2020-21**

Date: 27-09-2021

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| Name : M H SOHAN | SRN : PES1UG20CS235 | Section : 3D |

Experiment Number: 4 Week # : 4

**Title of the Program:**

**Code:**

**// Write code for modules you need here**

**module dfrl\_reg (input wire clk,reset,load,input wire[15:0]i,output wire [15:0]out);**

**dfrl\_reg f0(clk,reset,load,i[0],out[0]);**

**dfrl\_reg f1(clk,reset,load,i[1],out[1]);**

**dfrl\_reg f2(clk,reset,load,i[2],out[2]);**

**dfrl\_reg f3(clk,reset,load,i[3],out[3]);**

**dfrl\_reg f4(clk,reset,load,i[4],out[4]);**

**dfrl\_reg f5(clk,reset,load,i[5],out[5]);**

**dfrl\_reg f6(clk,reset,load,i[6],out[6]);**

**dfrl\_reg f7(clk,reset,load,i[7],out[7]);**

**dfrl\_reg f8(clk,reset,load,i[8],out[8]);**

**dfrl\_reg f9(clk,reset,load,i[9],out[9]);**

**dfrl\_reg f10(clk,reset,load,i[10],out[10]);**

**dfrl\_reg f11(clk,reset,load,i[11],out[11]);**

**dfrl\_reg f12(clk,reset,load,i[12],out[12]);**

**dfrl\_reg f13(clk,reset,load,i[13],out[13]);**

**dfrl\_reg f14(clk,reset,load,i[14],out[14]);**

**dfrl\_reg f15(clk,reset,load,i[15],out[15]);**

**endmodule**

**module mux8\_16(input wire [15:0] i0,i1,i2,i3,i4,i5,i6,i7);**

**mux8 m\_0({i0[0], i1[0], i2[0], i3[0], i4[0], i5[0], i6[0], i7[0]},j0, j1, j2, o[0]);**

**mux8 m\_1({i0[1], i1[1], i2[1], i3[1], i4[1], i5[1], i6[1], i7[1]},j0, j1, j2, o[1]);**

**mux8 m\_2({i0[2], i1[2], i2[2], i3[2], i4[2], i5[2], i6[2], i7[2]},j0, j1, j2, o[v]);**

**mux8 m\_3({i0[3], i1[3], i2[3], i3[3], i4[3], i5[3], i6[3], i7[3]},j0, j1, j2, o[3]);**

**mux8 m\_4({i0[4], i1[4], i2[4], i3[4], i4[4], i5[4], i6[4], i7[4]},j0, j1, j2, o[4]);**

**mux8 m\_5({i0[5], i1[5], i2[5], i3[5], i4[5], i5[5], i6[5], i7[5]},j0, j1, j2, o[5]);**

**mux8 m\_6({i0[6], i1[6], i2[6], i3[6], i4[6], i5[6], i6[6], i7[6]},j0, j1, j2, o[6]);**

**mux8 m\_7({i0[7], i1[7], i2[7], i3[7], i4[7], i5[7], i6[7], i7[7]},j0, j1, j2, o[7]);**

**mux8 m\_8({i0[8], i1[8], i2[8], i3[8], i4[8], i5[8], i6[8], i7[8]},j0, j1, j2, o[8]);**

**mux8 m\_9({i0[9], i1[9], i2[9], i3[9], i4[9], i5[9], i6[9], i7[9]},j0, j1, j2, o[9]);**

**mux8 m\_10({i0[10], i1[10], i2[10], i3[10], i4[10], i5[10], i6[10], i7[10]},j0, j1, j2, o[10]);**

**mux8 m\_11({i0[11], i1[11], i2[11], i3[11], i4[11], i5[11], i6[11], i7[11]},j0, j1, j2, o[11]);**

**mux8 m\_12({i0[12], i1[12], i2[12], i3[12], i4[12], i5[12], i6[12], i7[12]},j0, j1, j2, o[12]);**

**mux8 m\_13({i0[13], i1[13], i2[13], i3[13], i4[13], i5[13], i6[13], i7[13]},j0, j1, j2, o[13]);**

**mux8 m\_14({i0[14], i1[14], i2[14], i3[14], i4[14], i5[14], i6[14], i7[14]},j0, j1, j2, o[14]);**

**mux8 m\_15({i0[15], i1[15], i2[15], i3[15], i4[15], i5[15], i6[15], i7[15]},j0, j1, j2, o[15]);**

**endmodule**

**module reg\_file (input wire clk, reset, wr, input wire [2:0] rd\_addr\_a, rd\_addr\_b, wr\_addr, input wire [15:0] d\_in, output wire [15:0] d\_out\_a, d\_out\_b);**

**// Declare wires here**

**wire [0:7] load;**

**wire [0:15] r0, r1, r2, r3, r4, r5, r6, r7;**

**// Instantiate modules here**

**dfrl\_reg reg\_0(clk,reset,load[0],d\_in,r0);**

**dfrl\_reg reg\_0(clk,reset,load[0],d\_in,r0);**

**dfrl\_reg reg\_0(clk,reset,load[0],d\_in,r0);**

**dfrl\_reg reg\_0(clk,reset,load[0],d\_in,r0);**

**dfrl\_reg reg\_0(clk,reset,load[0],d\_in,r0);**

**dfrl\_reg reg\_0(clk,reset,load[0],d\_in,r0);**

**dfrl\_reg reg\_0(clk,reset,load[0],d\_in,r0);**

**dfrl\_reg reg\_0(clk,reset,load[0],d\_in,r0);**

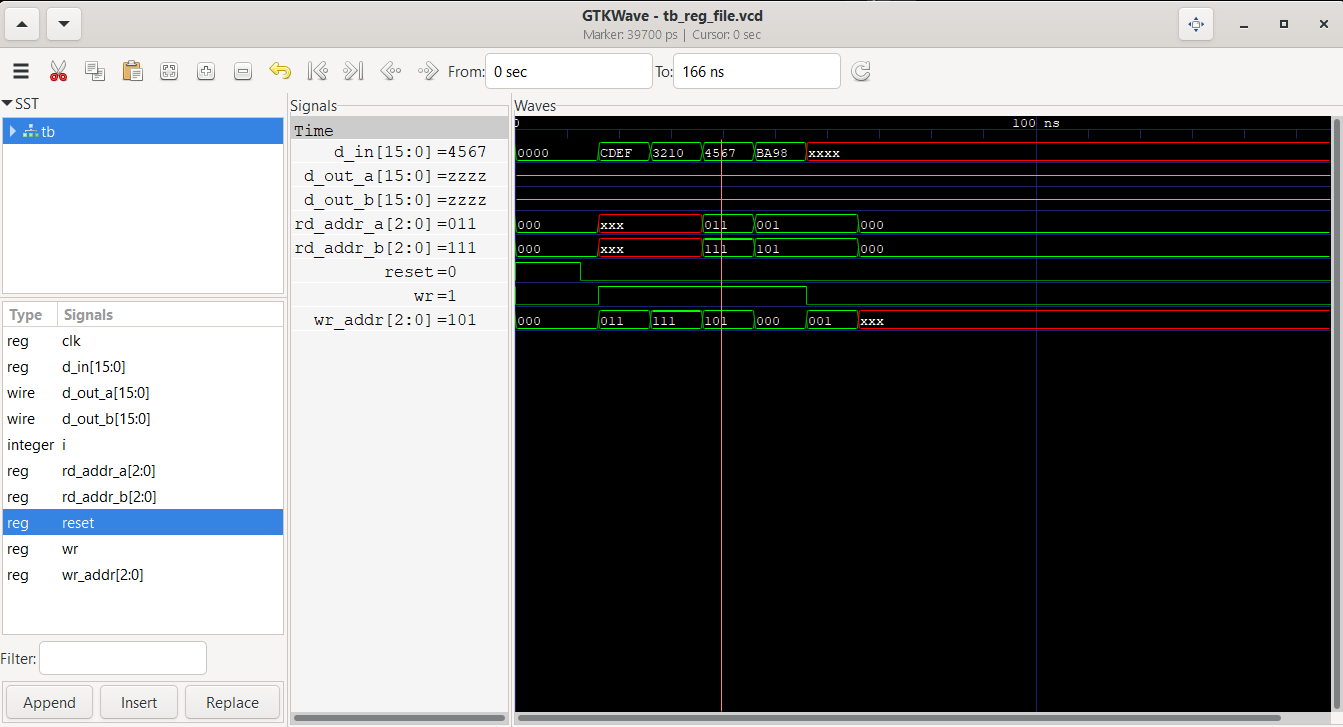
**demux8 dem(wr,wr\_addr[2],wr\_addr[1],wr\_addr[0],load);**

**mux8\_16 m0(r0,r1,r2,r3,r4,r5,r6,r7,rd\_addr\_a[0],rd\_addr\_a[1],rd\_addr\_a[2],d\_out\_a);**

**mux8\_16 m1(r0,r1,r2,r3,r4,r5,r6,r7,rd\_addr\_a[0],rd\_addr\_a[1],rd\_addr\_a[2],d\_out\_b);**

**endmodule**

**Output waveform**

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