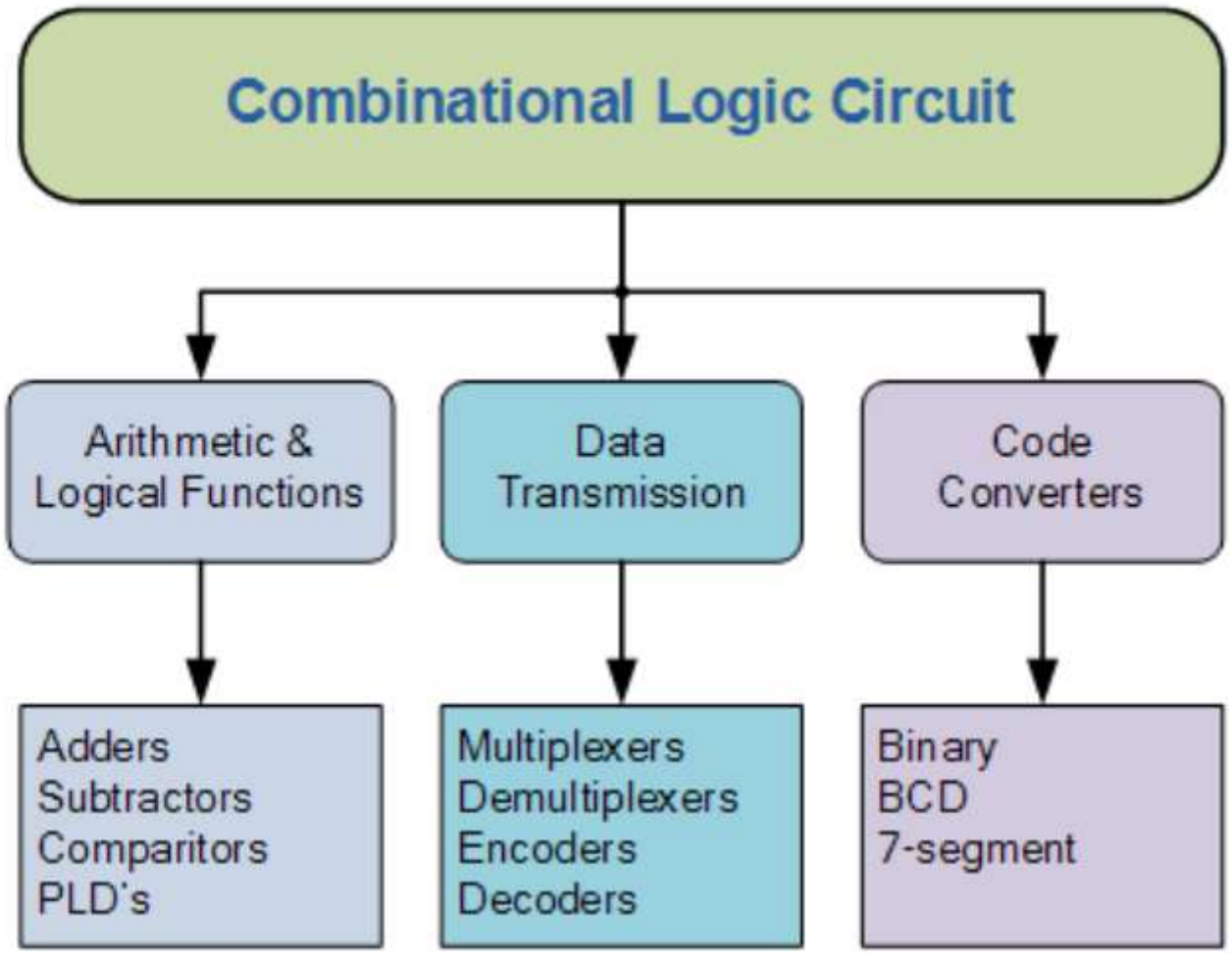
Outline

- Design Combinational Logic Circuit for scenario
- Adder
- Subtractor
- Comparator
- Multiplexer
- Demultiplexer
- Encoder
- Decoder
- Code Conversions
- Implementation

Application of CLC



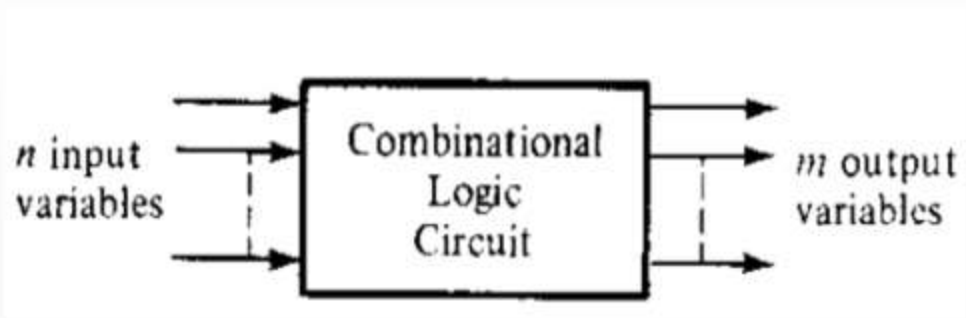
Introduction

LOGIC CIRCUITS:
1. Combinational
2. Sequential

Combinational Logic Circuits (Circuits without a memory): In this type of logic circuits outputs depend only on the current inputs.

Sequential Logic Circuits (Circuits with memory): In this type of logic circuits outputs depend on the current inputs and previous inputs. These circuits employ storage elements and logic gates.

Combinational Logic Circuits



- A combinational circuit consists of input variables (n), logic gates, and output variables (m).
- For (n) input variables there are 2^n possible combinations of binary input values.
- For each possible input combination there is one and only one possible output combination, a combinational circuit can be describe by (m) Boolean functions one for each output variable.
- Each output function expressed in terms of the (n) input variables.

Adders

- Digital computers perform a variety of information processing tasks. Among the basic functions encountered are the various *arithmetic operations (addition)*.

Binary Arithmetic

1. Addition: The rules of addition are:

$0 + 0 = 0$

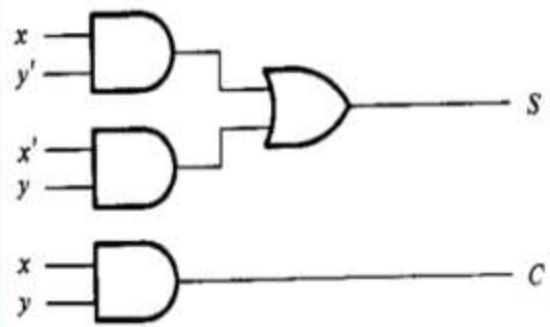
$0 + 1 = 1$

$1 + 0 = 1$

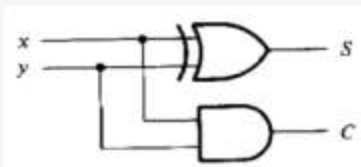
$1 + 1 = 10$

$1 + 1 + 1 = 11$

The block diagram for the half adder is:



(a) $S = xy' + x'y$
$C = xy$



(b) $S = x \oplus y$
$C = xy$

Binary Adder -Full Adder

Q/Design a combinational logic circuit that performs arithmetic operation for adding three bits?

Answer: n=3bit , $n=2^3=8$

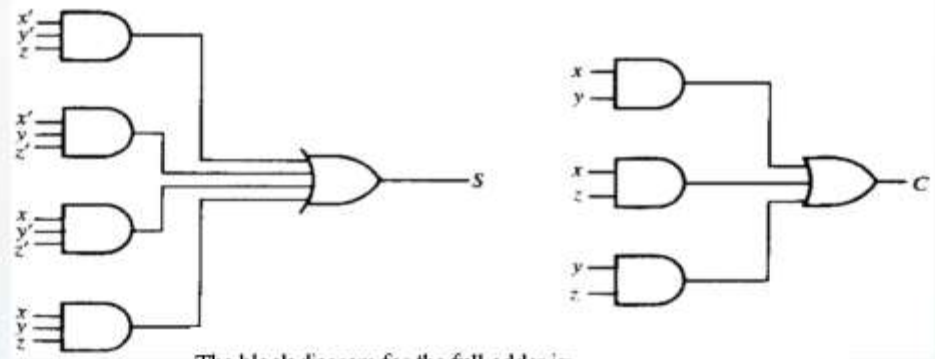
Inputs			Outputs	
X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

X \ YZ	00	01	11	10
0		1		1
1	1		1	

$S = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XYZ$

X \ YZ	00	01	11	10
0			1	
1		1	1	1

$C = XY + XZ + YZ$



The block diagram for the full adder is:

Subtractor

- Digital computers perform a variety of information processing tasks. Among the basic functions encountered are the various *arithmetic operations (Subtraction)*.

Binary Arithmetic

2. Subtraction: The rules of subtractions are:

$0 - 0 = 0$
$1 - 0 = 1$
$10 - 1 = 1$
$1 - 1 = 0$

Binary Subtractor- Half Subtractor

Q/Design a combinational logic circuit that performs arithmetic operation for subtracting two bits?

Answer: n= 2bit , $n=2^2=4$

0 – 0 =0

1 – 0 =1

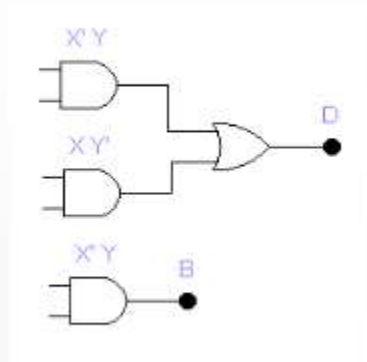
1 – 1 =0

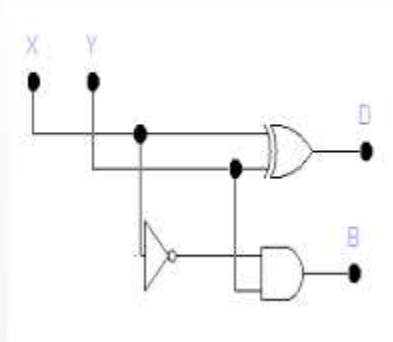
0 – 1 = 10 – 1 = 1 (The 1 borrowed from the next higher stage)

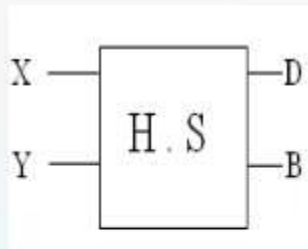
Inputs		Outputs	
X	Y	B	D
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

$D = \bar{X}Y + X\bar{Y} = X \oplus Y$

$B = \bar{X}Y$


X'Y
XY'
X'Y
D
B


X
Y
D
B

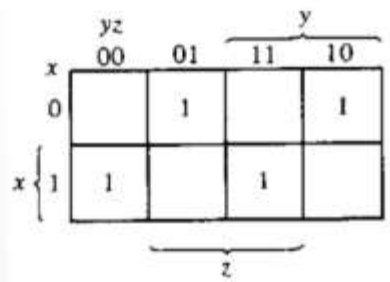

X
Y
H.S
D
B

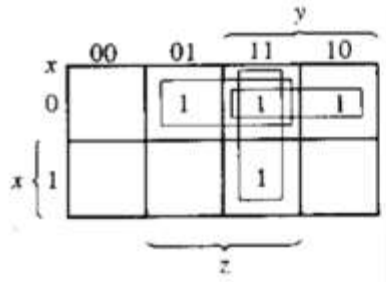
Binary Subtractor – Full Subtractor

Q/Design a combinational logic circuit that performs arithmetic operation for subtracting three bits?

Answer: n=3bits , $n=2^3=8$

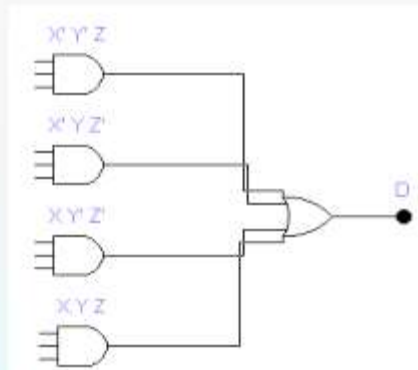
Inputs			Outputs	
X	Y	Z	B	D
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

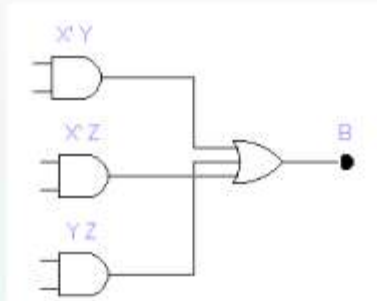




$D = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XYZ$

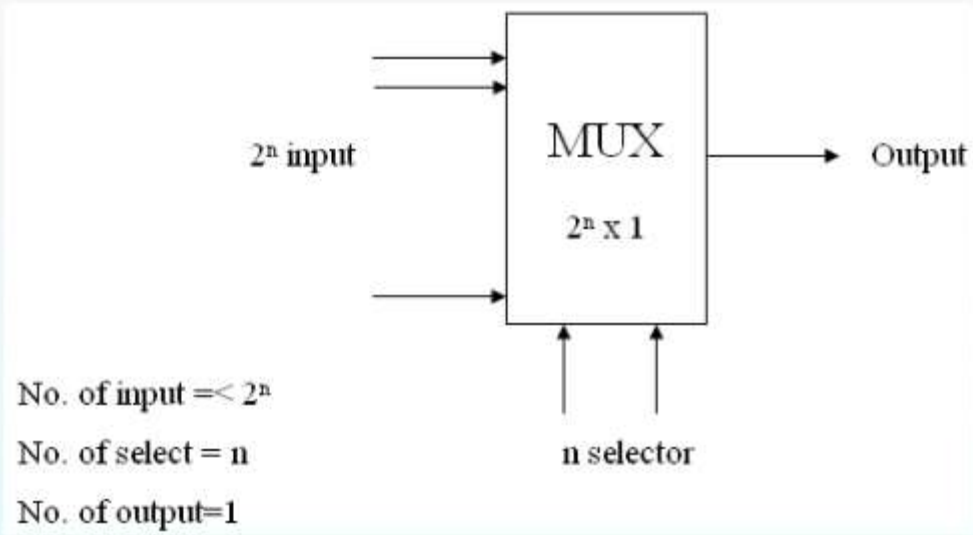
$B = \bar{X}Y + \bar{X}Z + YZ$





Multiplexer (Data Selector)

Multiplexing means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is CLC that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by of a selection lines.



No. of input =< 2^n

No. of select = n

No. of output=1

Design MUX:

AND gates used to represent inputs.

One **OR** gate only used to collect inputs.

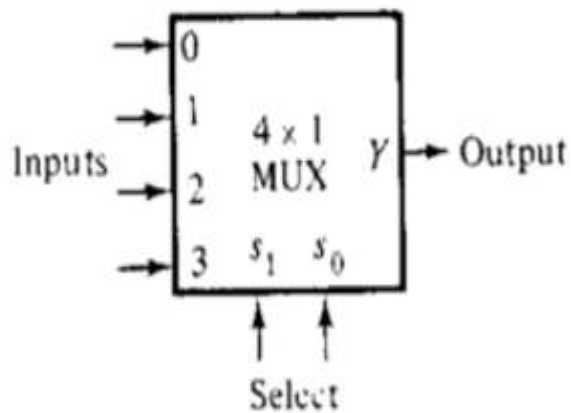
NOT gates as a selector to connect inputs to output.

Example: Design 4 x 1 multiplexer?

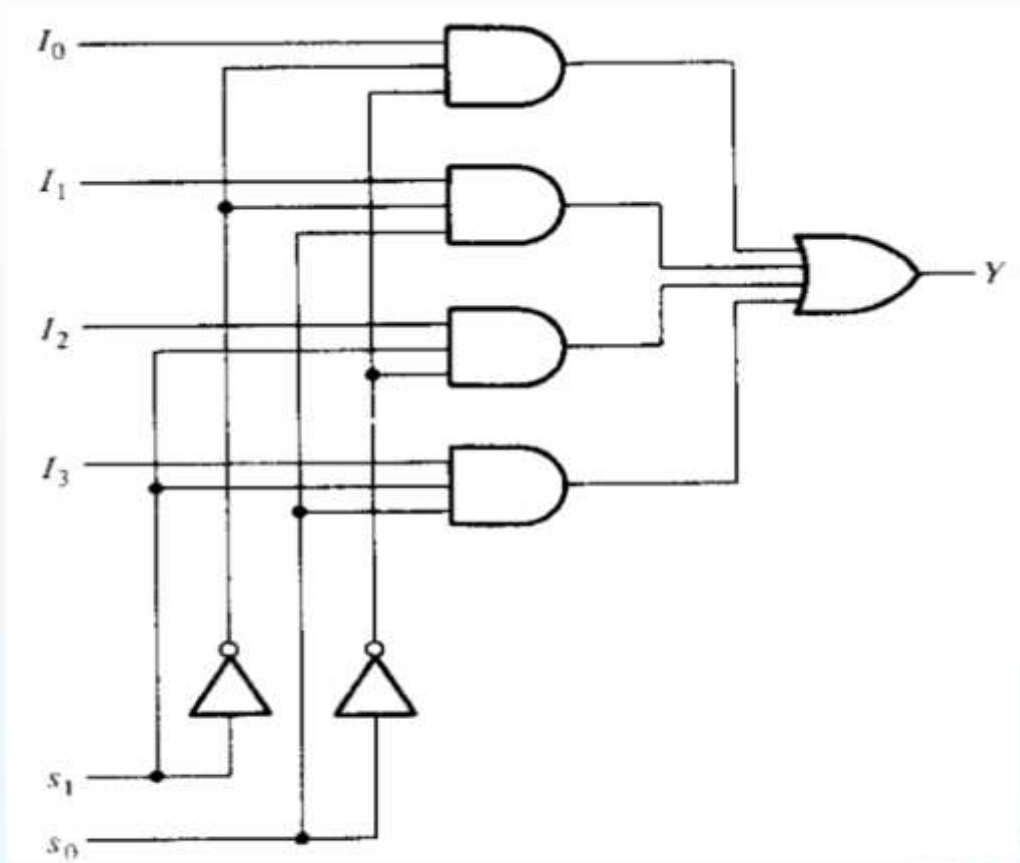
Solution: No. of inputs = $4 = 2^2$, No. of select=2, No. of output=1

Select		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Truth Table



Block diagram



4x1 Multiplexer Logic Diagram