Shift Registers

Contents:

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Shift Register

A register is a digital circuit with two basic functions

- Data storage
- Data shifting or data transfer or data movement

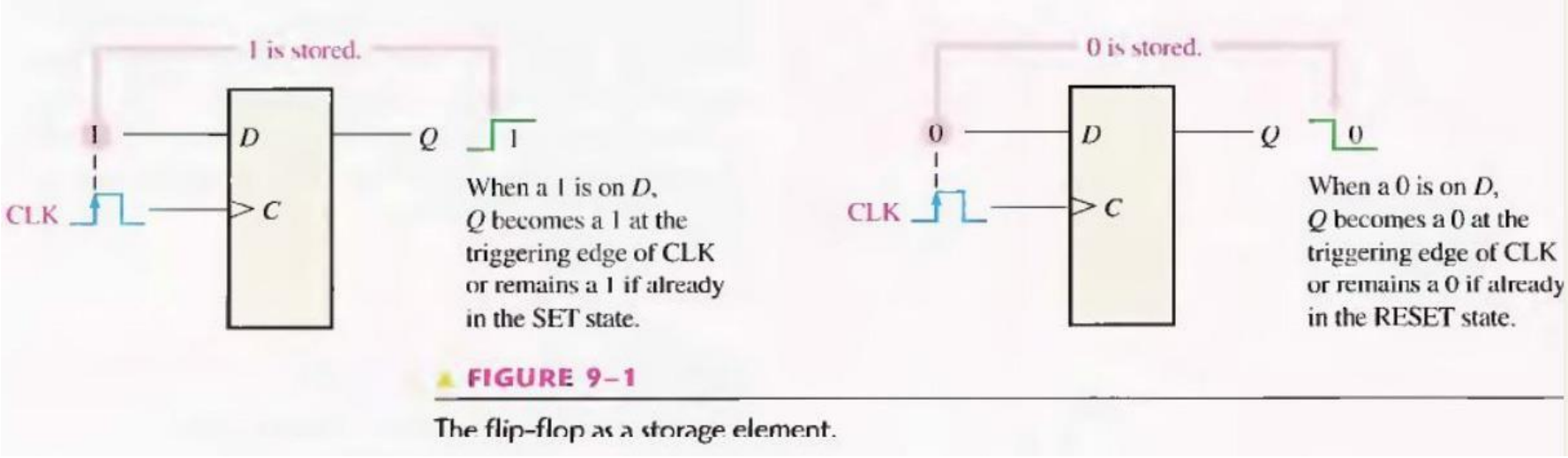
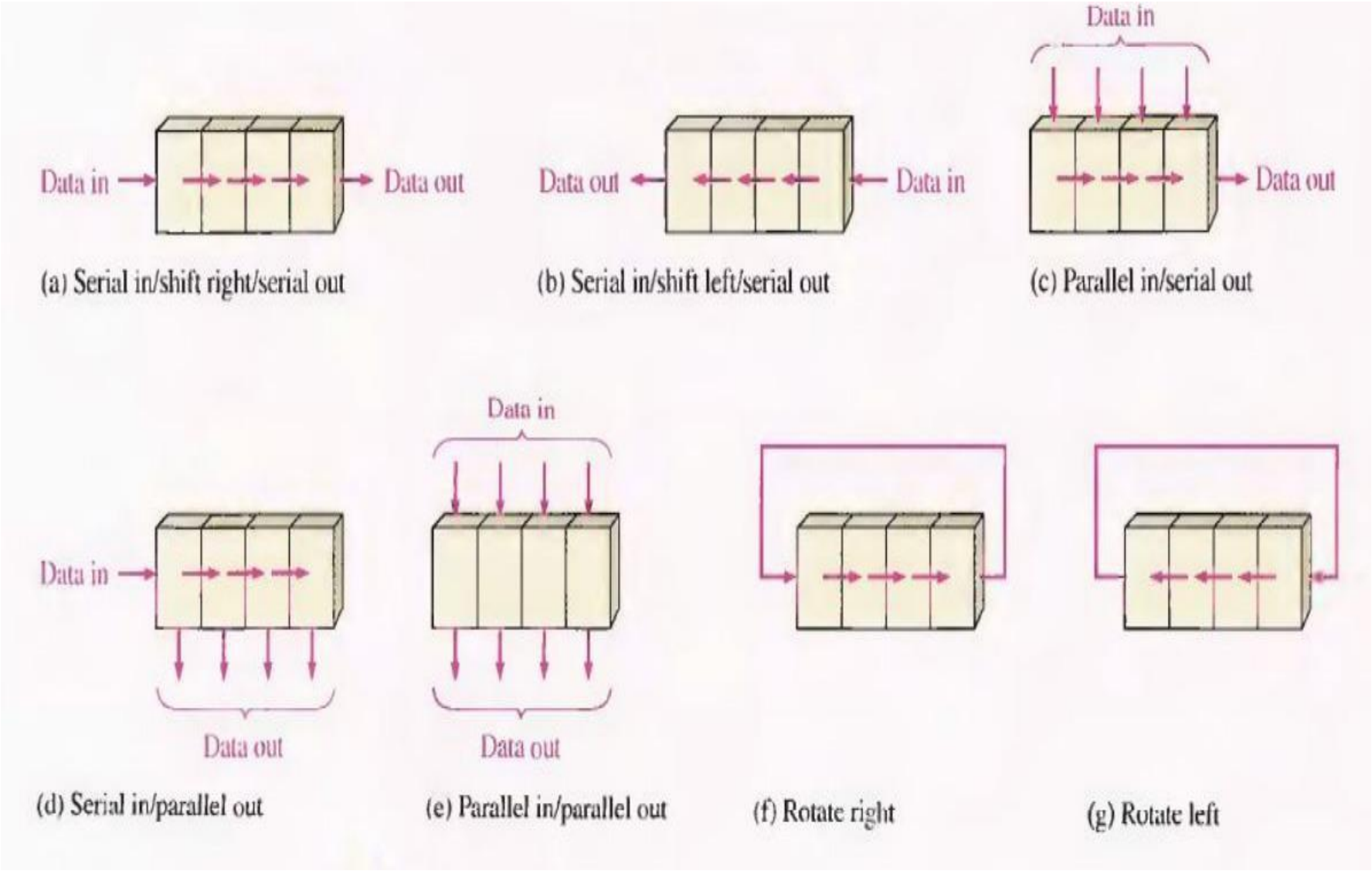


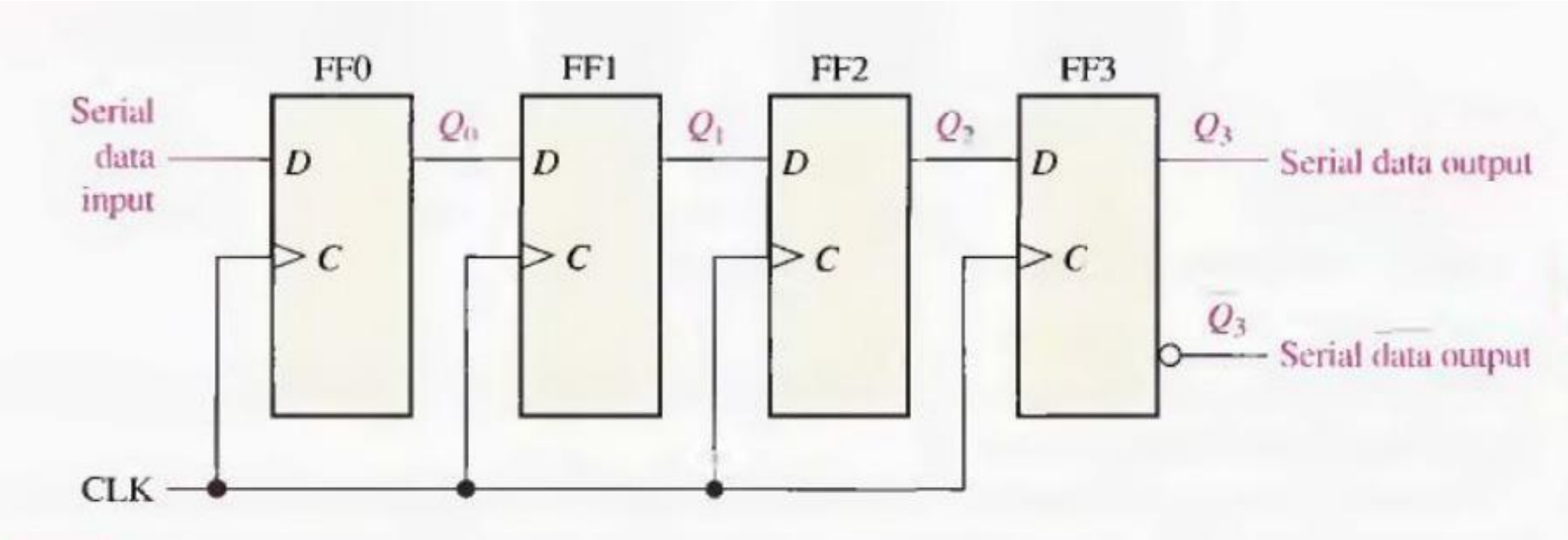
FIGURE 9–1

The flip-flop as a storage element.

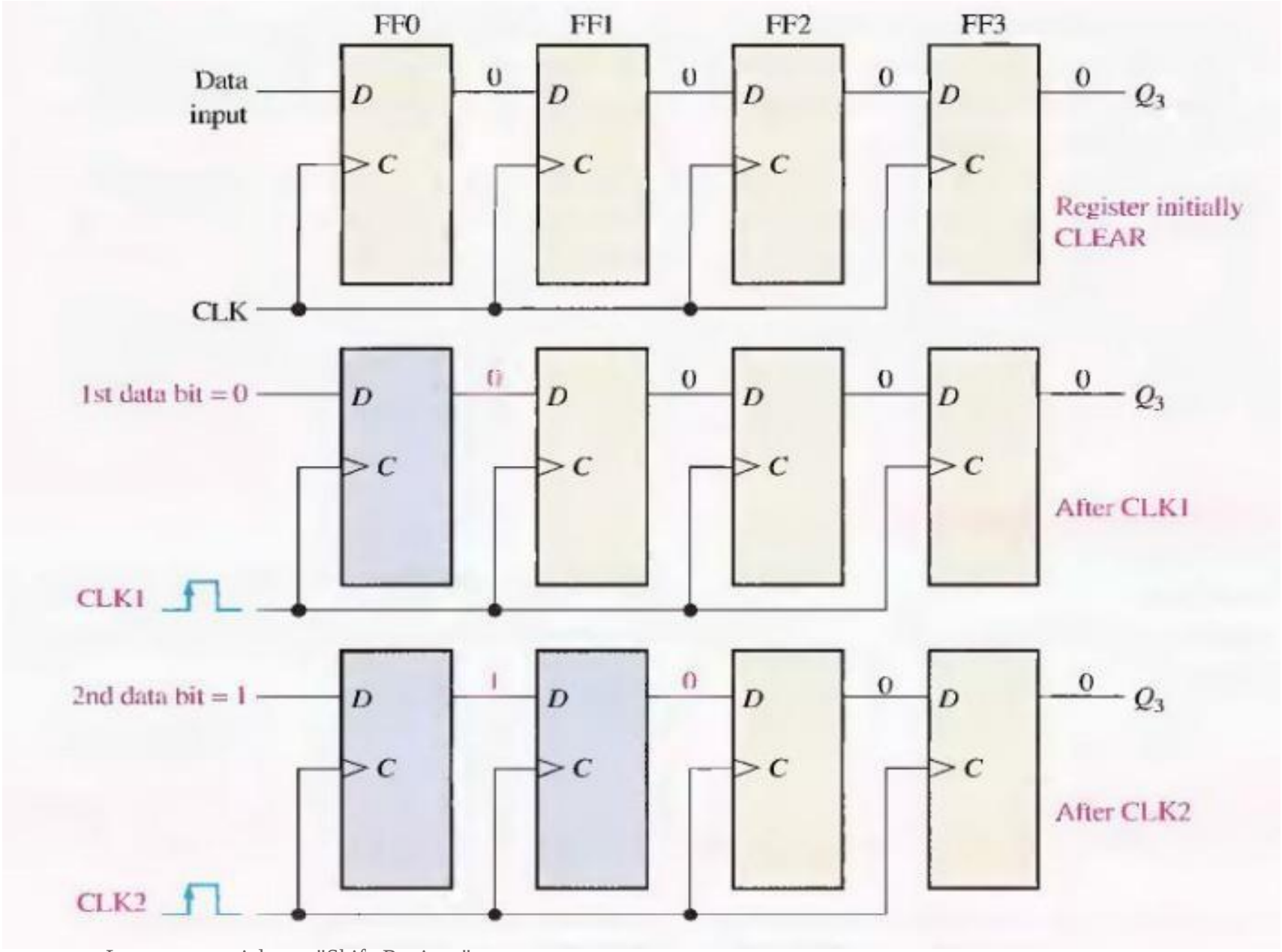
Data Shifting



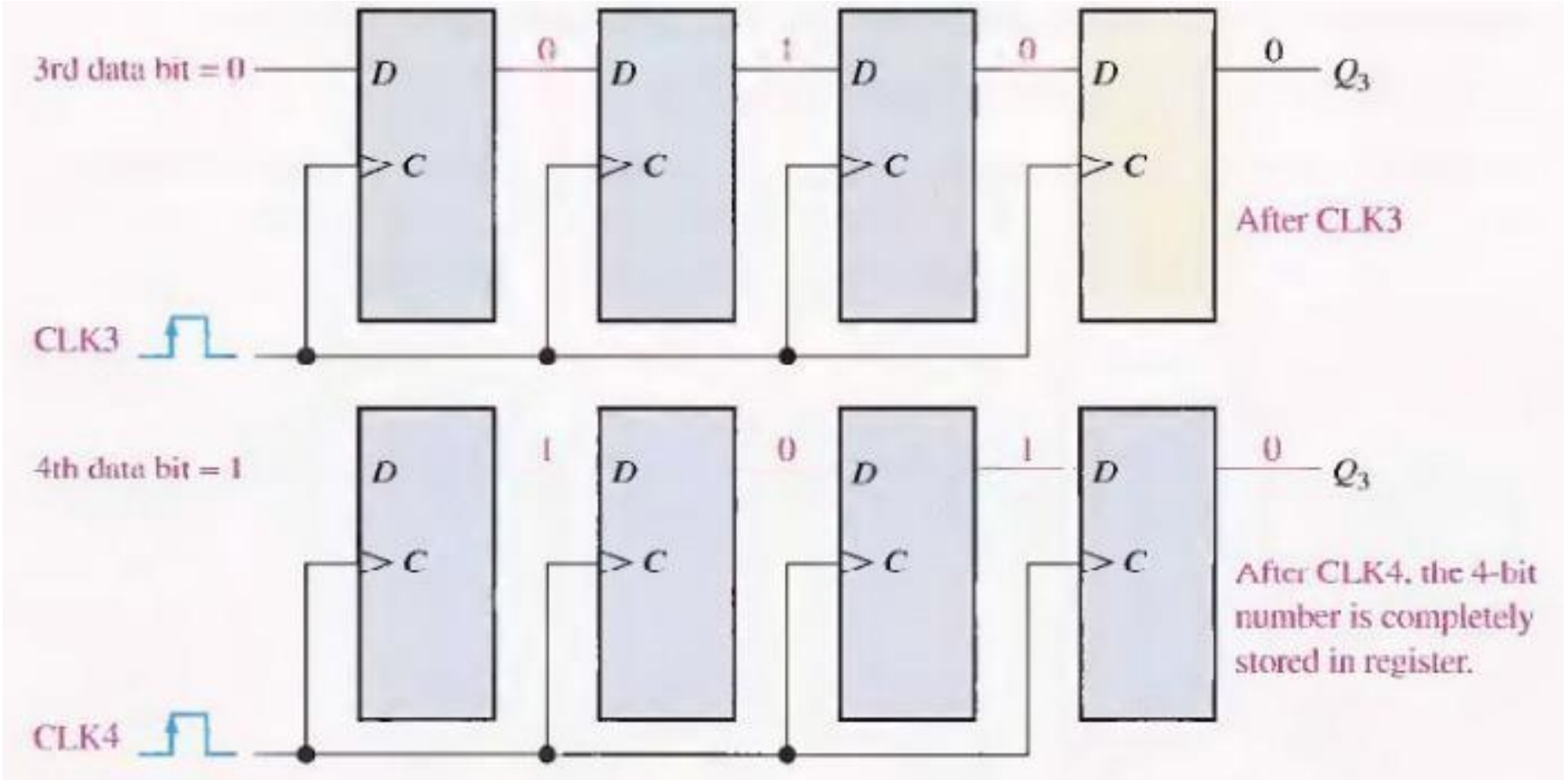
Serial In/ Serial Out Shift Registers



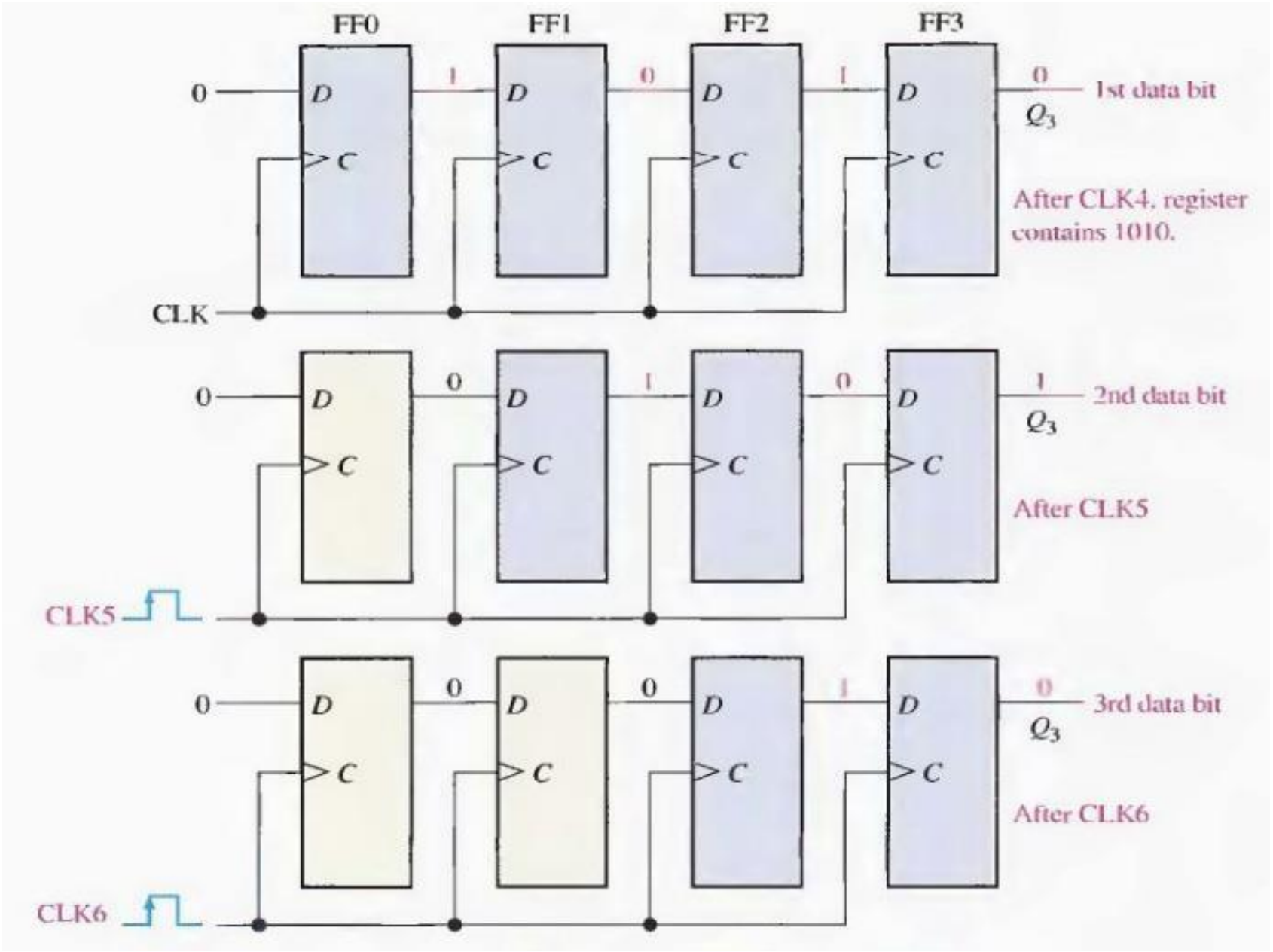
Serial In


FF0
FF1
FF2
FF3
Data input
D
C
0
Q_3
CLK
Register initially CLEAR
1st data bit = 0
After CLK1
CLK1
2nd data bit = 1
1
After CLK2
CLK2

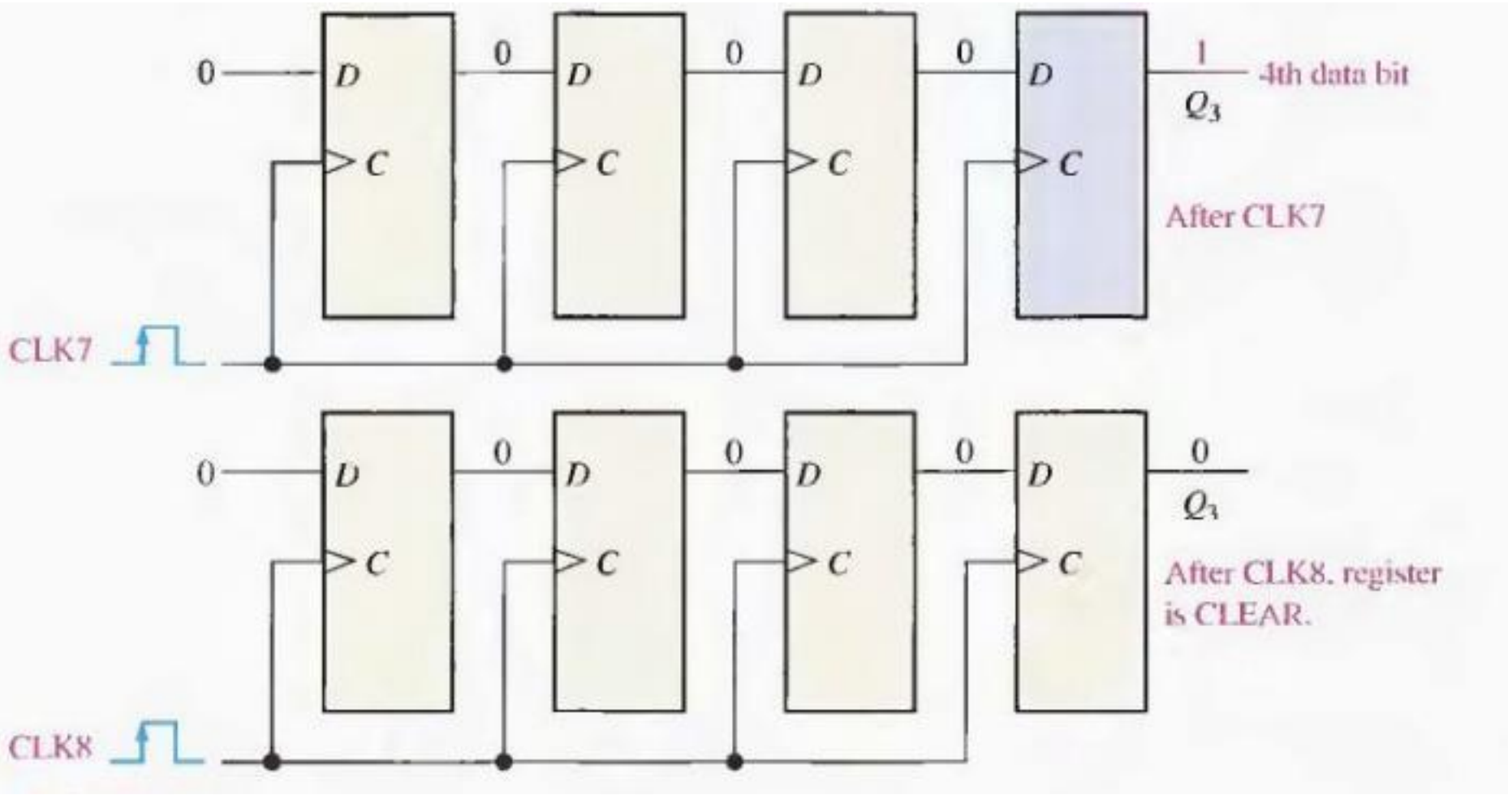
Serial In


3rd data bit = 0
D
C
0
1
0
0
Q_3
After CLK3
CLK3
4th data bit = 1
1
0
1
0
Q_3
After CLK4, the 4-bit number is completely stored in register.
CLK4

Serial Out

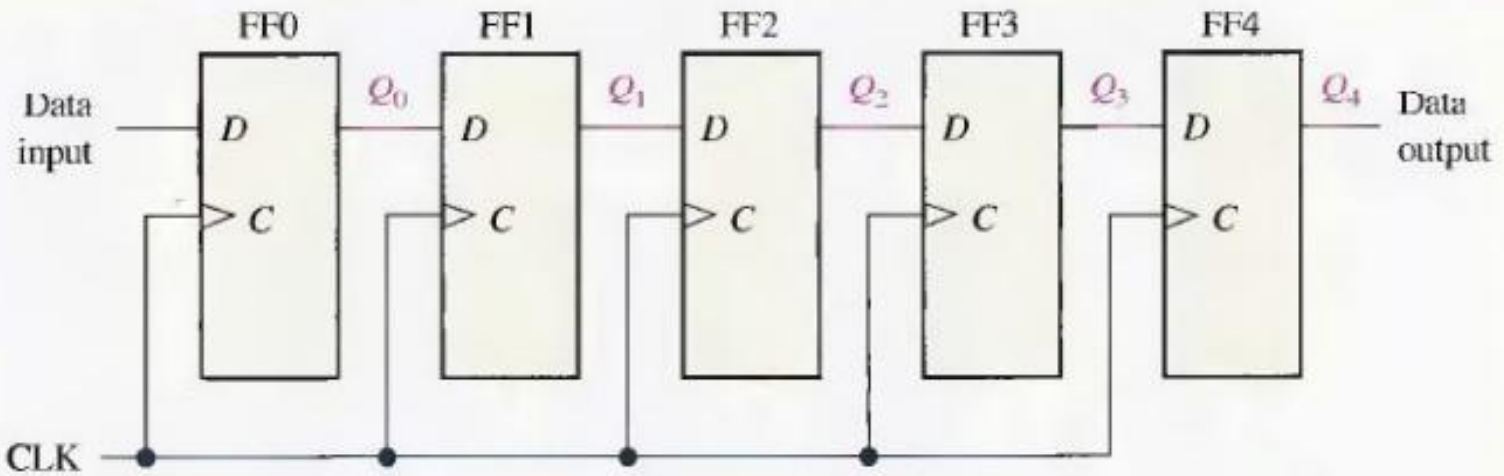

FF0
FF1
FF2
FF3
0
D
C
1
0
1
0
Q_3
1st data bit
After CLK4, register contains 1010.
CLK
0
D
C
0
1
0
1
Q_3
2nd data bit
After CLK5
CLK5
0
D
C
0
0
1
0
Q_3
3rd data bit
After CLK6
CLK6

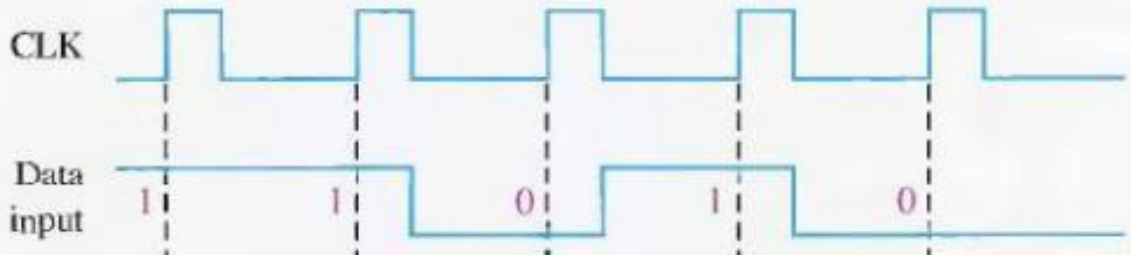
Serial Out

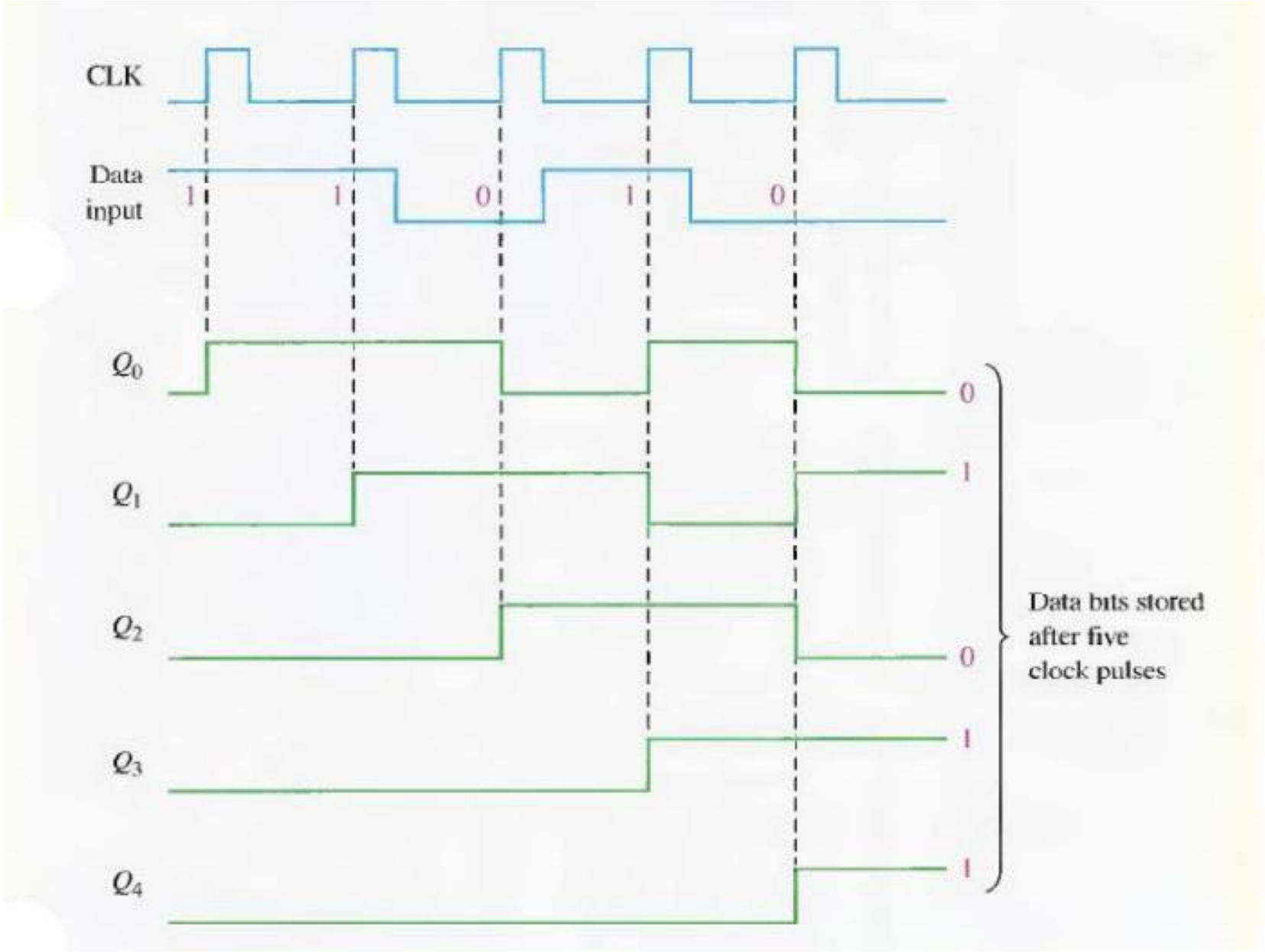

0
D
C
0
D
C
0
D
C
0
D
C
1
Q_3
4th data bit
After CLK7
CLK7
0
D
C
0
D
C
0
D
C
0
D
C
0
Q_3
After CLK8. register is CLEAR.
CLK8

Example 9-1

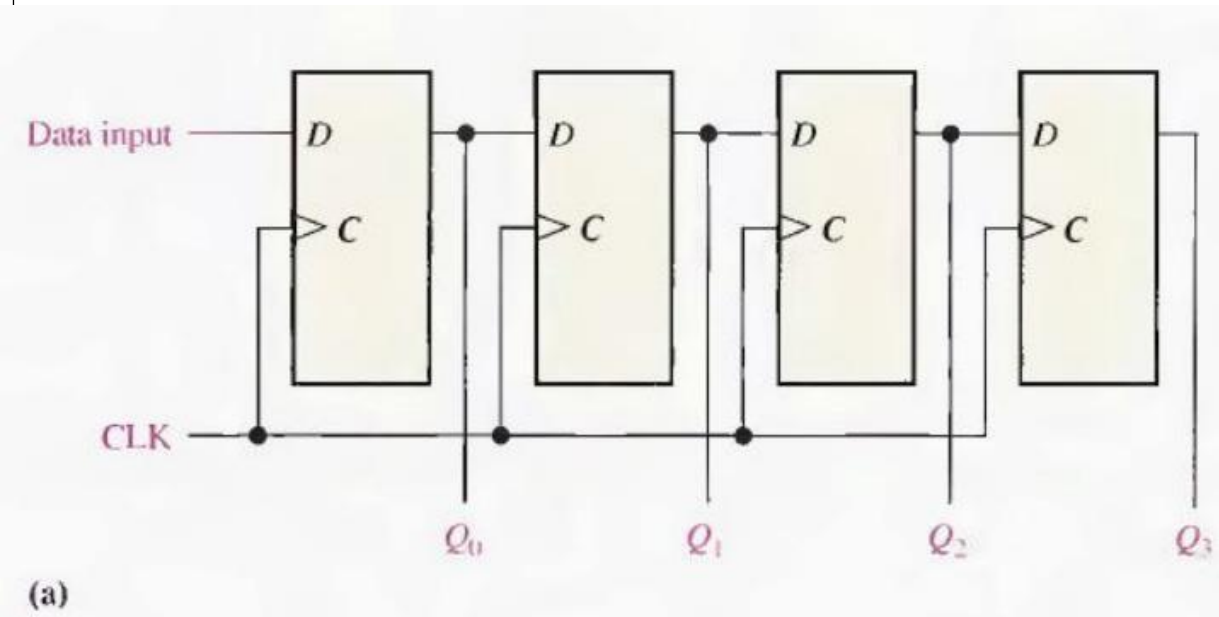
Show the states of the 5-bit register in Figure 9–6(a) for the specified data input and clock waveforms. Assume that the register is initially cleared (all 0s).

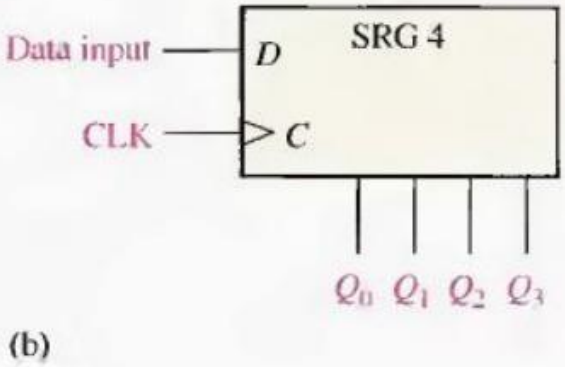





CLK
Data input
1
1
0
1
0
Q_0
Q_1
Q_2
Q_3
Q_4
0
1
0
1
1
Data bits stored after five clock pulses

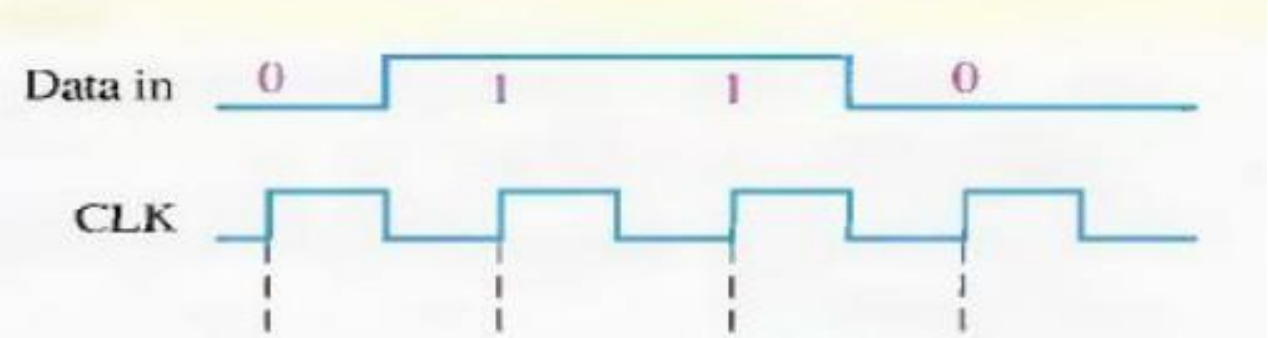
Serial In/Parallel out Shift Register

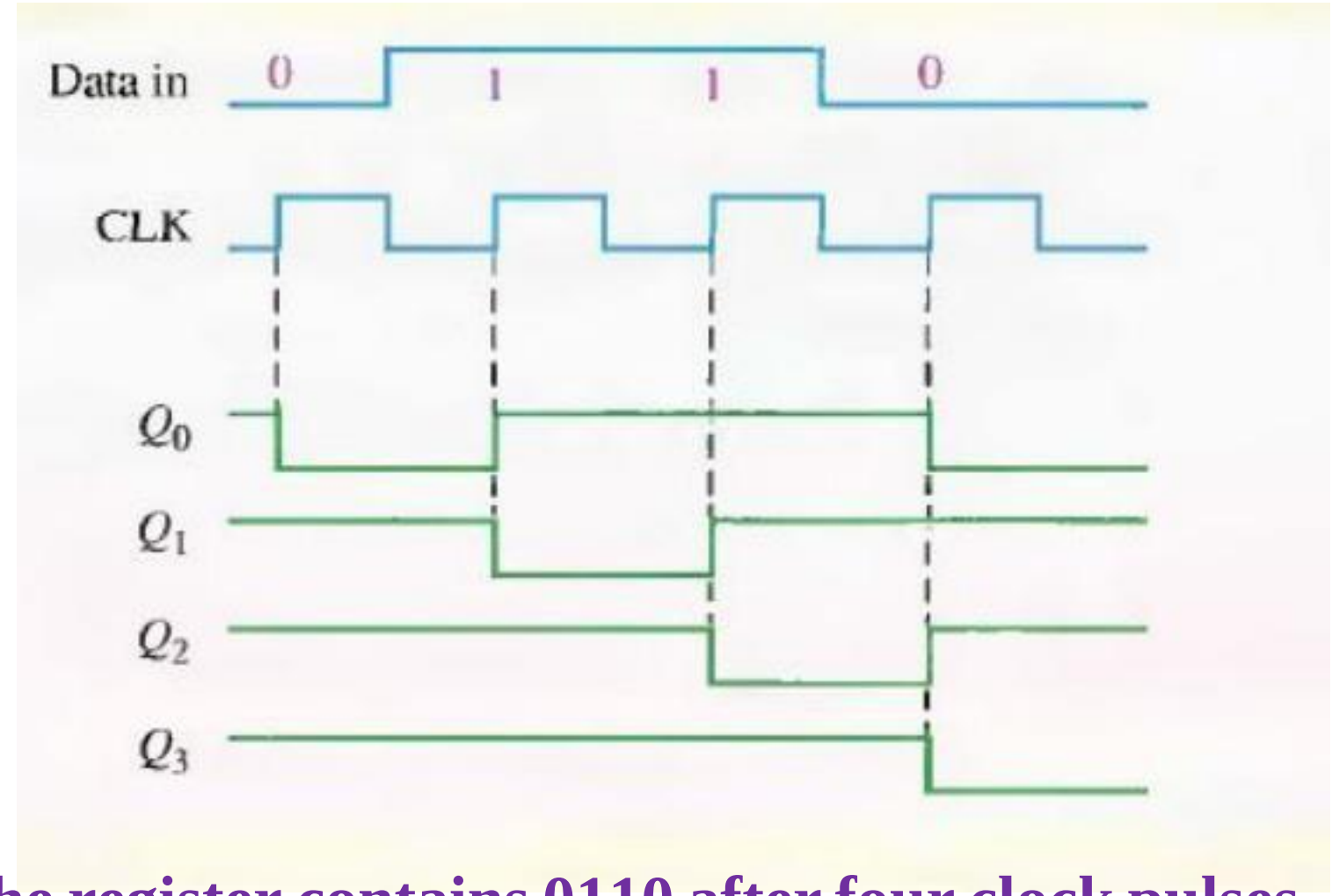




Example 9-2

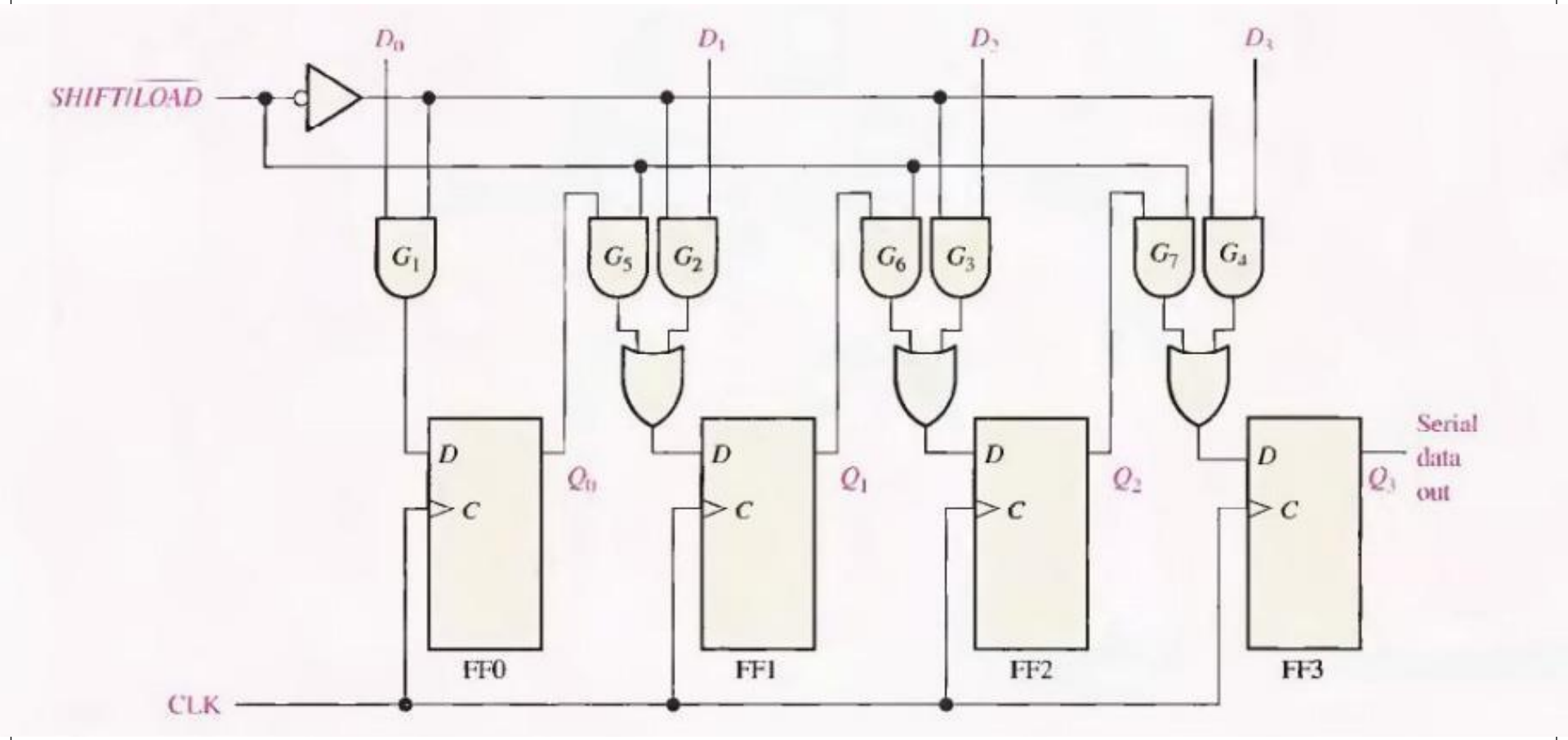
Show the states of the 4-bit register (SRG 4) for the data input and clock waveforms in Figure 9–9(a). The register initially contains all 1s.





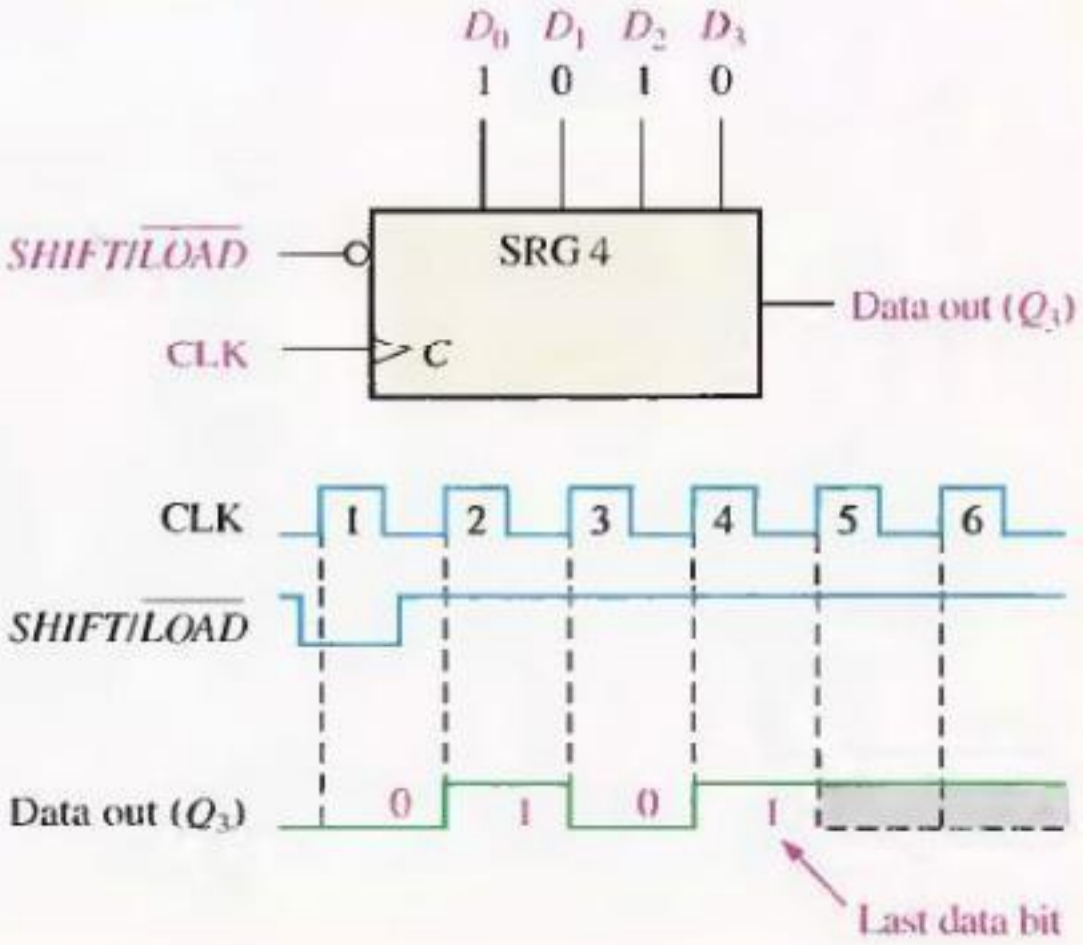
The register contains 0110 after four clock pulses

Parallel In serial Out Shift Register

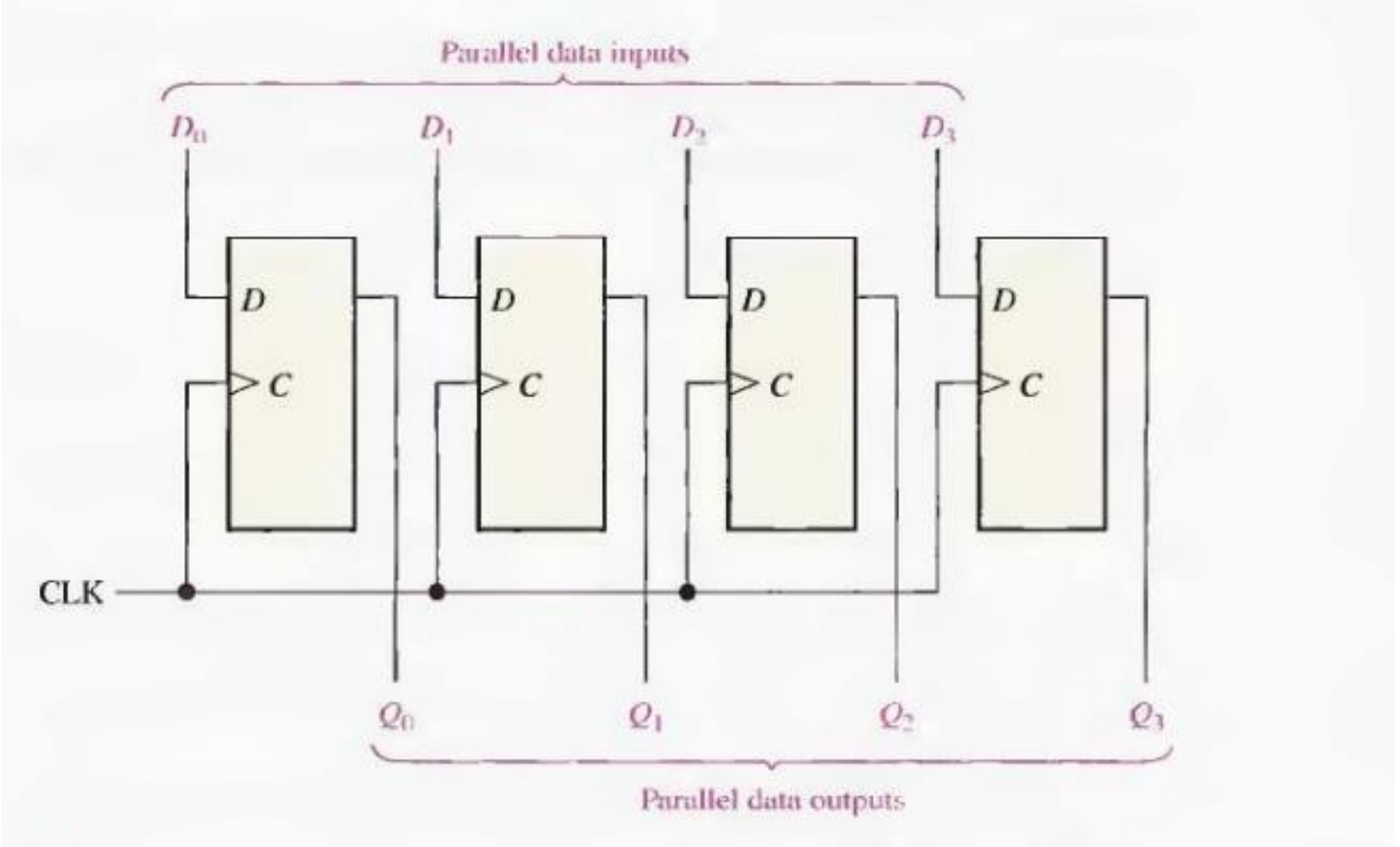


Show the data-output waveform for a 4-bit register with the parallel input data and the clock and *SHIFT*/$\overline{LOAD}$ waveforms given in Figure 9–13(a). Refer to Figure 9–12(a) for the logic diagram.

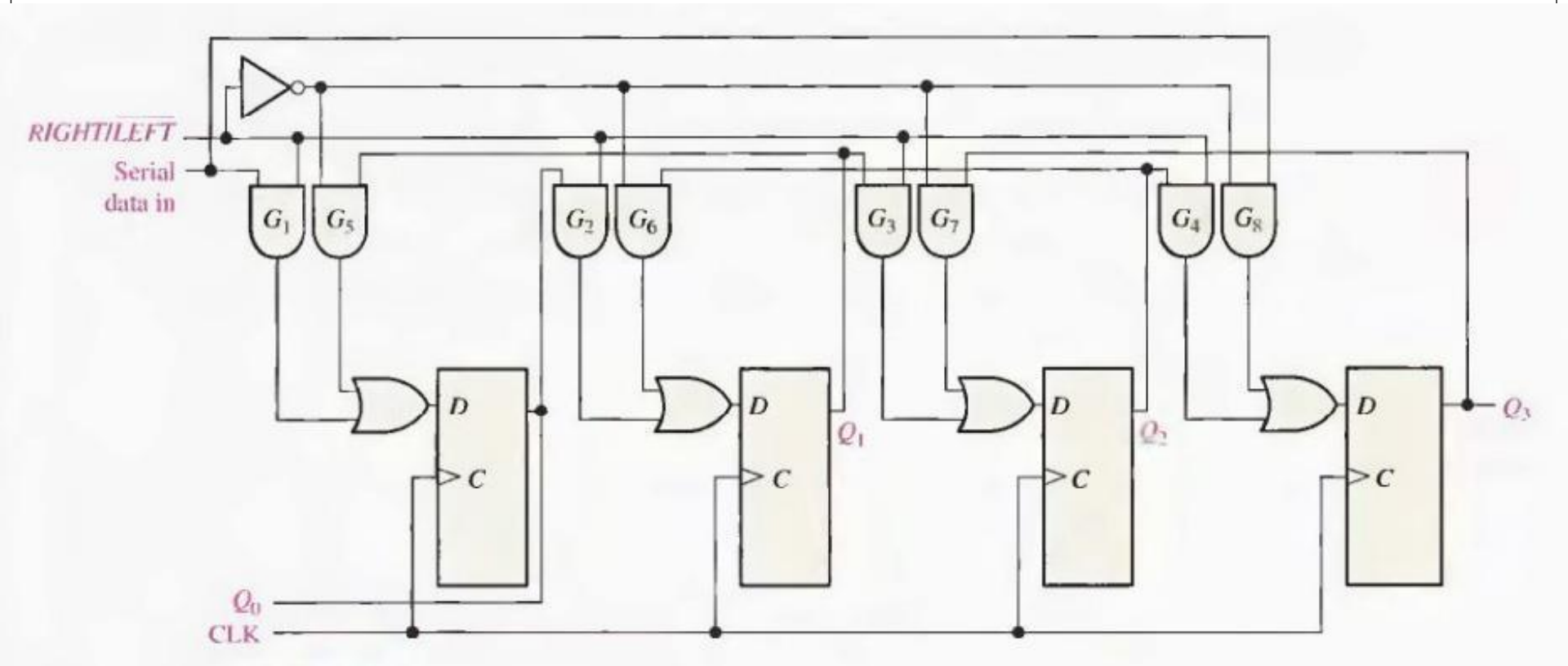
Example 9-3



Parallel In/ Parallel out Register

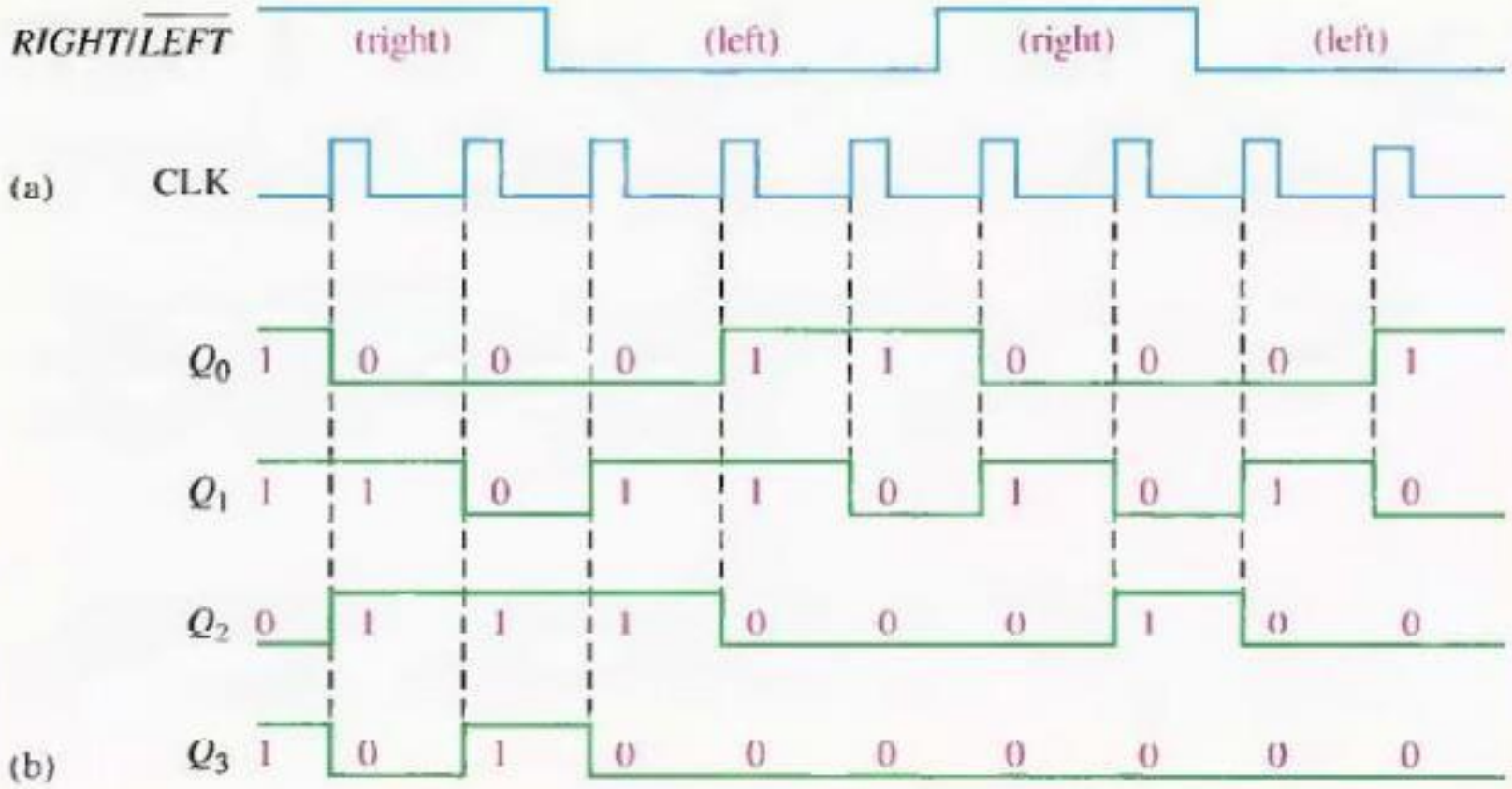


Bidirectional shift Register



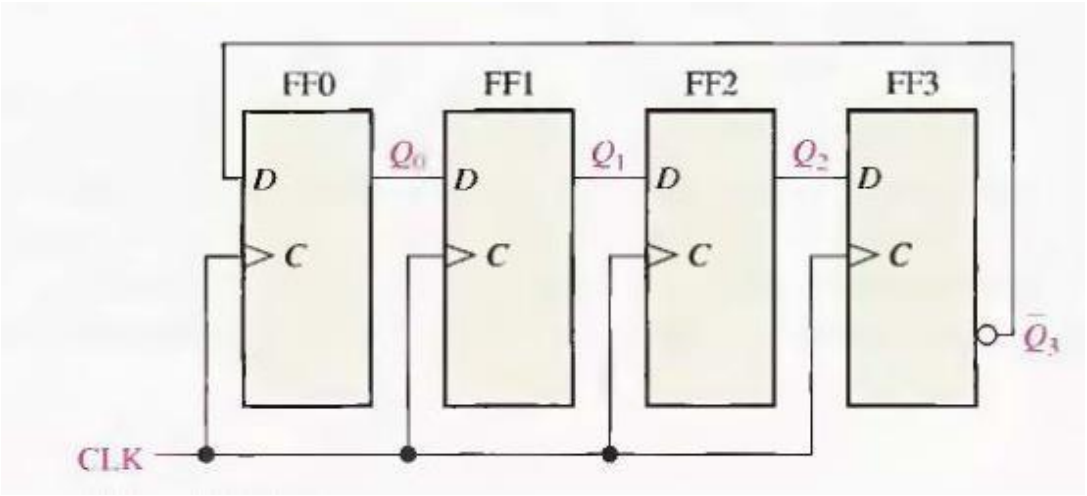
Example 9-4

Determine the state of the shift register of Figure 9–19 after each clock pulse for the given *RIGHT*/$\overline{LEFT}$ control input waveform in Figure 9–20(a). Assume that $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 0$, and $Q_3 = 1$ and that the serial data-input line is LOW.



Shift Register Counters

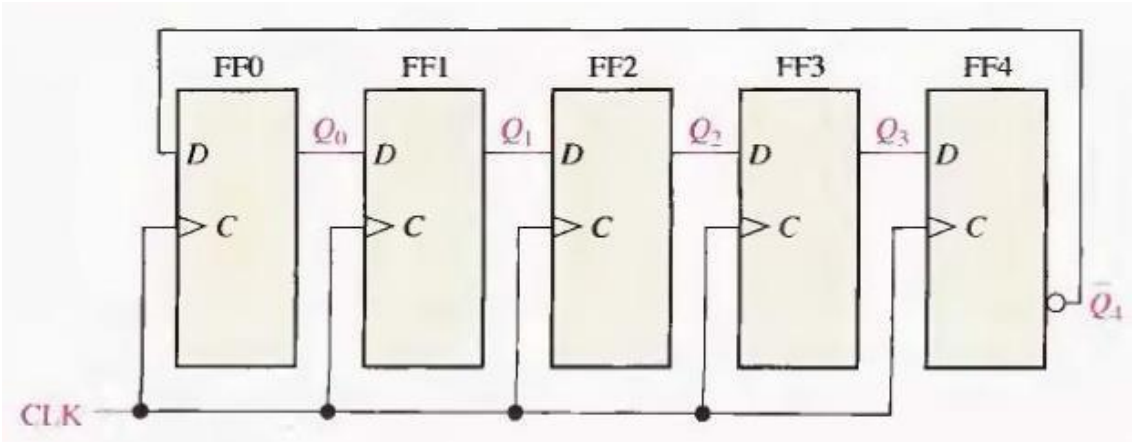
4-bit Johnson Counter



CLOCK PULSE	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

Shift Register Counters

5-bit Johnson Counter



CLOCK PULSE	Q_0	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

Shift Register Counters

1010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101
0101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010101010

FIGURE 9–24
Timing sequence for a 4-bit Johnson counter.

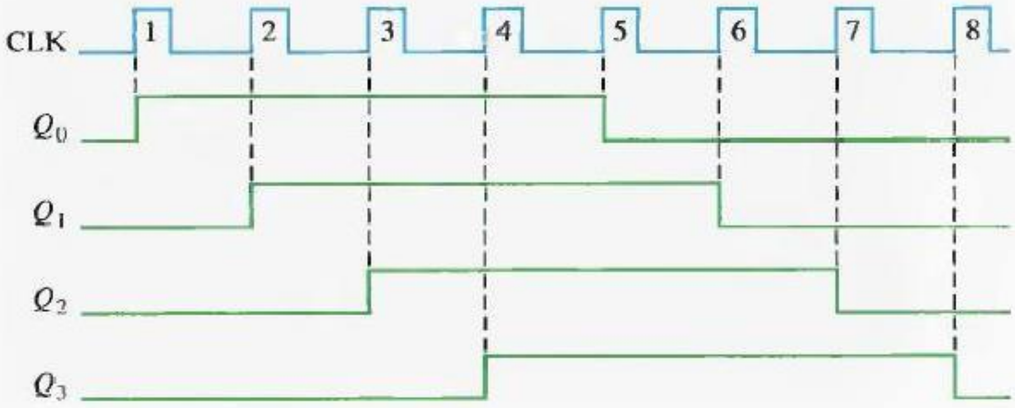
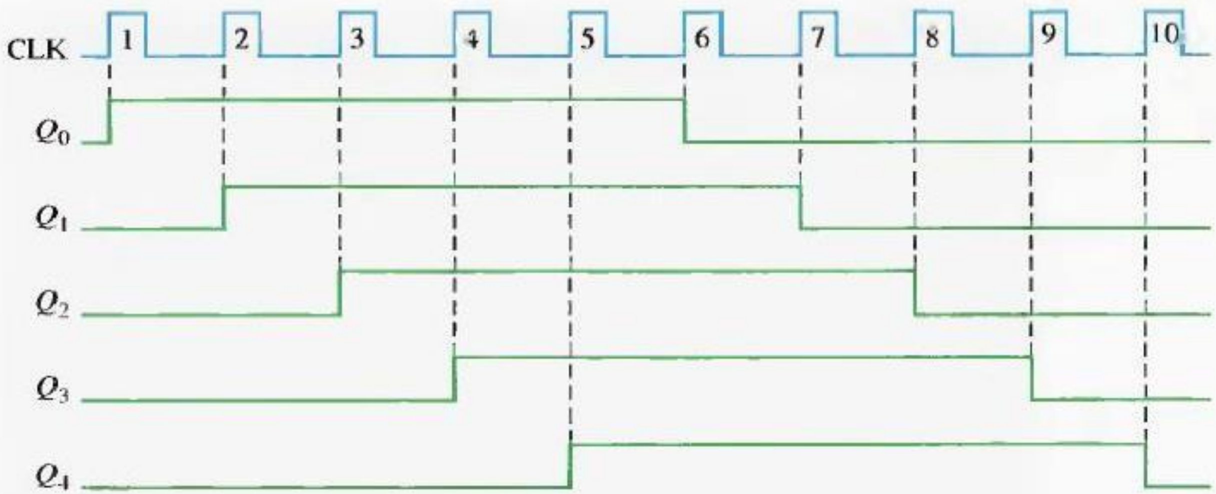
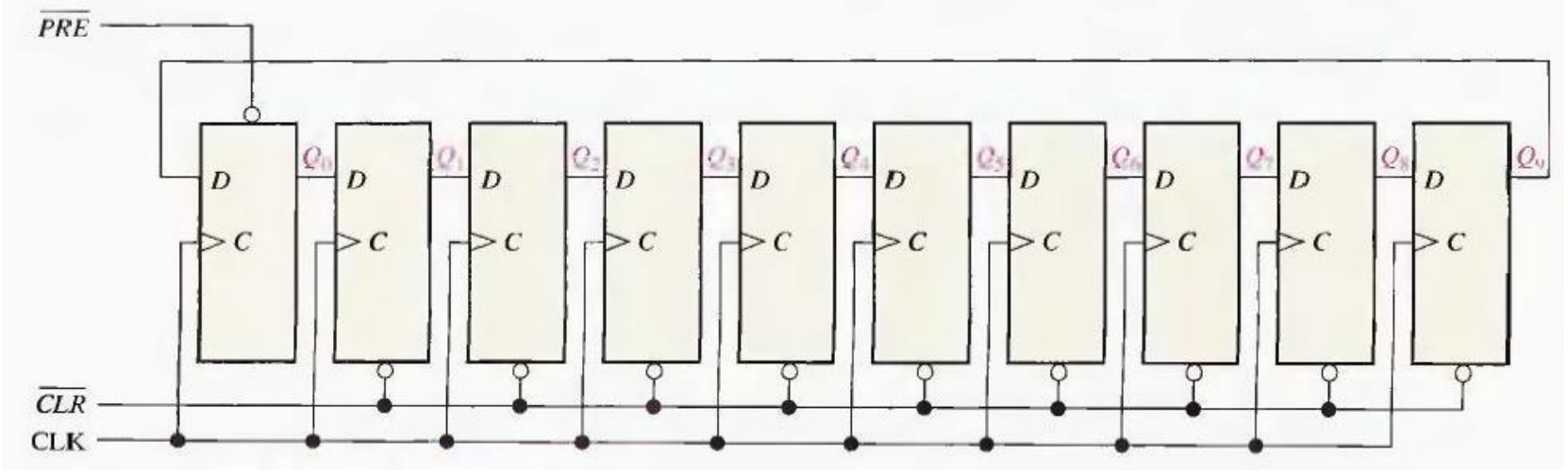


FIGURE 9–25
Timing sequence for a 5-bit Johnson counter.



Shift Register Counters

10-bit Ring Counter



CLOCK PULSE	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0
3	0	0	0	1	0	0	0	0	0	0
4	0	0	0	0	1	0	0	0	0	0
5	0	0	0	0	0	1	0	0	0	0
6	0	0	0	0	0	0	1	0	0	0
7	0	0	0	0	0	0	0	1	0	0
8	0	0	0	0	0	0	0	0	1	0
9	0	0	0	0	0	0	0	0	0	1