OPERATIONS OF A MICROPROCESSOR

- Microprocessor Initiated operations
- Internal Operations
- Peripheral(Externally Initiated) operations

Microprocessor Initiated Operations

- Memory Read
- Memory Write
- I/O Read
- I/O Write

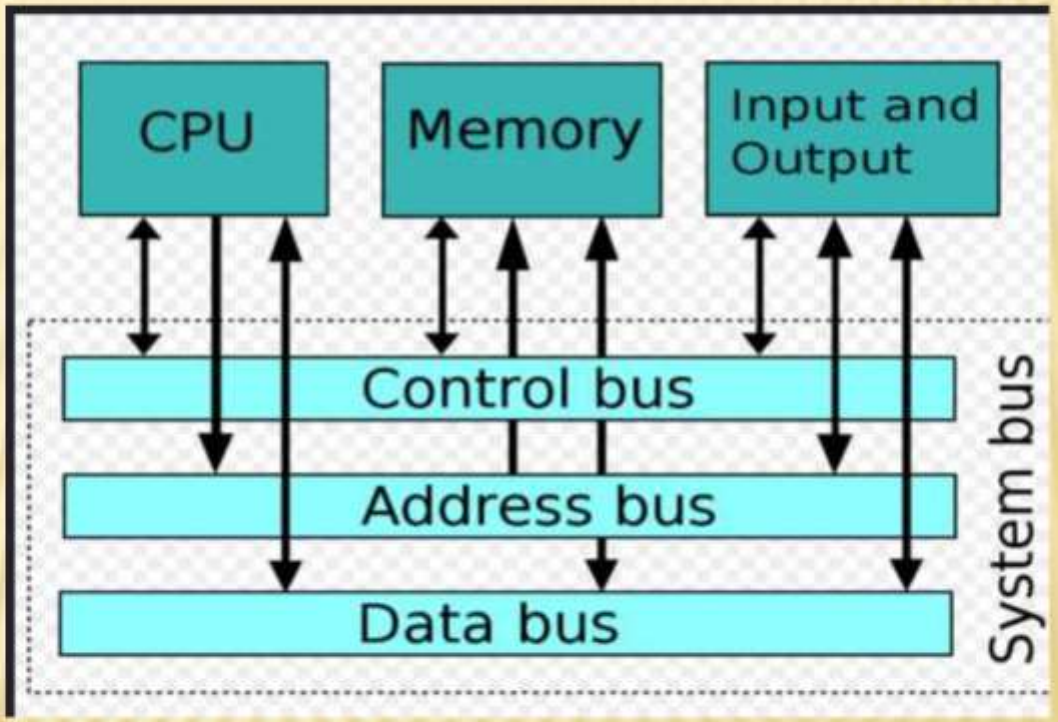
BUS ORGANIZATION

- What is a Bus?
- It is a set of pins, wires or signals having common functions as bus.

- What is system Bus?
- A system bus is a bundle of wires that are grouped together to serve a single purpose in microprocessor, generally there are three sets of communication lines that are called buses.
- It combines the functions of a data bus to carry information, an address bus to determine where it should be sent, and a control bus to determine its operation.

- They are address bus, the data bus and control bus

System bus (data, address and control bus)



ADDRESS BUS

- The bus over which the microprocessor sends out the address of a memory location or I/O location is called as the address bus.
- In 8085 microprocessor, Address bus is of 16 bits. This means that Microprocessor 8085 can transfer maximum 16 bit address which means it can address 65,536 different memory locations.
- This bus is multiplexed with 8 bit data bus. So, the most significant bits (MSB) of address goes through Address bus and LSB goes through multiplexed data bus.
- In 8085 address bus is 16 bit A0 – A15

- Data Bus

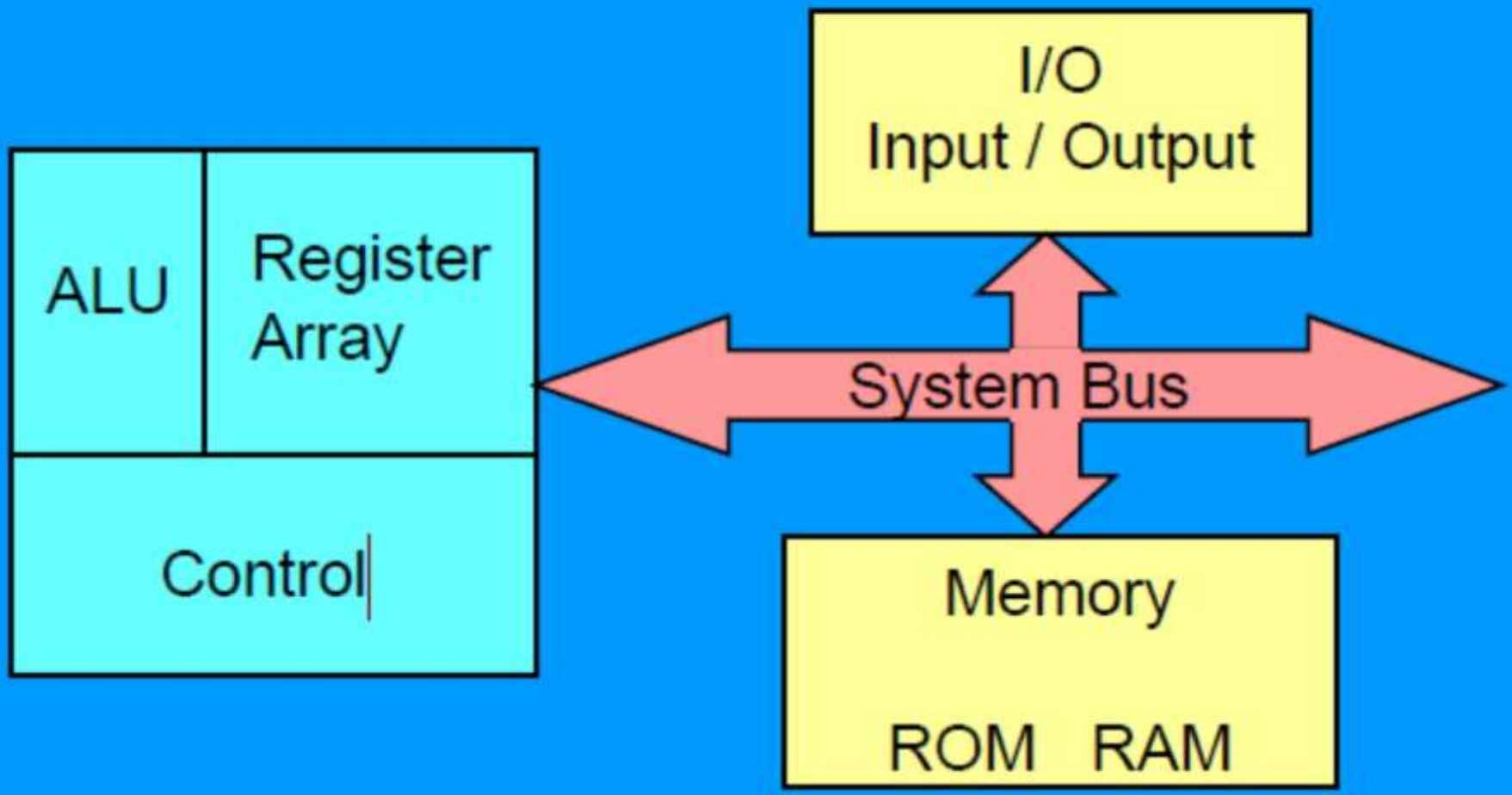
- It is bi-directional as Microprocessor requires to send or receiver data. The data bus also works as bus in 8 bits long.
- A data bus simply carries data. Internal buses carry information within the processor, while external buses carry data between the processor and the memory. Typically, the same data bus is used for both read/write operations.
- When it is a write operation, the processor will put the data on to the data bus. When it is the read operation, the memory controller will get the data from the specific memory block and put it in to the data bus.
- The data bus in8085 is of 8 parallel lines $D_0 – D_7$

CONTROL BUS

- The control bus is used for sending control signals to the memory and I/O devices. The CPU sends control signal on the control bus to enable the outputs of addressed memory devices or I/O port devices.

- Some of the control bus signals are as follows:
- 1.Memory read
- 2.Memory write
- 3.I/O read
- 4.I/O write.

MICROPROCESSOR SYSTEMS WITH BUS ORGANIZATION



MEMORY

- The user enters its instructions in binary format into the memory.
- The microprocessor then reads these instructions and whatever data is needed from memory, executes the instructions and places the results either in memory or produces it on an output device.

MEMORY ORGANIZATION

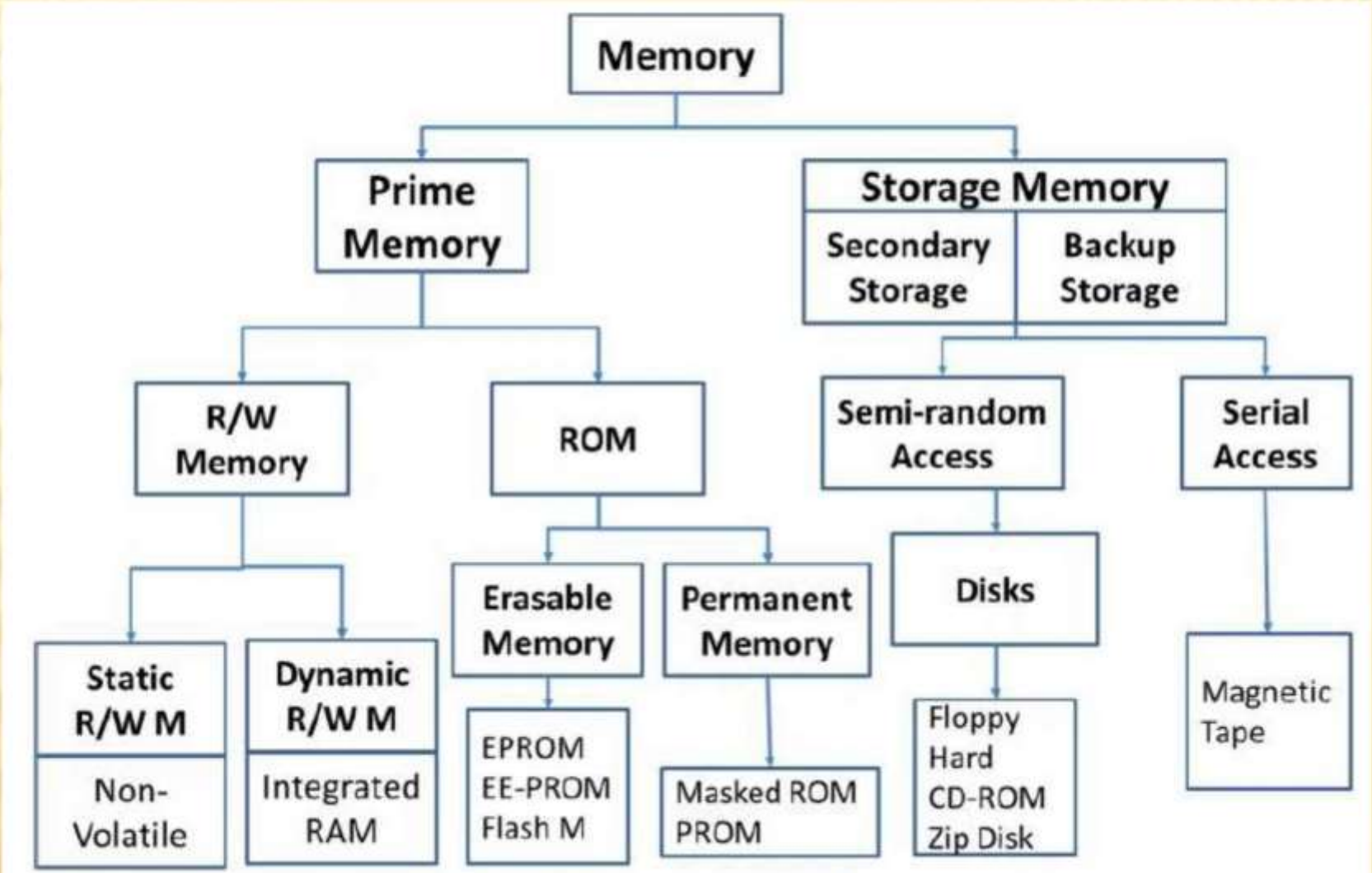


Figure: Classification of Memory

- ✓ Masked ROM: the program or data are permanently installed at the time of manufacturing as per requirement. The data cannot be altered. The process of permanent recording is expensive but economic for large quantities.
- ✓ PROM (Programmable Read Only Memory): The basic function is same as that of masked ROM. but in PROM, we have fuse links. Depending upon the bit pattern, the fuse can be burnt or kept intact.
- ✓ EPROM (Erasable Programmable Read Only Memory): The EPROM is programmable by the user. It uses MOS circuitry to store data. They store 1's and 0's in form of charge. The information stored can be erased by exposing the memory to ultraviolet light which erases the data stored in all memory locations.
- ✓ EEPROM: (Electrically erasable programmable read only memory): This is similar to EPROM except that the erasing is done by electrical signals instead of ultraviolet light. The main advantage is the memory location can be selectively erased and reprogrammed. But the manufacturing process is complex and expensive so do not commonly used.

+ Classification of RAM memory

- ✓ SRAM (Static RAM): SRAM consists of the flip-flop; using either transistor or MOS. for each bit we require one flip-flop. Bit status will remain as it is; unless and until you perform next write operation or power supply is switched off.

+ Advantages of SRAM:
  - ✓ Fast memory (less access time)
  - ✓ Refreshing circuit is not required.
+ Disadvantages of SRAM:
  - ✓ Low package density
  - ✓ Costly
+ DRAM (Dynamic RAM): In this type of memory a data is stored in form of charge in capacitors. When data is 1, the capacitor will be charged and if data is 0, the capacitor will not be charged. Because of capacitor leakage currents, the data will not be held by these cells. So the DRAMs require refreshing of memory cells. It is a process in which same data is read and written after a fixed interval.
+ Advantages of DRAM:
  - ✓ High package density
  - ✓ Low cost
+ Disadvantages of DRAM:
  - ✓ Required refreshing circuit to maintain or refresh charge on the capacitor, every
+ after few milliseconds.

INPUT / OUTPUT (I/O)

- MPU communicates with outside word through I/O device.
- There are 2 different methods by which MPU identifies and communicates With I/O devices these methods are:
  a. Direct I/O (Peripheral)
  b. Memory-Mapped I/O
- The methods differ in terms of the
- No. of address lines used in identifying an I/O device.
- Type of control lines used to enable the device.
- Instructions used for data transfer.

INPUT / OUTPUT (I/O)

- Direct I/O (Peripheral):-
- This method uses two instructions (IN & OUT) for data transfer.
- MPU uses 8 address lines to send the address of I/O device (can identify 256 input devices & 256 output devices).
- The (I/P & O/P devices) can be differentiated by control signals I/O Read (IOR) and I/O Write (IOW).
- The steps in communicating with an I/O device are similar to those in communicating with memory and can be summarized as follows:
  - 1 The MPU places an 8-bit device address on address bus then decoded.
  - 2 The MPU sends a control signal (IOR or IOW) to enable the I/O device.
  - 3 Data are placed on the data bus for transfer.

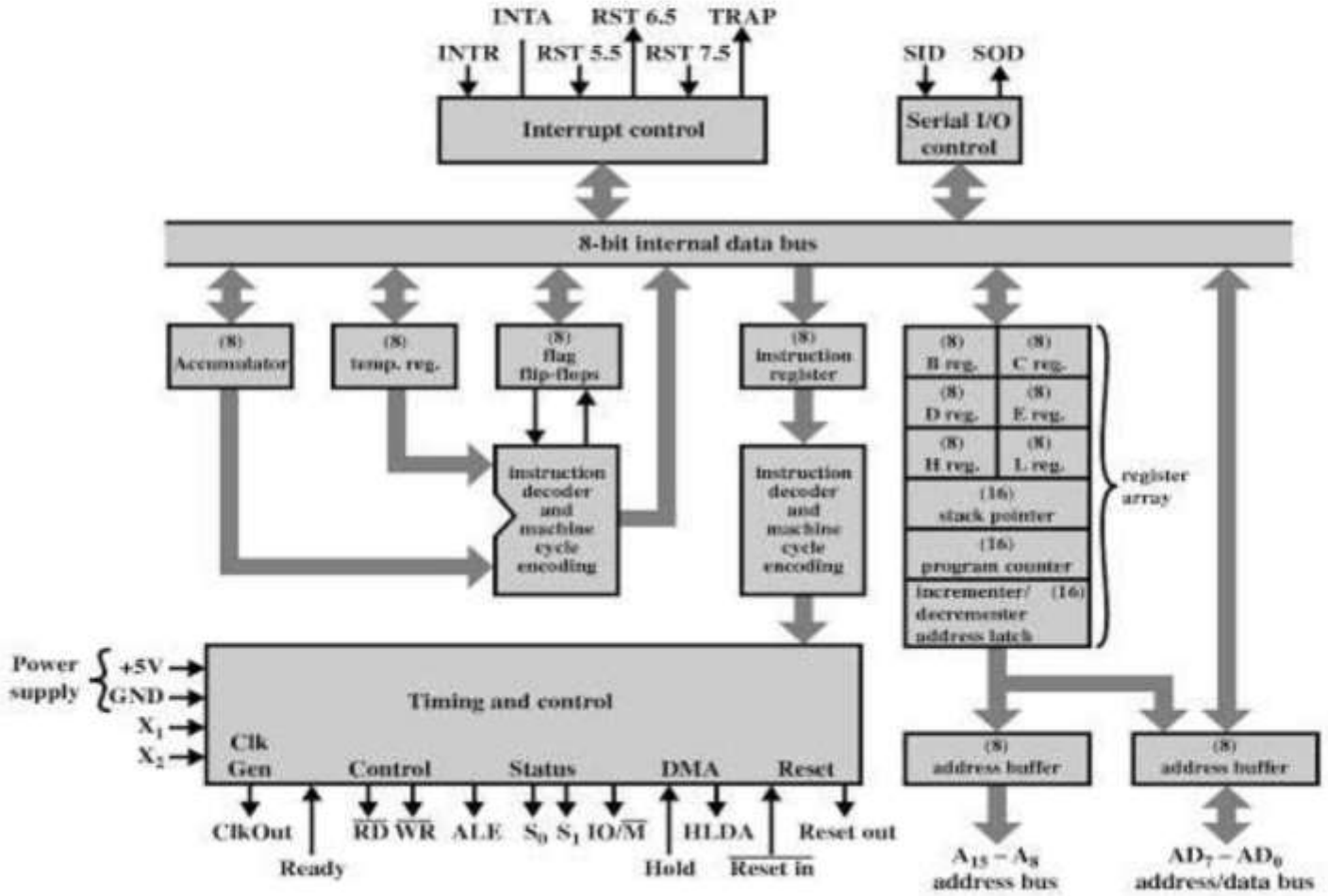
INPUT / OUTPUT (I/O)

- Memory-Mapped I/O:-
- The MPU uses 16 address lines to identify an I/O device.
- This is similar to communicating with a memory location.
- Use the same control signals (MEMR or MEMW) and instructions as those of memory.
- The MPU views these I/O devices as if they were memory locations.
- There are no special I/O instructions.
- It can identify 64k address shared between memory & I/O devices.

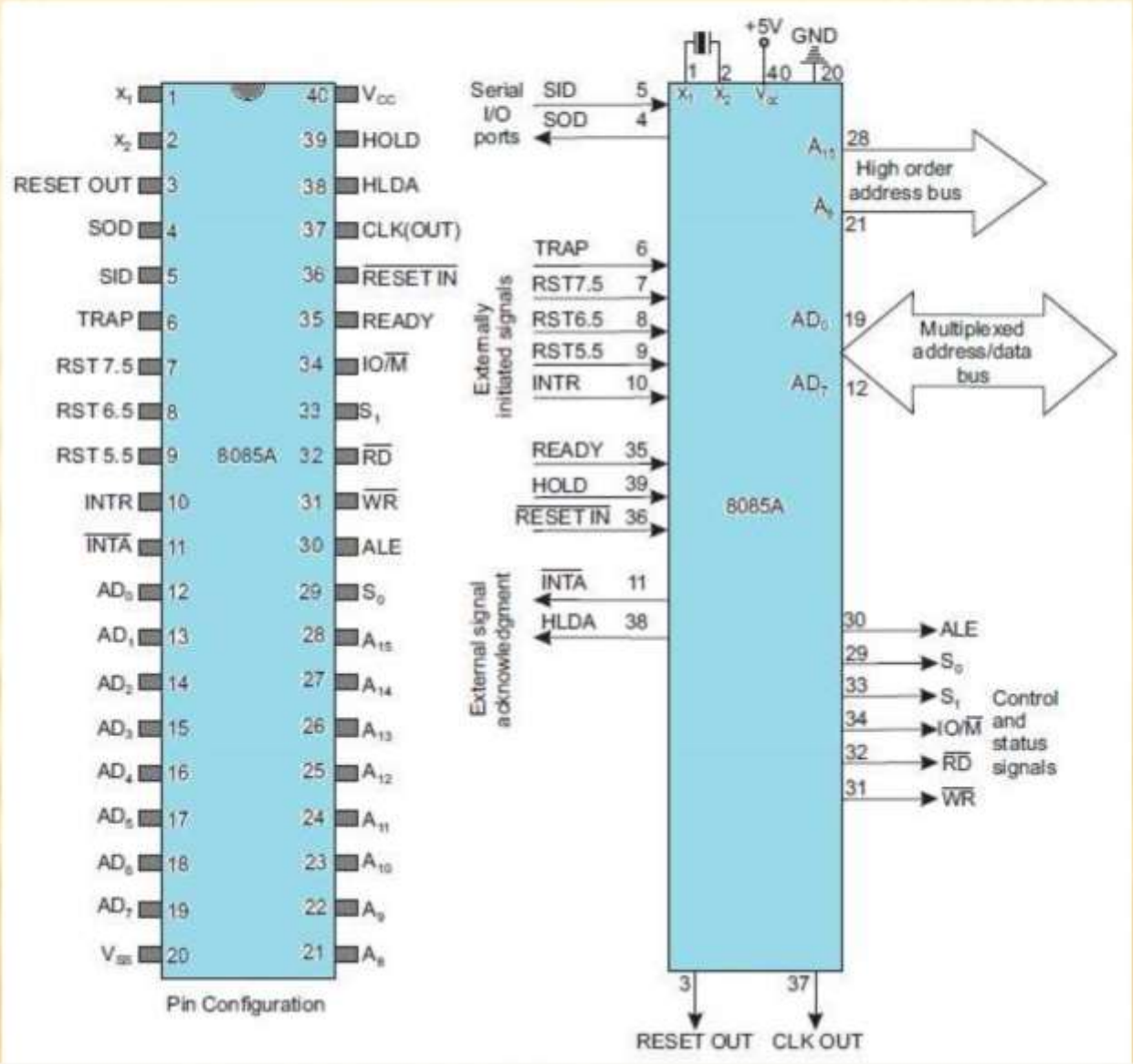
8085 MICROPROCESSOR

- It is an 8-bit microprocessor i.e. it can accept, process, or provide 8-bit data simultaneously.
- It operates on a single +5V power supply connected at Vcc; power supply ground is connected to Vss.
- It operates on clock cycle with 50% duty cycle.
- It has on chip clock generator. This internal clock generator requires tuned circuit like LC, RC or crystal. The internal clock generator divides oscillator frequency by 2 and generates clock signal, which can be used for synchronizing external devices.
- It can operate with a 3 MHz clock frequency. The 8085A-2 version can operate at the maximum frequency of 5 MHz
- It has 16 address lines, hence it can access (216) 64 Kbytes of memory.
- It provides 8 bit I/O addresses to access (28) 256 I/O ports.
- In 8085, the lower 8-bit address bus (A0 – A7) and data bus (D0 – D7) are Multiplexed to reduce number of external pins. But due to this, external hardware (latch) is required to separate address lines and data lines.

FUNCTIONAL BLOCK DIAGRAM OF 8085



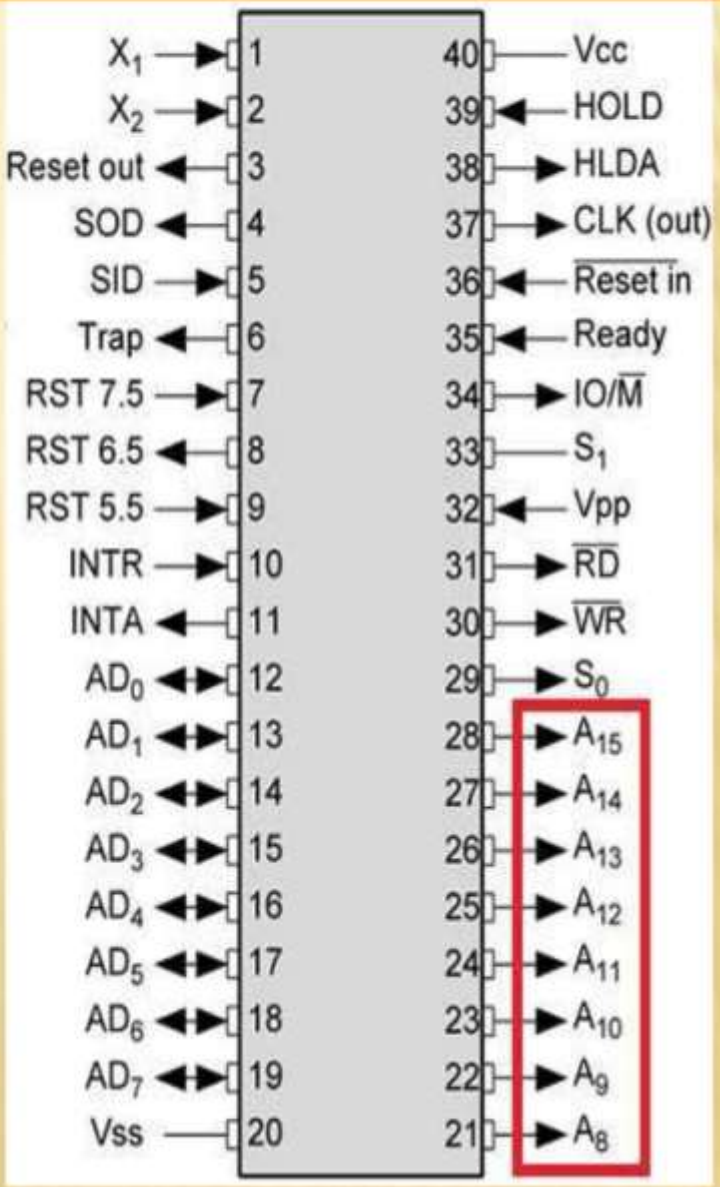
PIN DIAGRAM


8085A
Pin Configuration
Serial I/O ports
SID
SOD
Externally initiated signals
TRAP
RST7.5
RST6.5
RST5.5
INTR
External signal acknowledgment
INTA
HLDA
READY
HOLD
RESET IN
+5V
GND
High order address bus
Multiplexed address/data bus
Control and status signals
ALE
RD
WR
RESET OUT
CLK OUT

PIN DIAGRAM...

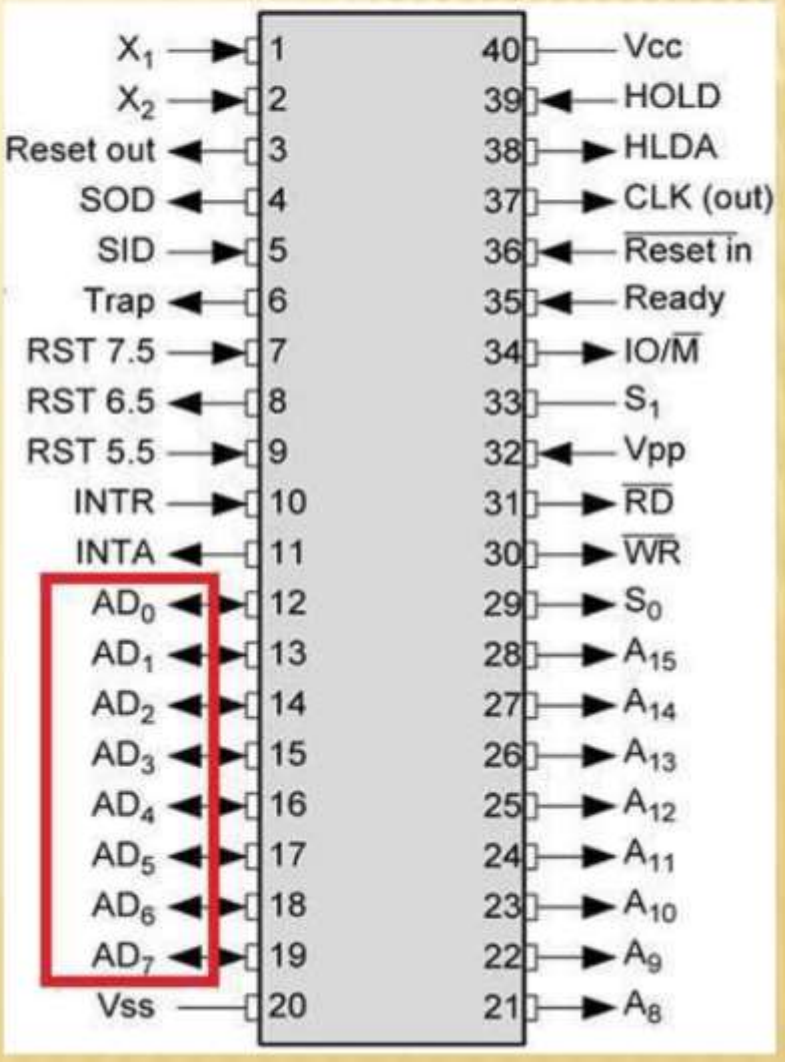
- Address Bus

- These pins carry the higher order of address bus.
- The address is sent from microprocessor to memory.
- A8 – A15. It carries the most significant 8-bit of memory I/O address.



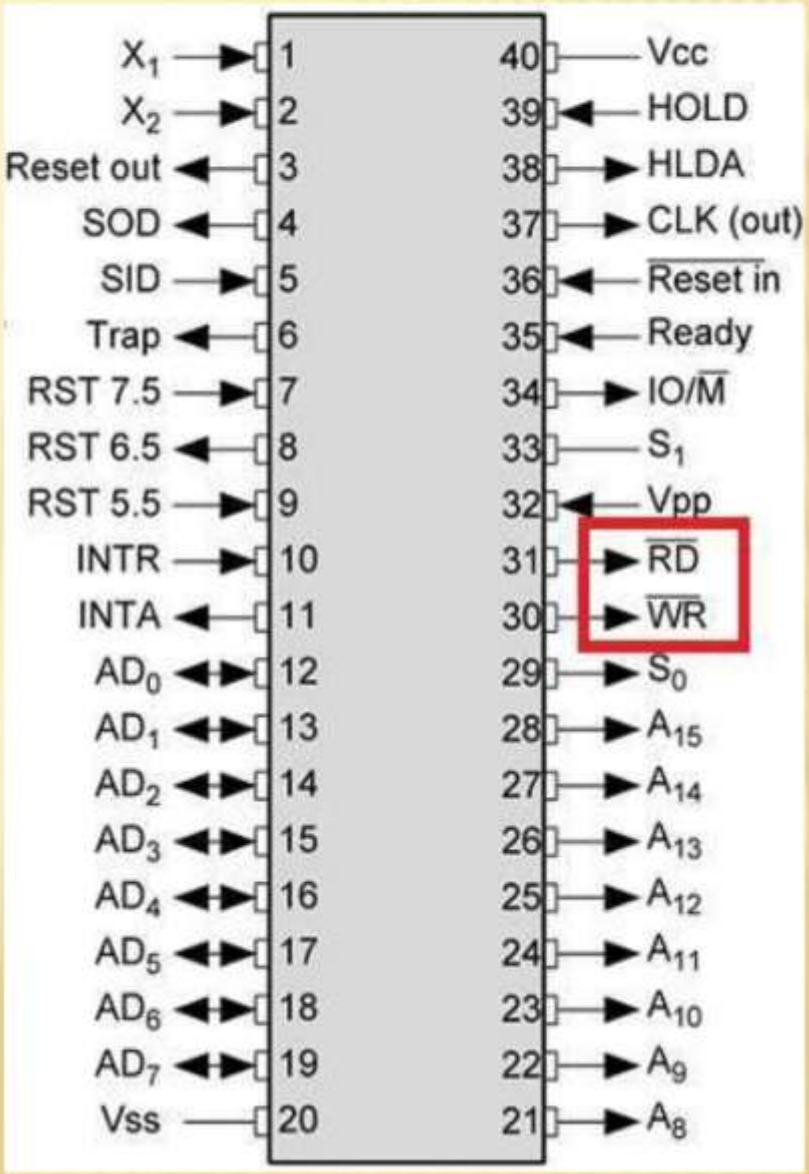
PIN DIAGRAM..

- Data Bus
  - ✓ Data bus is of 8 Bit.
  - ✓ It is used to transfer Data between microprocessor and memory.
  - ✓ AD0 – AD7. It carries the least significant 8-bit address and data bus.



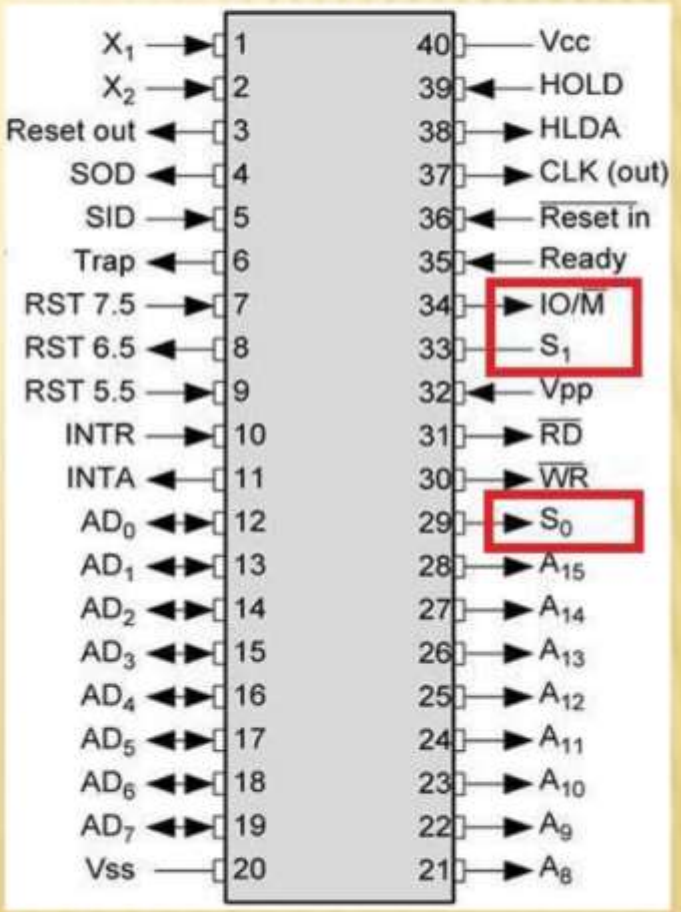
CONTROL SIGNAL

- **RD(Active Low Signal)**
- This signal indicates that the selected IO or memory device is to be read and is ready for accepting data available on the data bus.
- **WR(Active Low Signal)**
- This signal indicates that the data on the data bus is to be written into a selected memory or IO location.



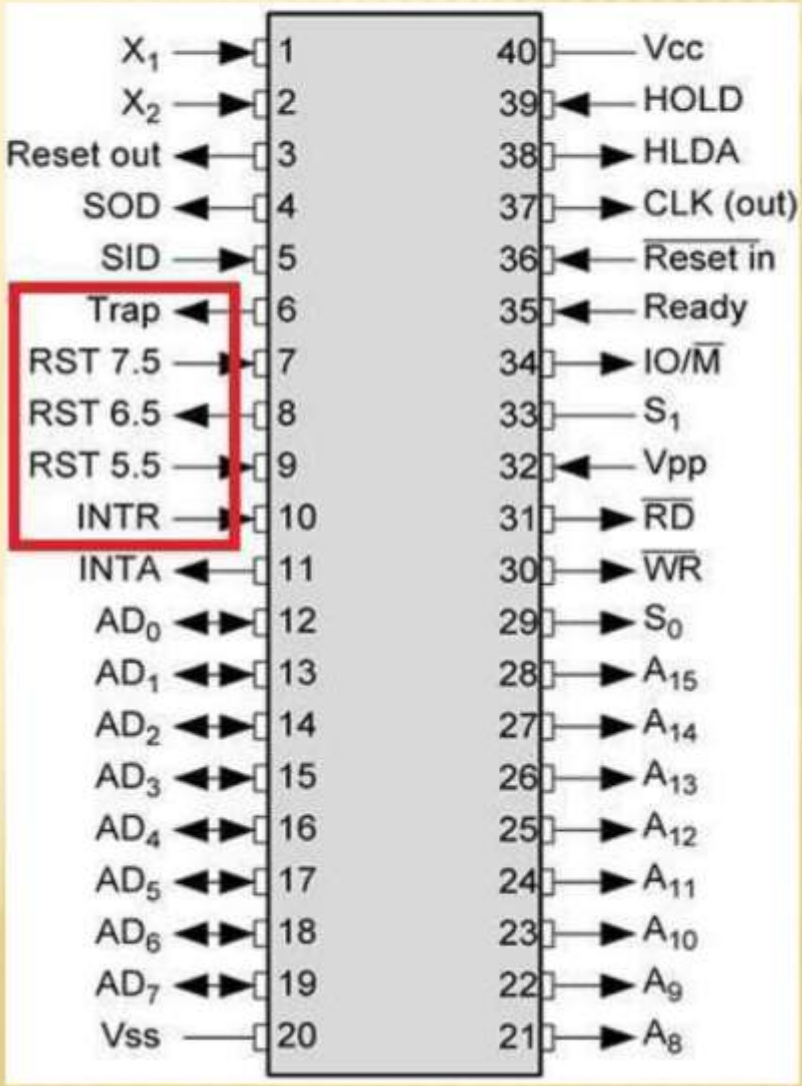
STATUS SIGNALS

- IO/M(Active low)
- This signal is used to differentiate between IO and Memory operations, i.e. when it is high indicates IO operation and when it is low then it indicates memory operation.
- **S0 & S1**
- These signals are used to identify the type of current operation.



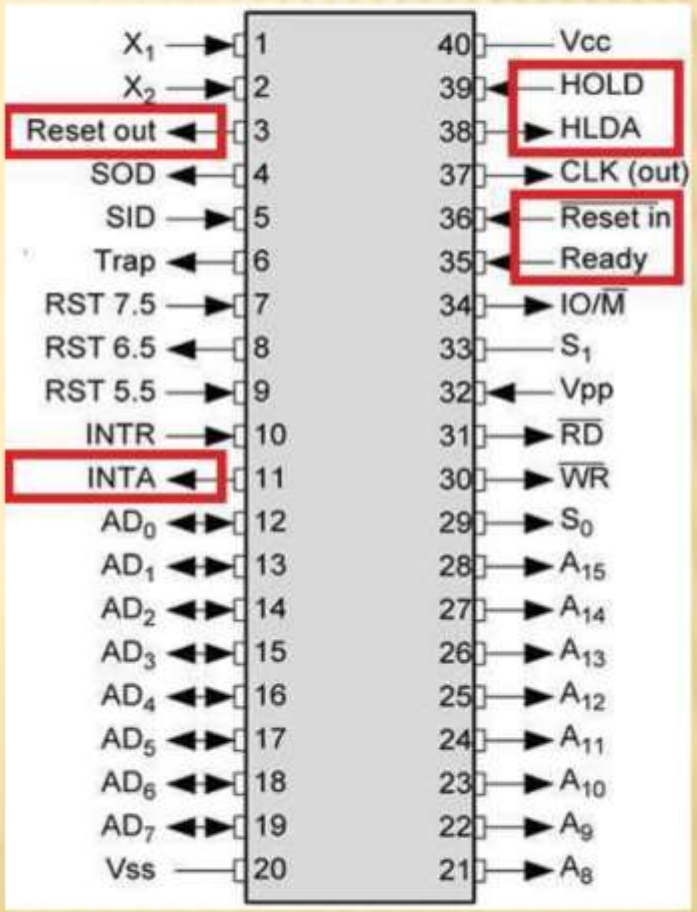
INTERRUPT SIGNALS

- TRAP is usually used for power failure and emergency shutoff.
- RST 7.5
- It is a maskable interrupt. It has the second highest priority.
- RST 6.5
- It is a maskable interrupt. It has the third highest priority.
- RST 5.5
- It is a maskable interrupt. It has the fourth highest priority.
- INTR
- It is a general-purpose interrupt. It is a maskable interrupt. It has the lowest priority.



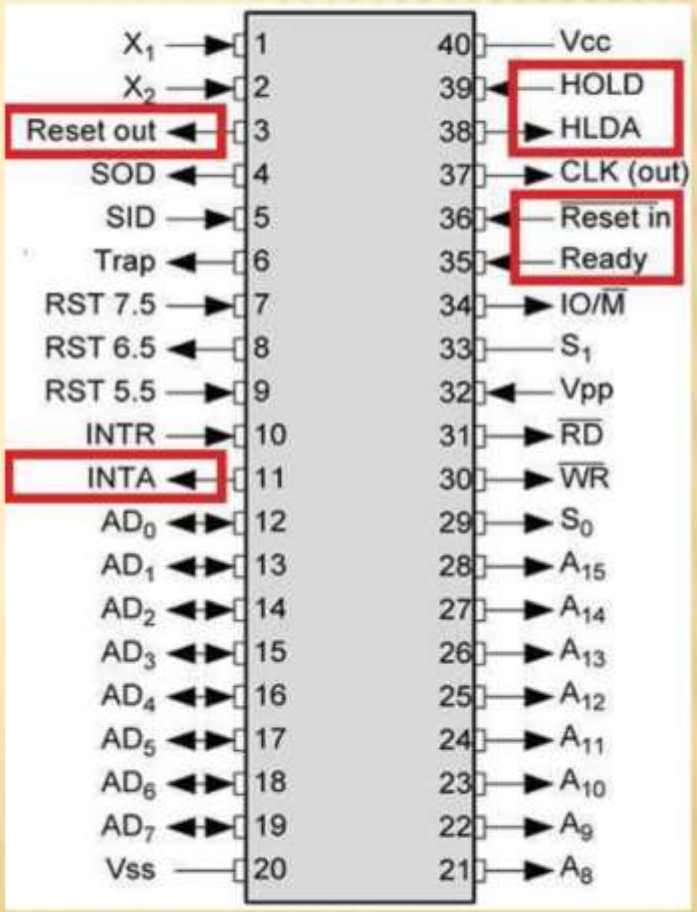
EXTERNALLY INITIATED SIGNALS

- INTA
- It is an interrupt acknowledgment signal.
- RESET IN
- This signal is used to reset the microprocessor by setting the program counter to zero.
- RESET OUT
- This signal is used to reset all the connected devices when the microprocessor is reset.



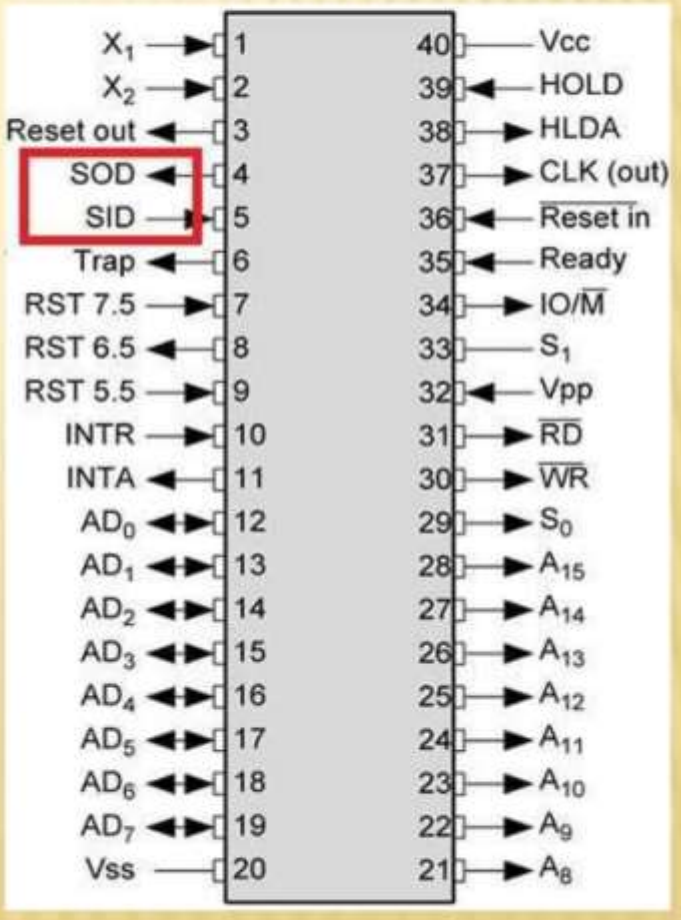
EXTERNALLY INITIATED SIGNALS

- Ready
- This signal indicates that the device is ready to send or receive data. If READY is low, then the CPU has to wait for READY to go high.
- HOLD
- This signal indicates that another master is requesting the use of the address and data buses.
- HLDA
- It indicates that the CPU has received the HOLD request and it will relinquish the bus in the next clock



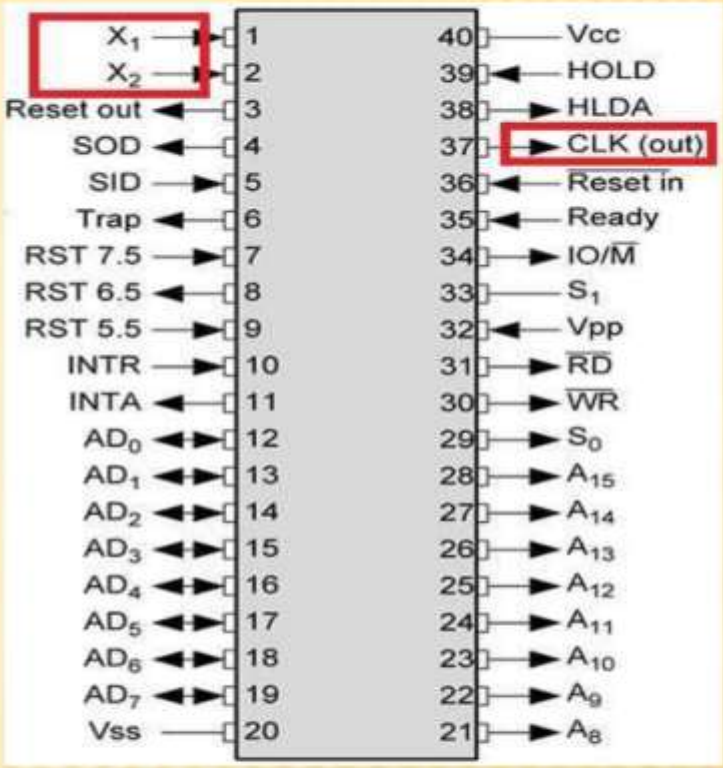
SERIAL I/O SIGNALS

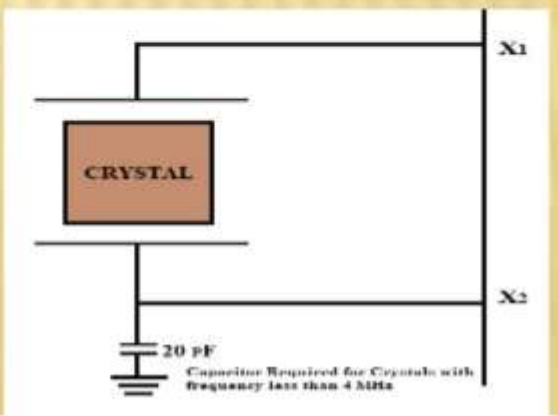
- SOD
- (Serial Output Data line) The output SOD is set/reset as specified by the SIM instruction.
- SID
- (Serial Input Data line) The data on this line is loaded into accumulator whenever a RIM instruction is executed.



CLOCK SIGNALS

- **X1, X2**
- A crystal (RC, LC N/W) is connected at these two pins and is used to set frequency of the internal clock generator. This frequency is internally divided by
- 2. To obtain 3.03 MHz, a clock source of 6.06 MHz must be connect to X1 and X2
- **CLK OUT**
- This signal is used as the system clock for devices connected with the microprocessor.

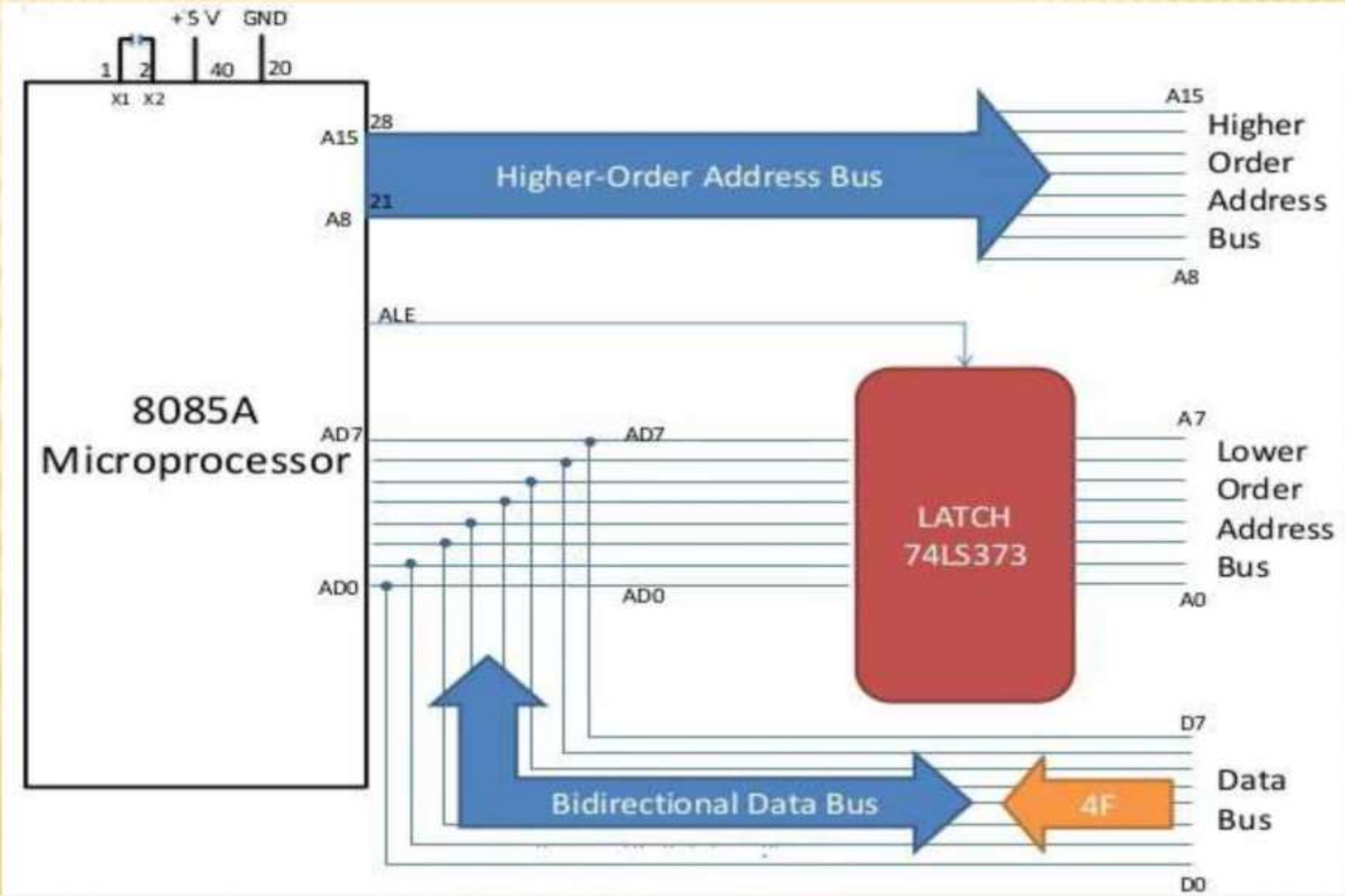




ADDRESS BUS

- The address bus has 8 signal lines A8 – A15 which are unidirectional.
- The other 8 address bits are multiplexed(time shared) with the 8 data bits. So, the bits AD0 –AD7are bi-directional and serve as A0 –A7and D0 –D7at the same time.
- The AD7–AD0 lines are serving a dual purpose and that they need to be demultiplexed to get all the information.
- The high order bits of the address remain on the bus for three clock periods. However, the low order bits remain for only one clock period and they would be lost if they are not saved externally. Also, notice that the low order bits of the address disappear when they are needed most.

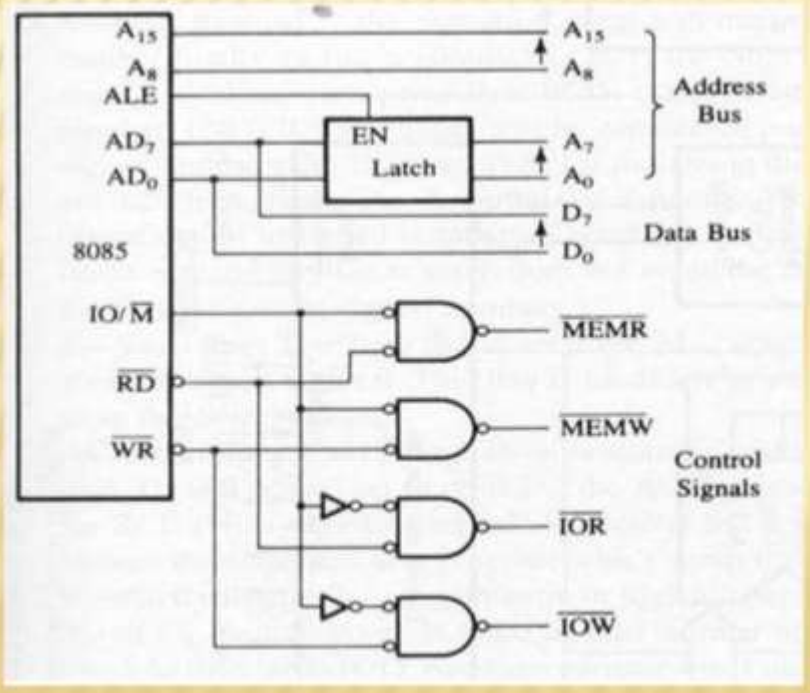
DEMULTIPLEXING OF BUSES



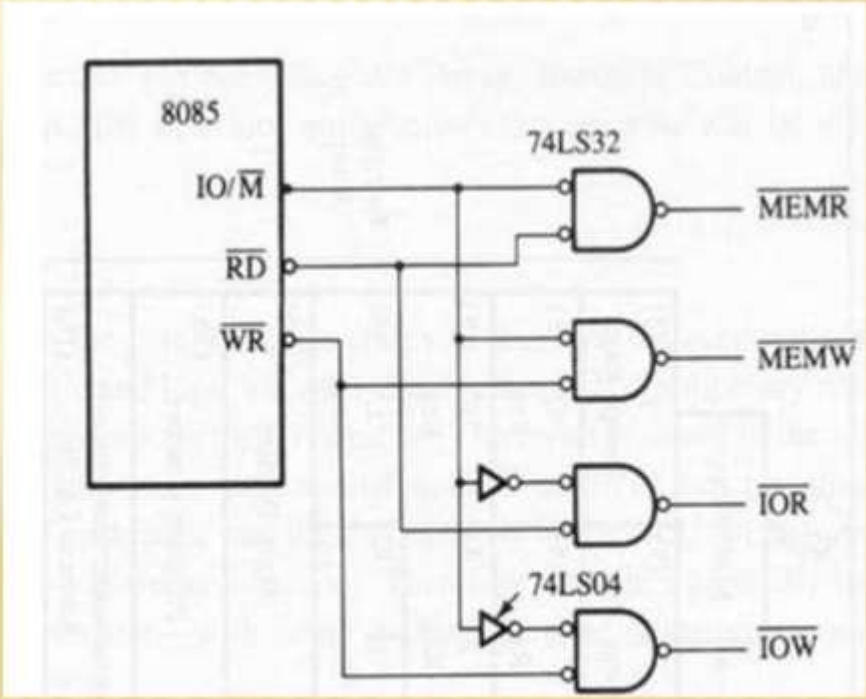
GENERATION OF CONTROL SIGNALS

- Signals are used both for memory and I/O related operations. So four different control signals are generated by combining the signals RD, WR and IO/M.

- 8085 De-multiplexed address and databus with Control Signal

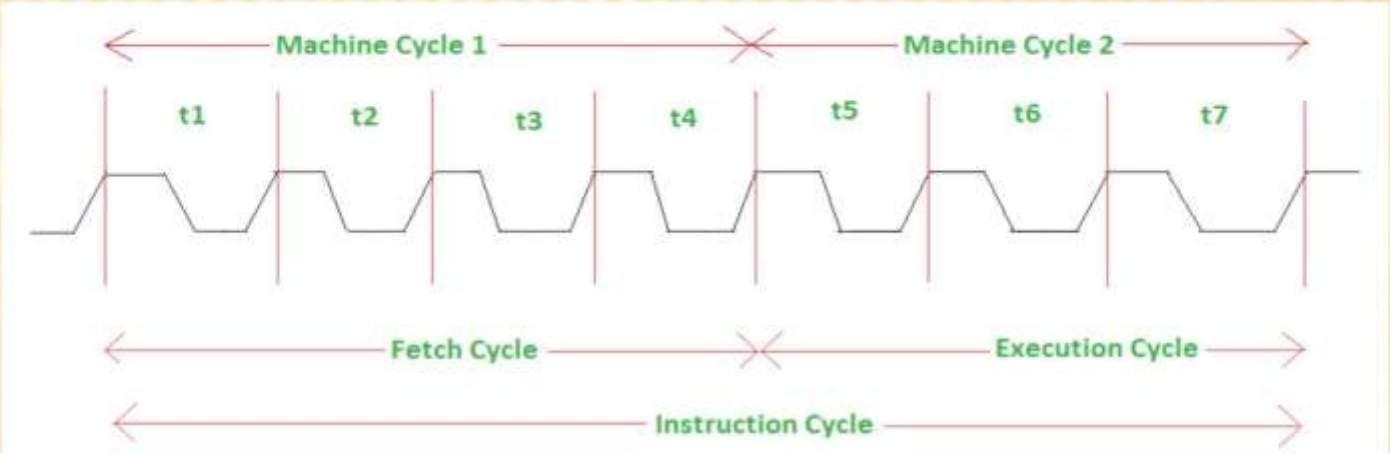


Control Signal Generation



INSTRUCTION CYCLE

- The time required to complete the execution of an instruction.
- In the 8085, an instruction cycle may consist of 1 to 6 machine cycles.
- The function of the microprocessor is divided into two cycle of the instruction
  a. Fetch (b)Execute
- Number of instructions are stored in the memory in sequence.
- In the normal process of operation, the microprocessor fetches (receives or reads) and executes one instruction at a time in the sequence until it executes the halt (HLT) instruction.
- Thus, an instruction cycle is defined as the time required to fetch and execute an instruction. Instruction Cycle (IC) = Fetch cycle (FC) + Execute Cycle (EC)



MACHINE CYCLE

- The time required to complete one operation of accessing memory, I/O, or acknowledging an external request. This cycle may consist of 3 to 6 T-states.
- The 8085 microprocessor has 7 basic machine cycles. They are
- 1. Opcode fetch cycle (4T)
- 2. Memory read cycle or operand fetch(3 T)
- 3. Memory write cycle (3 T)
- 4. I/O read cycle (3 T)
- 5. I/O write cycle (3 T)
- 6. Interrupt Acknowledge
- 7. Bus Idle cycle

OPCODE FETCH CYCLE

- The first step of executing any instruction is the Opcode fetch cycle. In this cycle, the microprocessor brings in the instruction's Opcode from memory.
- To differentiate this machine cycle from the very similar "memory read" cycle, the control & status signals are set as follows
- IO/M=0, s0 and s1 are both 1.
- This machine cycle has four T-states.
- The 8085 uses the first 3 T-states to fetch the opcode.
- T4 is used to decode and execute it.
- It is also possible for an instruction to have 6 T-states in an opcode fetch machine cycle.