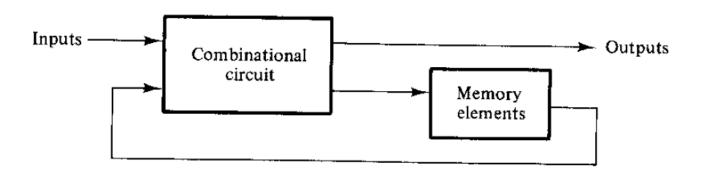
- ✓ Sequential Circuit: Synchronous and asynchronous sequential circuit.
- Flip-Flops: Basic Flip-Flops circuit, RS, D, JK and T Flip-Flip
- Triggering of Flip-Flops.
- Analysis of clocked sequential circuit: State Table, state diagram, state equation
- State reduction.
- Flip-Flop Characteristic and Excitation Table.
- Design of Clocked Sequential Circuits.
- ✓ Design of synchronous counter.

## **Sequential Circuit**

A **sequential circuit** is one whose outputs depend not only on its current inputs but also on the past sequence of inputs.



The block diagram demonstrates that the external outputs in a sequential circuit are a function not only of external inputs but also of the present state of the memory element. The next state of the memory elements is also a function of external inputs and the present state. Thus, a sequential circuit is specified by a time sequence of inputs, outputs and internal states.

## **Types of Sequential Circuit**

There are two main types of sequential circuits based on the timing of their signals-

- 1) Synchronous Sequential circuit.
- 2) Asynchronous Sequential Circuit.

A Synchronous Sequential circuit is a system whose behavior can be defined from the knowledge of its signals at discrete instants of time. It must employ signals that affect the memory elements only at discrete instants of time. One way of achieving this goal is to use clock pulses. The clock pulses are distributed throughout the system in such a way that memory elements are affected only with the arrival of the synchronization pulse. Synchronoussequential circuits that use clock pulses in the inputs of memory elements are called clocked sequential circuits.

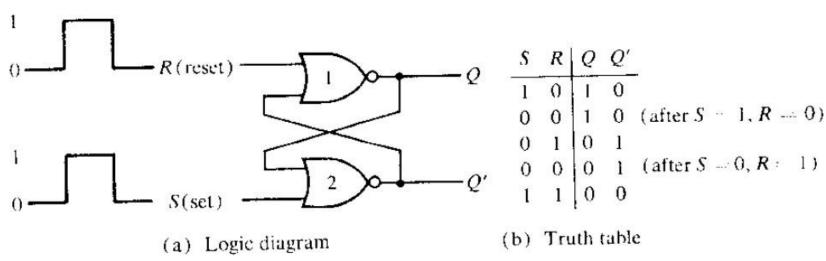
The behavior of an asynchronous sequential circuit depends upon the order in Which its input signals change and can be effected at any instant of time.

## Flip-Flops

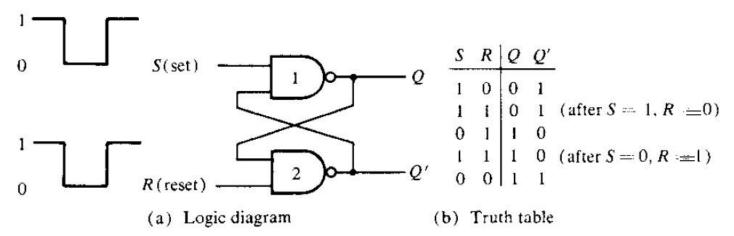
- ✓ The memory elements used in a clocked sequential circuits are called flip-flops. These circuits are binary cells capable of storing one bit information. A flip-flop circuit has two outputs, one for the normal value and one for the complement value of the bit stored in it.
- ✓ A flip-flop can maintain a binary state indefinitely (as long as power delivered to the circuit) until directed by an input signals to switch states.
- ✓ The major differences among various types of flip-flops are in the number of inputs they possess and in the manner in which the inputs affect the binary state.
- ✓ The most common types of flip-flops are
  - a) RS Flip-Flop
  - b) D Flip-Flop
  - c) JK Flip-Flop
  - d) T Flip-Flop

## **Basic Flip-Flop Circuit by NOR Gate**

- ✓ A flip-flop circuit can be constructed from two NAND gates or two NOR gates.
- ✓ The cross-coupled connection from the output of one gate to the input of the other gate constitutes a feedback path. For this reason, the circuits are classified as asynchronous sequential circuits.
- ✓ Each flip-flop has two outputs, Q and Q', and two inputs, set and reset. This types of flip-flop is sometimes called a direct-coupled RS flip-flop or SR latch.



## **Basic Flip-Flop Circuit by NAND Gate**

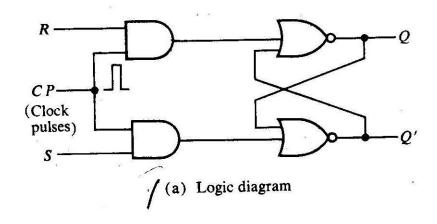


#### Note:

✓ A flip-flop has two useful states. When Q=1 and Q'=0, it is in the set state (or 1-state) and when Q=0 and Q'=1, it is the clear state (or, 0-state)

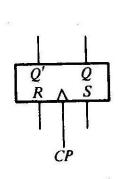
Inputs	Output (Flip-flop with NOR gates)	Output (Flip-flop with NAND gates)
S=1 and R=0	goes set state	goes reset state
S=0 and R=1	goes reset state	goes set state
S=0 and R=0	remain unchanged	goes indeterminate (undefined ) state
S=1 and R=1	goes indeterminate (undefined ) state	remain unchanged

# **Clocked RS Flip-Flop**

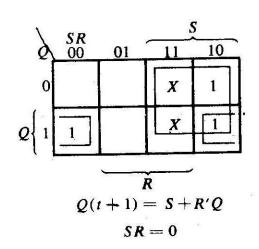


$\boldsymbol{\mathcal{Q}}$	S	R	Q(t+1)
0	0	0	0
0	0	i	0
0	1	0	1
0	1	1	indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	indeterminate

(c) Pharacteristic table

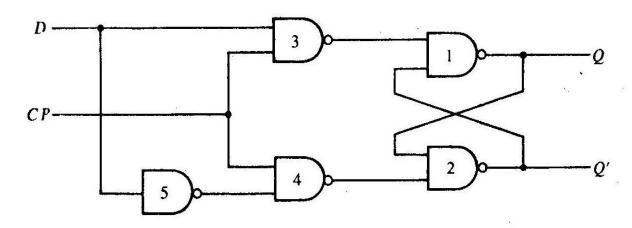


(b) Graphic symbol

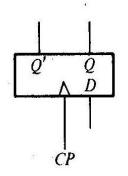


(d) Characteristic equation

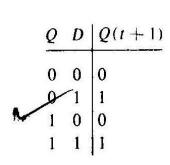
# **D-Flip-Flop**



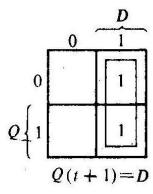
(a) Logic diagram with NAND gates



(b) Graphic symbol

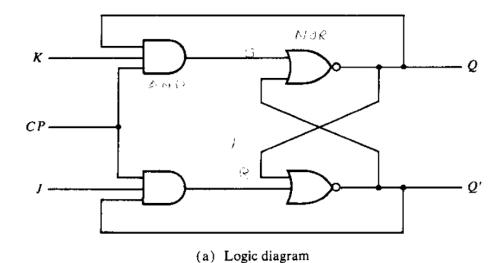


(c) Characteristic table



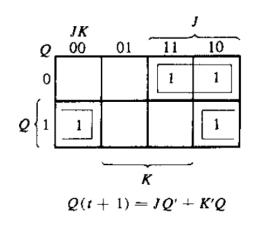
(d) Characteristic equation

# JK Flip-Flop



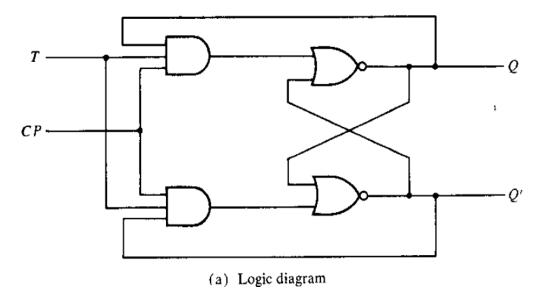
Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(b) Characteristic table



(c) Characteristic equation

## T Flip-Flop



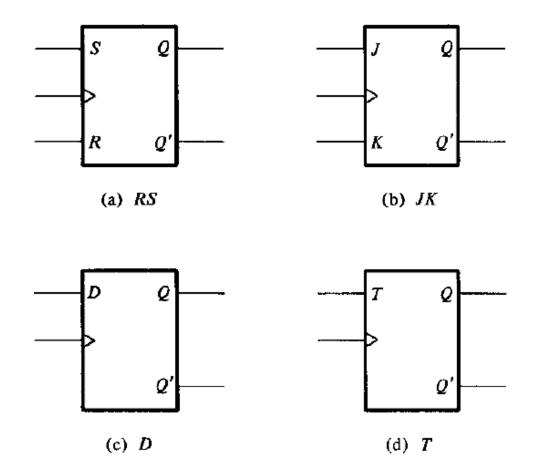
$\frac{Q}{0}$	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	ı	0

(b) Characteristic table

$$Q = \begin{bmatrix} T & T & T \\ 0 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}$$

$$Q(t+1) = TQ' + T'Q$$
  
(c) Characteristic equation

# **Graphic Symbols of Flip-Flops**



## **Triggering of Flip-Flops**

#### **✓** What is triggering?

The state of flip-flop is switched by a momentary change in input signal. This momentary change is called a trigger and the transition it causes is said to trigger the flip-flop.

## ✓ Trigger of Asynchronous and synchronous flip-flops

Asynchronous flip-flops (such as basic flip-flop circuit by NAND or NOR gate i.e SR latch) require an input trigger defined by a change of signal level.

Synchronous flip-flops (such as clocked flip-flop) are triggered by pulses. A pulse starts from an initial value of 0 or 1, goes momentarily to 1 or 0, and after a short time, returns to its initial 0 or 1 value.

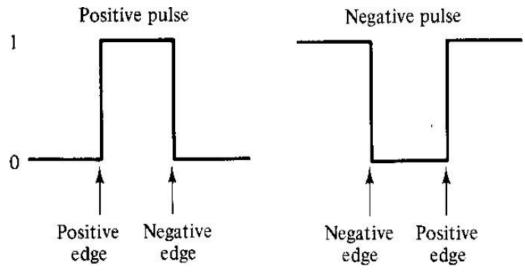


Fig. Definition of clock pulse transition.

## **Triggering of Flip-Flops**

## **✓** Multiple-transition problem in triggering of clocked flip-flops.

The clocked flip-flops (such as clocked RS, JK, D and T-flip-flops) are triggered during the positive edge of the pulses and the state transition starts as soon as the pulse reaches the logic-1 level. The new state of the flip-flop may appear at the output terminals while the input pulse is still 1. If the other inputs of the flip-flop change while the clock is still 1, the

flip-flop will start responding to these new values and a new output statemay occur i.e. multiple transition happens in one clock pulse. When this happens, the output of one flip-flop cannot be applied to the inputs of another flip-flop when both are triggered by the same clock pulse.

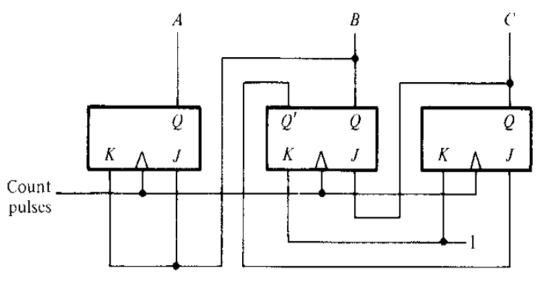
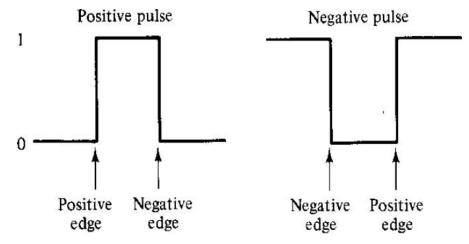


Fig. Output of flip-flop is used as input for another flip-flop.

# **Triggering of Flip-Flops**

✓ Solution of Multiple-transition problem in triggering of clocked flip-flops.

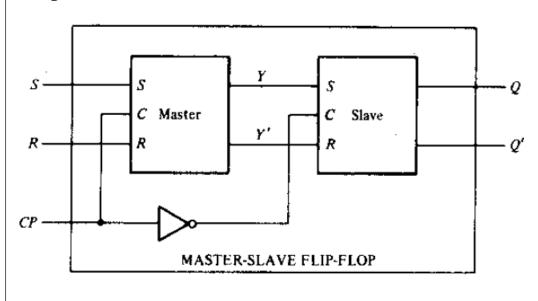
However, if we make the flip-flop respond to the positive (or negative) edge transition only, instead of the entire pulse duration then the multiple-transition problem can be eliminated.



One of the way to achieve edge triggering is to use a master-slave or edge-triggered flip-flop.

## **Master-Slave Flip-Flop**

A master-slave flip-flops is constructed from two separate flip-flops. One circuit serves as master and other as a slave, and the overall circuit is referred to as a master-slave flip-flop. Assume that the flip-flop is in the clear state prior to the occurrence of a pulse, so that Y=0 and Q=0. The input conditions are S=1, R=0. The next clock pulse should change the flip-



flop to the set state with Q=1.

Fig. Logic diagram of Master-Slave flip-flop

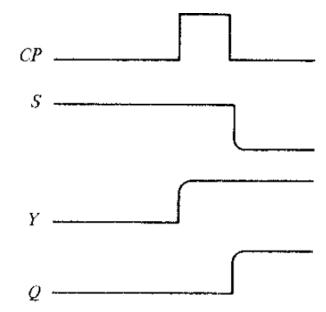


Fig. Timing Relationships Master-Slave flip-flop

## **Clocked Master-Slave JK Flip-Flop**

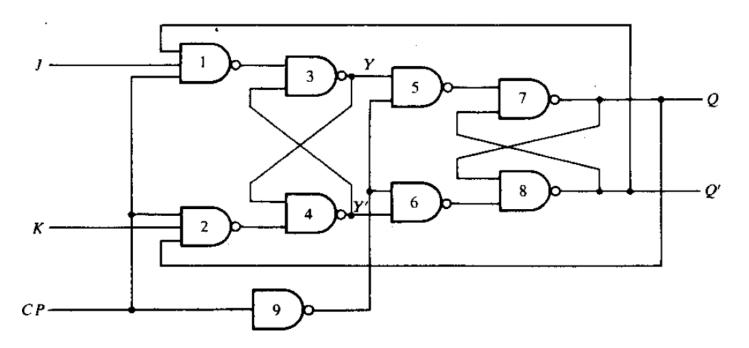


Fig. Clocked Master-Slave JK flip-flop

#### **Questions:**

- a) Draw the logic diagram (showing all gates) of a master-slave D flip-flop. Use NAND gates.
- b) Obtain the logic diagram of a master-slave JK flip-flop with AND and NOR gates.
- c) What is meant by trigger of flip-flops? Introduce the multiple transition problem in triggering of clocked flip-flops. How this problem can be solved by using a master-slave flip-flop?

The behavior of a sequential circuit is determined from the inputs, the outputs and the states of its flip-flop. Both the outputs and the next state are a function of the inputs and the present state.

The analysis of sequential circuits consists of obtaining a table (known as state table) or a diagram (known as state diagram) or boolean expression (known as state equation) that describe the behavior of sequential circuits.

**State Table:** The time sequence of inputs, outputs and flip-flop states is enumerated in a state table. It consists of three sections labeled present state, next state and output. Present state designates the states of flip-flops before clock and next state shows the state afterclock. Output section lists the values of the output variables during the present state.

**State Diagram:** The information available in a state table may be represented graphically in a state diagram.

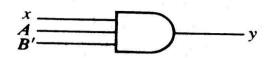
**State Equations:** A state equation (also known as an application equation) is an algebraic expression that specifies the conditions for a flip-flop state transition.

The left side of the equation denotes the next state of a flip-flop and the right side, a Boolean function that specifies the present state conditions that make the next state equal to 1

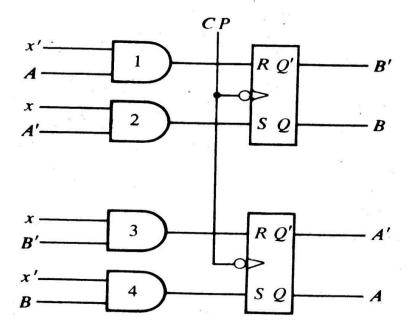
## Example of Analysis a clocked sequential circuit

#### **Question:**

Obtain the state table, state diagram and state equations of the following sequential circuit.



**Table**: State Table of the given sequential circuit



	Next	state	Output		
Present State	x = 0	x = 1	x = 0	x = 1	
AB	AB	AB	у	<u>y</u> .	
00	00	01	0	0	
δι	11.	01	0	. 0	
10 -	18	00	0	<b>1</b> 0	
. 11	10	11	Õ	0	

	Next	state	Out	tput
Present State	x = 0	x = 1	x = 0	x = 1
AB	AB	AB	у	<u> </u>
00	00	01-	0	0
δι	11.	01	0	. 0
10 -	18	00	Ô	<b>1</b> 0
. 11	10	11	0	0

## **State Equations**

According to characteristic equation of RS flip flop we get the state equation as follows:

$$A(t+1) = S+R'A=Bx'+(B'x)'A$$
 and

$$B(t+1) = S+R'B = A'x+(Ax')'B$$

#### **State Diagram**

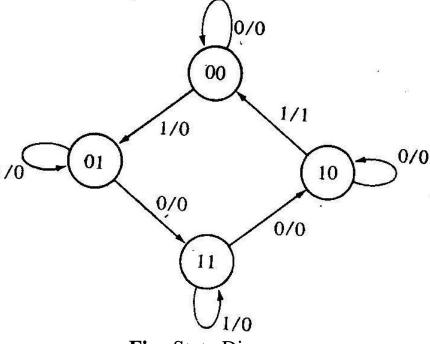
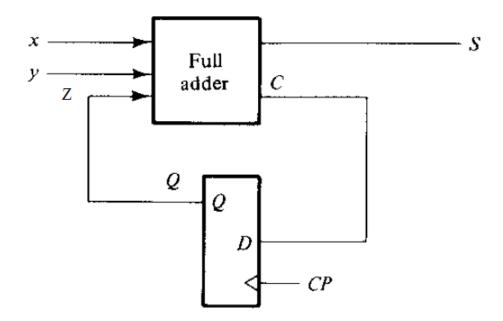


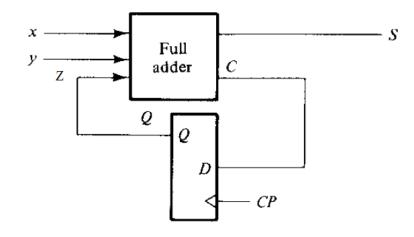
Fig: State Diagram

#### **Problem:**

The full adder shown in fig. receives two external inputs x and y; the third input z comes from the output of a D flip-flop. The carry output is transferred to the flip-flop at every clock pulse. The external S output gives the sum of x,y and z. Obtain the state table and state diagram of the sequential circuit.



#### **Solution:**



#### **State Table**

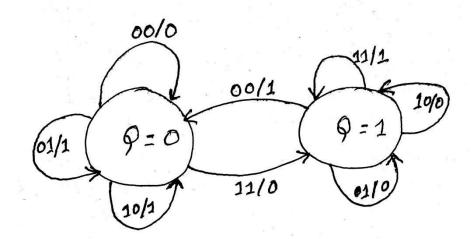
Present State	Next State			Output				
Q	x=0, y=0	x=1, y=0	x=0, y=1	x=1, y=1	x=0, y=0	x=1, y=0	x=0, y=1	x=1, y=1
	Q(t+1)	Q(t+1)	Q(t+1)	Q(t+1)	S	S	S	S
0	0	0	0	1	0	1	1	0
1	0	1	1	1	1	0	0	1

#### **Solution:**

State Table

Present State	Next State							
Q	x=0, y=0	x=1, y=0	x=0, y=1	x=1, y=1	x=0, y=0	x=1, y=0	x=0, y=1	x=1, y=1
	Q(t+1)	Q(t+1)	Q(t+1)	Q(t+1)	S	S	S	S
0	0	0	0	1	0	1	1	0
1	0	1	1	1	1	0	0	1

**State Diagram** 

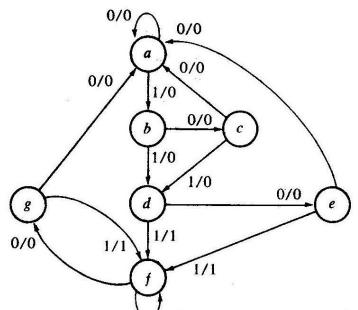


#### **State Reduction**

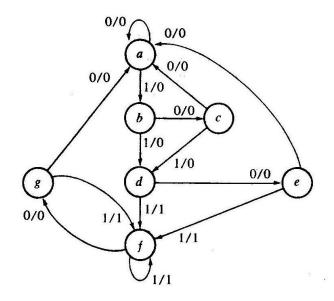
The reduction of number of flip-flops in a sequential circuit is referred to as the state reduction problem. State reduction algorithms are concerned with procedures for reducing the number of states in a state table while keeping the external input-output requirements unchanged.

#### **State Reduction Example**

Reduce the number of states of the state diagram shown in fig..



## **State Reduction Example**



### **State Table**

¥	Next	state	Output		
Present state	x = 0	x = 1	x = 0	x = 1	
<i>a</i> ,	a	ь	0	0	
- <b>b</b>	c	d	Õ	0	
c	a	d	Õ	0	
d	e	f	ő	1	
e	a	f	ő	1	
f	8	f	. 0	1	
g	<i>a</i>	f	Õ	1	

#### **State Reduction Example**

**Algorithm of state reduction:** Two states are said to be equivalent if for each member of the set of inputs, they give exactly the same output and send the circuit either to the same state or to an equivalent state.

#### **Reducing the State Table**

	Next	state	*	Ou	tput
Present state	x = 0	x = 1		x = 0	x = 1
а	а	Ь		0	0
b	c	d		0	0
c	a	d		0	0
d,	e.	£d		0	1
e	a	fd :	*	0	1
gu-	g e.	f		0	1 *
8	a	f		0	1

## **State Reduction Example**

#### **Reduced State Table**

		Nex	t state	Outp	ut
	Present state	x = 0	x = 1	x = 0	x = 1
ä	а	а	ь	0	0
	<b>b</b>	c	d	0	0
0/0	c	а	d	0	0
<b>&gt;</b>	d	e	d	0	1
0/0 0/0	e	a	d	0	1.
e b 0/0 c 1/1 1/0 1/0 1/0 1/1	Re	duced Sta	ate Diagram		

# Flip-Flop Characteristic Table

S	R	Q(t+1)	a a	J	K	Q(t+1)
0	0	Q(t)		0	0	Q(t)
0	1	0		0	1	0
1	0	1		1	0	Ĭ
1	1	?		1	. <b>.</b>	Q'(t)
(a) <i>RS</i>		(b) <i>JK</i>				
		5.				<b>4</b> / /
71 <del>-</del>	D	Q(t+1)		T	Q(t +	1)
	0	0		0	Q(t)	)
	1	1	*	1	Q'(t	)
	208	(c) D	. (3	T.	(d) T	

(d) T

# Flip-Flop Excitation Table

O(t)	O(t+1)			Q(t)	Q(t+1)		K
0	0	0	X	0	0	0	X
0	1	1	0	0	1	1	X
1	0	0	1	1	0	X	1
1	1	$\boldsymbol{X}$	0	1	1	X	0
	(a) RS				(b) <i>JK</i>		

	O(t+1)	D	Q(t)	Q(t+1)	Т
0	0	0	0	0	0
0	1	1	0	1	1
1	0	0	1	0	]
1	1	1	1	1	0

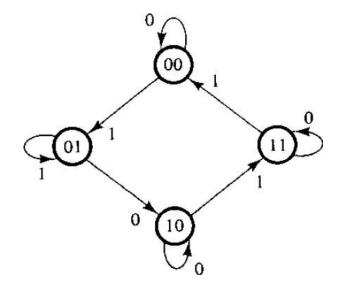
## Design Procedure of clocked Sequential Circuit

#### **Steps in Design Procedure**

- 1) Description of circuit behavior is stated. This may be accompanied by a state diagram, a timing diagram or other pertinent information.
- 2) From the given information about the circuit, obtain the state table.
- 3) The number of states may be reduced by state reduction method.
- 4) Assigned binary values to each state if the state table obtained in step 2 or 3 contains letter symbols.
- 5) Determine the number of flip-flops needed and assign a letter symbol to each. Number of flip-flops is determined from number of steps.
- 6) Choose the type of flip-flop to be used.
- 7) From the state table, derive the circuit excitation and output tables.
- 8) Using the map or any other simplification method, derive the circuit output functions and the flip-flop input functions.
- 9) Draw the logic diagram.

# **Clocked sequential circuit Design Example**

Design a clocked sequential circuit whose state diagram is given in figure.



## **Solution:**

## **Finding State Table**

			Next	State	
Present State			= 0	<i>x</i> =	: 1
A	В	Α	В	Α	В
0	0	0	0	0	1
0	1	1	0	0	1
1	0	1	0	1	1
1	1	1	1	0	0

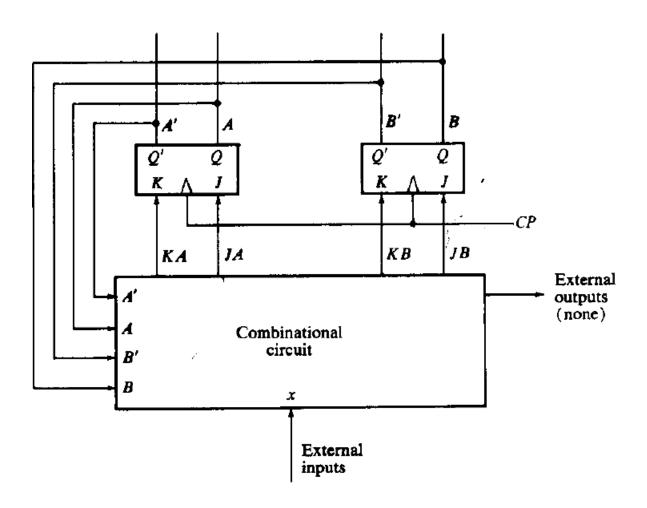
# **Clocked sequential circuit Design Example**

#### **Excitation Table**

Inputs of Combinational Circuit				Outputs of Combinational Circuit				
Pres Stat	sent e	Input	Next	State		Flip-Flo	p Input	S
A	В	X	A	В	JA	KA	JB	KB
0	0	0	0	0	0	X	0	X
0	0	1	0	ì	0	$\boldsymbol{X}$	1	$\boldsymbol{X}$
0	1	0	1	0	1	X	$\boldsymbol{X}$	1
0	1	1	0	1	0	$\boldsymbol{X}$	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	ı	$\boldsymbol{X}$
1	1	0	1	1	X	0	X	0
l	1	1	0	0	X	1	$\boldsymbol{X}$	1

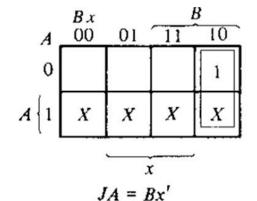
# **Clocked sequential circuit Design Example**

## **Block Diagram of sequential circuit**



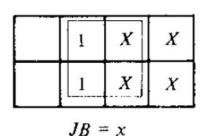
# **Design Procedure of clocked Sequential Circuit**

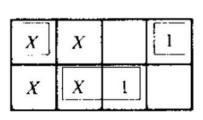
## **Maps for combinational Circuit**



X	X	X	X
		1	

KA = Bx

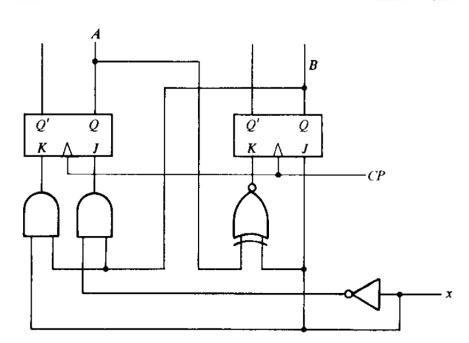




$$KB = (A \oplus x)'$$

**Logic Diagram of Sequential circuit** 





## **Design of Counters**

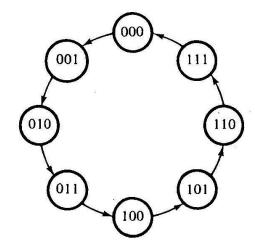
A sequential circuit that goes through a prescribed sequence of states upon the application of input pulses is called a counter

Two Types: Synchronous and Asynchronous

Synchronous: Clock pulse is same for all flip flops

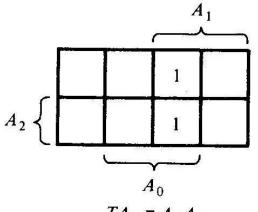
Asynchronous: Output of one flip-flop used as clock for another flip flop

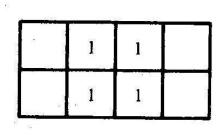
The state diagram of 3-bit counter is shown in fig. Find the logic diagram of this counter. [Use T flip-flop]



#### **Solution:**

Co	unt seque	nce	Fl	ip-flop inpi	ıts
$A_2$	$A_1$	$A_0$	$TA_2$	$TA_1$	$TA_0$
0	0	0	0	0	1
0	0	1	0	1	î
0	1	0	0	0	1
0	1	1	1	ī	i
1	0	0	0	Ô	î
1	0	1	0	ī	1
1	1	0	0	Ô	• 1
1	1	1	ī	1	î



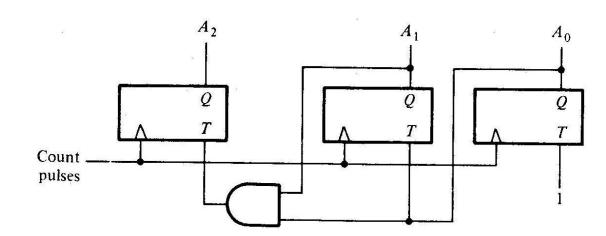


1	1	1	1
1	1	1	1

$$TA_2 = A_1 A_0 \quad .$$

$$TA_1 = A_0$$

$$TA_0 = 1$$



#### Example:

## Design a counter that has a repeated sequence of six states as listed in table

A	B	C
0	0	0
0	0	1
0	1	0
1	0	0
1	0	1
1	1	0

#### **Excitation Table for counter:**

Count sequence				Flip-flop inputs				
A	В	C	JA	KA	JB	KB	JC	KC
0	0	0	0	X	0	X	1	X
0	0	1	0	$\boldsymbol{X}$	1	X	X	1
0	1	0	1	X	X	1	0	X
1	0	0	X	0	0	X	1	X
1	0	1	X	0	ī	X	X	1
1	1	0	X	1	X	1	0	X

$$JA=B$$
  $KA=B$   $JB=C$   $KB=1$   $JC=B$ '  $KC=1$ 

$$JA=B$$
  $KA=B$   $JB=C$   $KB=1$   $JC=B$ '  $KC=1$ 

