

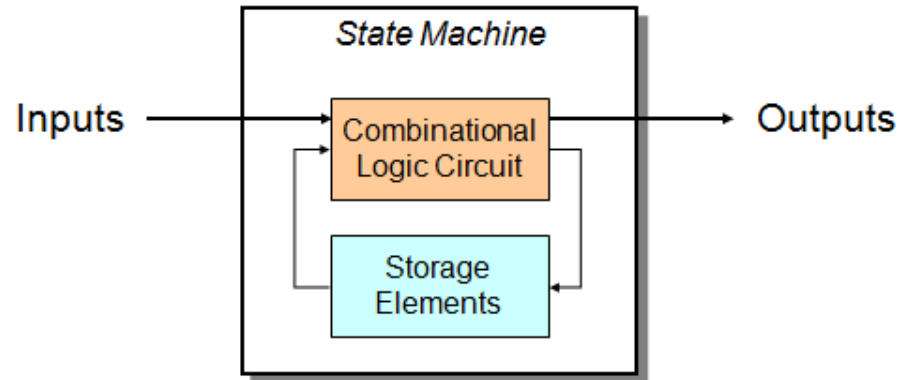
STATE MACHINES

State Machine

Another type of sequential circuit

Combines combinational logic with storage

—Remembers state, and changes output (and state) based on **inputs** and **current state**



State

The state of a system is a snapshot of all the relevant elements of the system at the moment the snapshot is taken.

Examples:

The state of a basketball game can be represented by the scoreboard.

Number of points, time remaining, possession, etc.

The state of a tic-tac-toe game can be represented by the placement of X's and O's on the board.

STATE MACHINES

STATE TABLES AND STATE DIAGRAMS

In this model the effect of all previous inputs on the outputs is represented by a state of the circuit. Thus, the output of the circuit at any time depends upon its current state and the input. These also determine the next state of the circuit. The relationship that exists among the inputs, outputs, present states and next states can be specified by either the **state table** or the **state diagram**.

State Table

The state table representation of a sequential circuit consists of three sections labeled *present state*, *next state* and *output*. The present state designates the state of flip-flops before the occurrence of a clock pulse. The next state shows the states of flip-flops after the clock pulse, and the output section lists the value of the output variables during the present state.

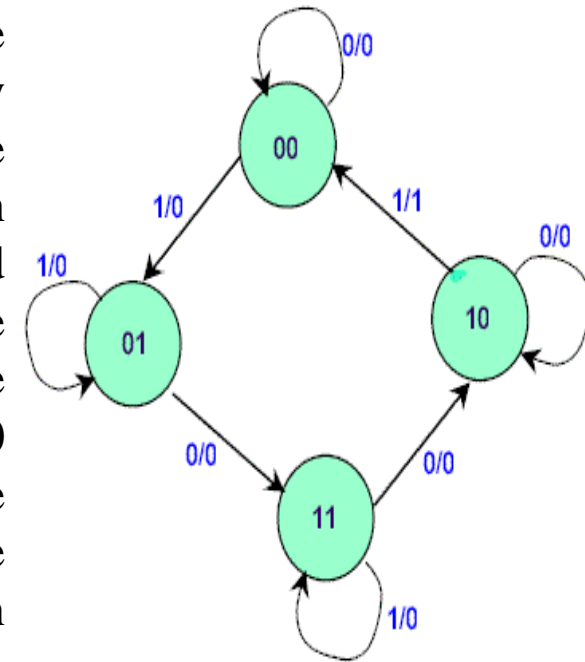
Present State	Next State		Present Output
	X=0	X=1	
a	d	c	0
b	d	c	0
c	d	a	0
d	d	c	1

STATE MACHINES

State Diagram

In addition to graphical symbols, tables or equations, flip-flops can also be represented graphically by a state diagram. In this diagram, a state is represented by a circle, and the transition between states is indicated by directed lines (or arcs) connecting the circles.

The binary number inside each circle identifies the state the circle represents. The directed lines are labelled with two binary numbers separated by a slash (/). The input value that causes the state transition is labelled first. The number after the slash symbol / gives the value of the output. For example, the directed line from state 00 to 01 is labelled 1/0, meaning that, if the sequential circuit is in a present state and the input is 1, then the next state is 01 and the output is 0. If it is in a present state 00 and the input is 0, it will remain in that state. A directed line connecting a circle with itself indicates that no change of state occurs. The state diagram provides exactly the same information as the state table and is obtained directly from the state table.

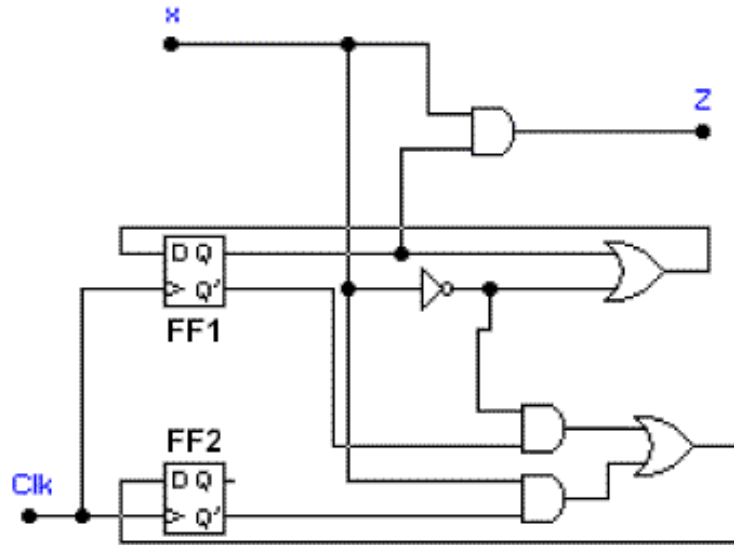


State Diagram

STATE MACHINES

Example:

Consider a sequential circuit



The behavior of the circuit is determined by the following Boolean expressions:

$$Z = x * Q1$$

$$D1 = x' + Q1$$

$$D2 = x * Q2' + x' * Q1'$$

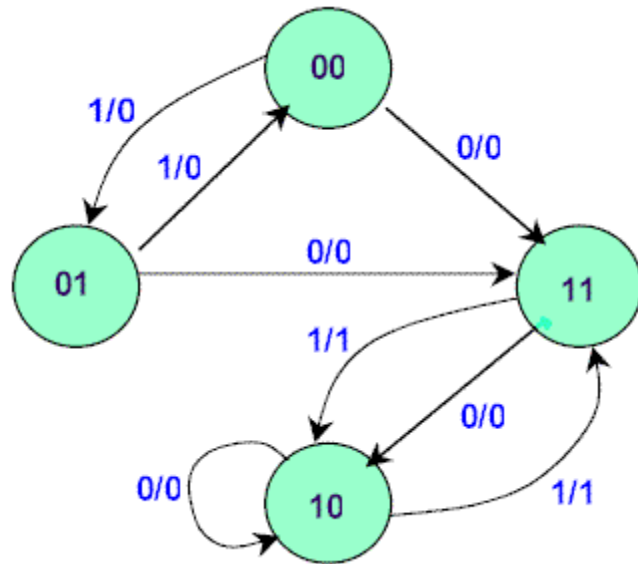
These equations can be used to form the state table. Suppose the present state (i.e. $Q1Q2$) = 00 and input $x = 0$. Under these conditions, we get $Z = 0$, $D1 = 1$, and $D2 = 1$. Thus the next state of the circuit $D1D2 = 11$, and this will be the present state after the clock pulse has been applied. The output of the circuit corresponding to the present state $Q1Q2 = 00$ and $x = 1$ is $Z = 0$. This data is entered into the state table as shown in Table 2.

STATE MACHINES

State table for the sequential circuit

Present State Q1Q2	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
0 0	1 1	0 1	0	0
0 1	1 1	0 0	0	0
1 0	1 0	1 1	0	1
1 1	1 0	1 0	0	1

The state diagram for the sequential circuit



STATE MACHINES

state diagrams of the four types of flip-flops

NAME	STATE DIAGRAM
SR	<pre> graph LR Q0((Q = 0)) Q1((Q = 1)) Q0 -- "S,R=0,0" --> Q0 Q1 -- "S,R=0,0" --> Q1 Q0 -- "S,R=1,0" --> Q1 Q1 -- "S,R=0,1" --> Q0 </pre>
JK	<pre> graph LR Q0((Q = 0)) Q1((Q = 1)) Q0 -- "J,K=0,0" --> Q0 Q1 -- "J,K=0,0" --> Q1 Q0 -- "J,K=1,0 or 1,1" --> Q1 Q1 -- "J,K=0,1 or 1,1" --> Q0 </pre>
D	<pre> graph LR Q0((Q = 0)) Q1((Q = 1)) Q0 -- "D=0" --> Q0 Q1 -- "D=1" --> Q1 Q0 -- "D=1" --> Q1 Q1 -- "D=0" --> Q0 </pre>
T	<pre> graph LR Q0((Q = 0)) Q1((Q = 1)) Q0 -- "T=0" --> Q0 Q1 -- "T=0" --> Q1 Q0 -- "T=1" --> Q1 Q1 -- "T=1" --> Q0 </pre>

STATE REDUCTION

State Reduction

Any design process must consider the problem of minimising the cost of the final circuit. The two most obvious cost reductions are reductions in the number of flip-flops and the number of gates.

The number of states in a sequential circuit is closely related to the complexity of the resulting circuit. It is therefore desirable to know when two or more states are equivalent in all aspects. The process of eliminating the equivalent or redundant states from a state table/diagram is known as **state reduction**.

Example: Let us consider the state table of a sequential circuit

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
A	B	C	1	0
B	F	D	0	0
C	D	E	1	1
D	F	E	0	1
E	A	D	0	0
F	B	C	1	0

State table

STATE REDUCTION

It can be seen from the table that the present state A and F both have the same next states, B (when $x=0$) and C (when $x=1$). They also produce the same output 1 (when $x=0$) and 0 (when $x=1$). Therefore states A and F are equivalent. Thus one of the states, A or F can be removed from the state table. For example, if we remove row F from the table and replace all F's by A's in the columns, the state table is modified

Present State	Next State		Output	
	$x = 0$	$x = 1$	$x = 0$	$x = 1$
A	B	C	1	0
B	A	D	0	0
C	D	E	1	1
D	A	E	0	1
E	A	D	0	0

State F removed

It is apparent that states B and E are equivalent. Removing E and replacing E's by B's results in the reduce table

STATE REDUCTION

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
A	B	C	1	0
B	A	D	0	0
C	D	B	1	1
D	A	B	0	1

Reduced state table

The removal of equivalent states has reduced the number of states in the circuit from six to four. Two states are considered to be **equivalent** if and only if for every input sequence the circuit produces the same output sequence irrespective of which one of the two states is the starting state.

FSM EXAMPLES

EXAMPLE #2

- A sequential circuit is defined by the following Boolean functions with input X , present states P_0 , P_1 , and P_2 , and next states N_0 , N_1 , and N_2 .
 - $N_2 = X(P_1 \oplus P_0) + \overline{X}(\overline{P_1 \oplus P_0})$
 - $N_1 = P_2$
 - $N_0 = P_1$
 - $Z = XP_1P_2$
- Derive the state table.
- Derive the state diagram.

FSM EXAMPLES

EXAMPLE #2

- The state table is formed as follows.

Present State			Input	Next State			Output
P ₂	P ₁	P ₀	X	N ₂	N ₁	N ₀	Z
0	0	0	0	1	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	0	1	0
0	1	0	1	1	0	1	0
0	1	1	0	1	0	1	0
0	1	1	1	0	0	1	0
1	0	0	0	1	1	0	0
1	0	0	1	0	1	0	0
1	0	1	0	0	1	0	0
1	0	1	1	1	1	0	0
1	1	0	0	0	1	1	0
1	1	0	1	1	1	1	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	1

FSM EXAMPLES

EXAMPLE #2

- The state diagram can be drawn as follows.

