- *The 8085 microprocessor has 5 basic machine cycles. They are*

1. Opcode fetch cycle (4T)

2. Memory write cycle (3T)

3. I/O read cycle (3T)

4. Memory read cycle (3T)

5. I/O write cycle (3T)

Some more machine cycles for 8085:

- *1. Interrupt Acknowledge*
- *2. Bus Idle*

8085 Machine Cycles

The three status signals IO/M*, S1 and S2 identify each type

Machine Cycle	Status			Control		
	$IO/\overline{M}$	S_1	S_0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
Opcode Fetch	0	1	1	0	1	1
Memory Read	0	1	0	0	1	1
Memory Write	0	0	1	1	0	1
I/O Read	1	1	0	0	1	1
I/O Write	1	0	1	1	0	1
INTR Acknowledge	1	1	1	1	1	0
Bus Idle	0	0	0	1	1	1

Signal Timings

ALE

- *This signal is active high signal. It is activated in the beginning of T1 state of each machine cycle except bus idle machine cycle and it remains active in the T1*

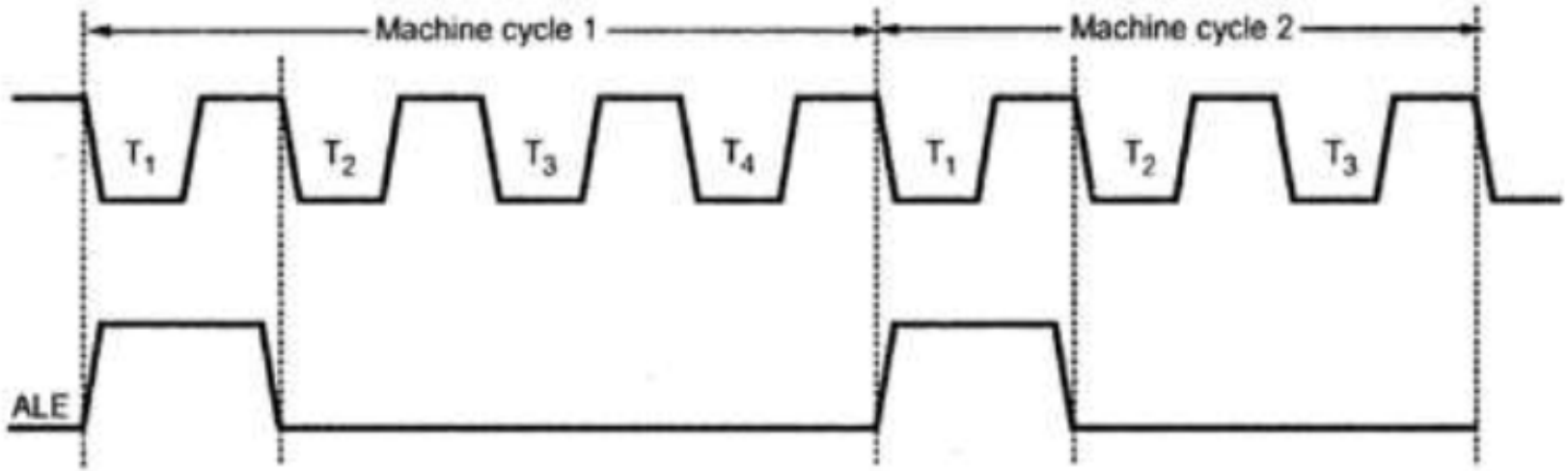


Fig. 1.22 ALE activation and its period

- ***D0 - D7 (Data Bus)***

The data from memory or I/O device and from microprocessor to memory or I/O device is transferred during T2 and T3 – states.

N.B: In read machine cycle, data will appear on the data bus during the later part of the T2 - state as shown

in fig. (next slide).

This is because to read data from memory or I/O device it is necessary to select memory or I/O device, after the selection, device will put the data from the selected location on the data bus. This action needs finite time. This time is referred as “Access Time”

- ***A0 - A7 (Lower Byte Address)***

This is available on the multiplexed address/data bus (AD0 - AD7) during T1 state of each machine cycle except bus idle machine cycle.

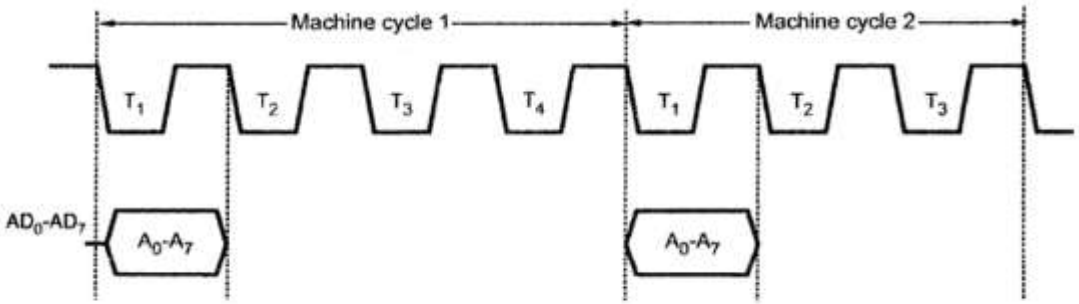


Fig. 1.23 Lower address on the multiplexed bus

Timing diagram of memory read cycle

Primary Function of memory interfacing is that the microprocessor should be able to read from and write into a given register of a memory chip:

- Select the Chip
- Identify the register
- Enable the appropriate buffer.

Timing Diagram of 8085 Memory Read/Write Machine Cycle allows to understand microprocessor interfacing concepts.

MEMR and MEMW are given to RD and WR pins of Memory chip.

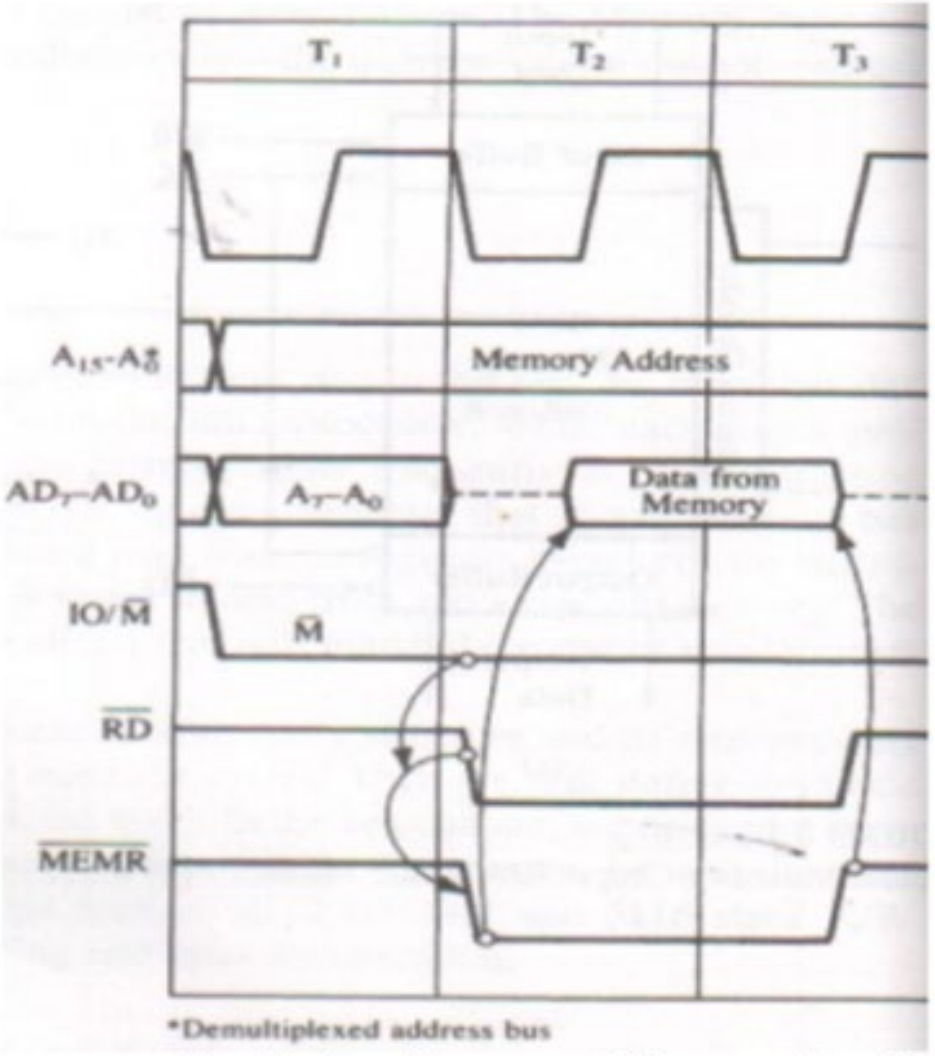
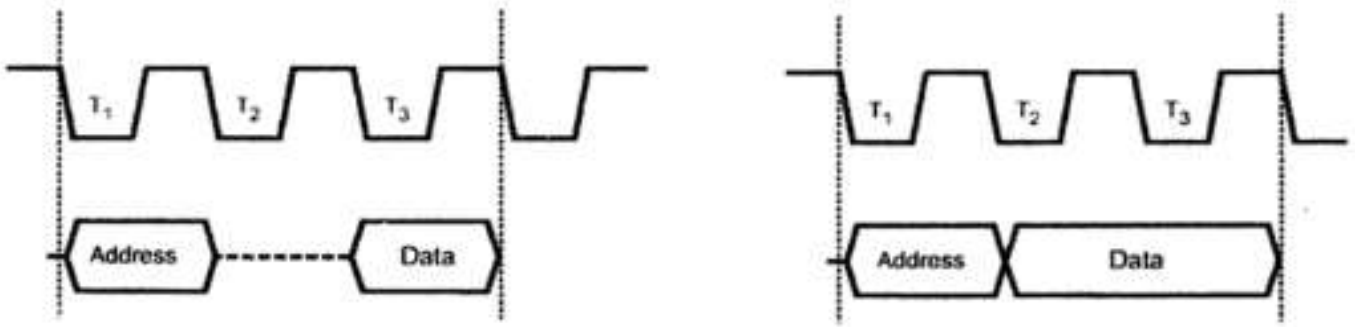


Fig: Timing Diagram of Memory Read Cycle

- ***D0 - D7 (Data Bus)***

In case of write cycle, data is available in the register set of the microprocessor and it can put that data on the data bus with zero access time.



(a) **Fig. 1.24 Data bus** (b)

- ***A8 - A15 (Higher Byte Address)***

The higher byte of address is available on the A8 –A15 bus during T1, T2, and T3 – state of each machine cycle, except bus idle machine cycle.

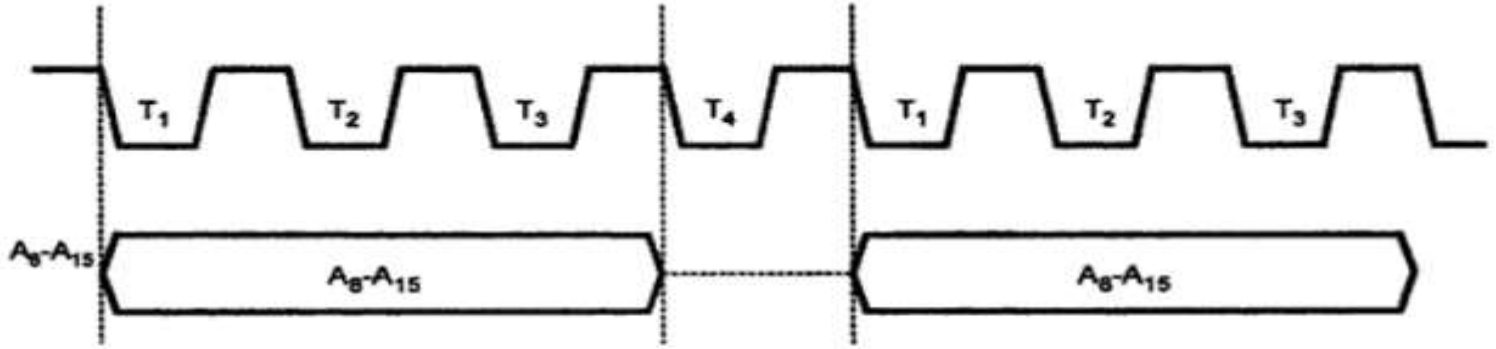


Fig. 2.29 Higher byte address on A8-A15

- ***IO/M*, S0, S1:*** ***These are called status signals. They decide the type of machine cycle to be executed. They are activated at the beginning of T1 – state of each machine cycle and remain active till the end of the machine cycle.***

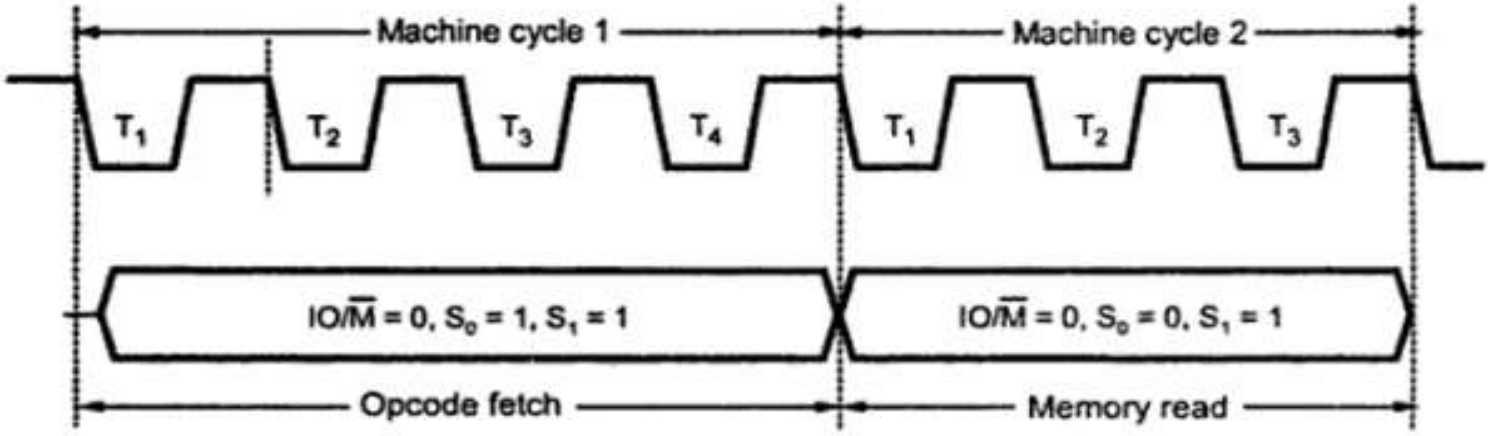


Fig. 2.30 Status signals

- ***RD* and WR* ('*' here denotes Bar)***

These decide the direction of the data transfer.

When RD* signal is active, data is transmitted from memory or I/O device to microprocessor.

When WR* signal is active, data is transmitted

from microprocessor to the memory or I/O device.

Both signals are never active at a time.

*****And since the data transfer in 8085 takes place during T2 and T3, these signals are activated during T2 and T3 as shown in the next slide***

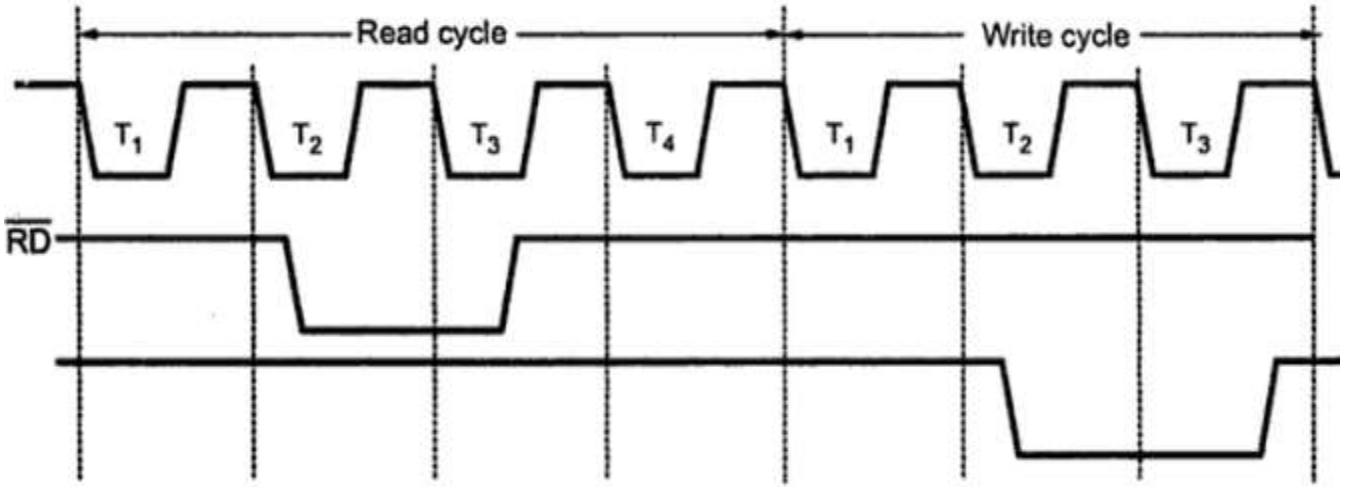
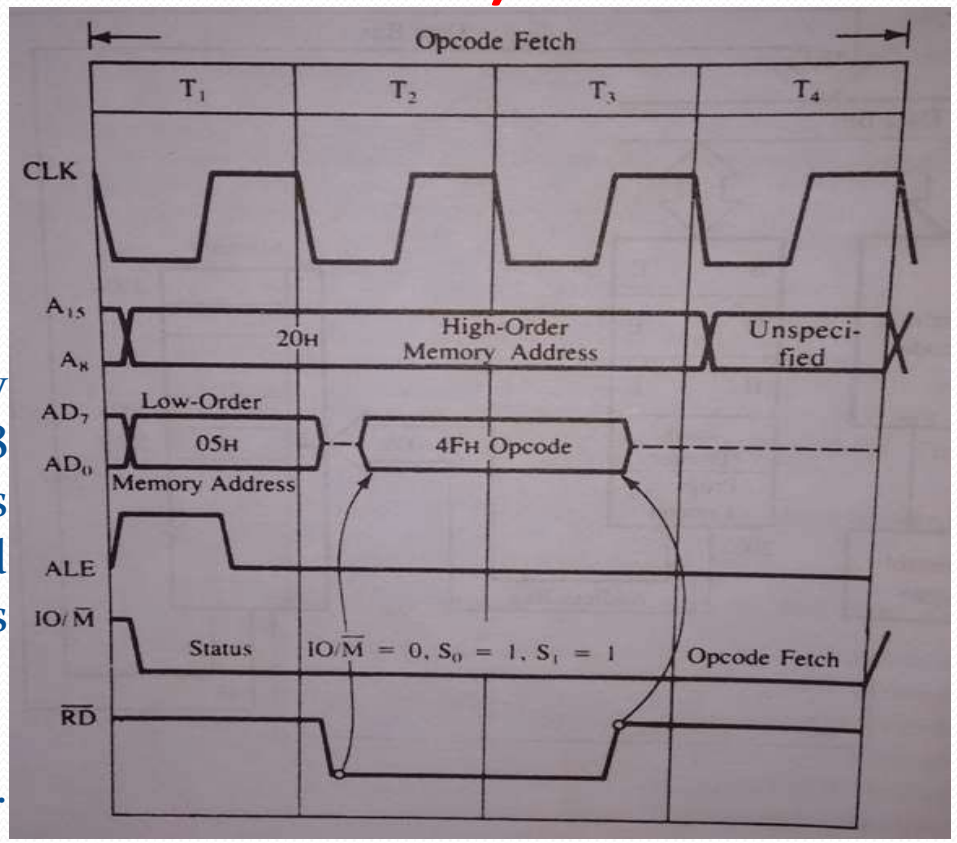


Fig. 2.31 $\overline{RD}$ and $\overline{WR}$ signals

Timing: Transfer of byte from memory to MPU(OPCODE FETCH)

- **How a data byte is transfer from memory to the MPU.**
- **It shows the five different group of signals with clock**



Step 1: At T1 higher order memory address 20H is placed on the A15 – A8 and the lower order memory address 05H is placed on the bus AD7-AD0, and ALE signal high. IO/M goes low(memory related signal).

Step 2: During T2 RD signal is sent out. RD is active during two clock periods.

Step 3 : During T3, Memory is enabled then instruction byte 4FH is placed on the data bus and transferred to MPU. When RD goes high it causes the bus to go into high impedance state.

Step 4: During T4, the machine code or byte is decoded by the instruction decoder and content of A is copied into register.

Timing diagram of memory write cycle

- 8085 places 16-bit address on address bus, and with this address only one register should be selected (only 11 low order address lines are required). Internal decoder of chip will identify and select the register for EPROM.

- Remaining 8085 address lines (A15-A11) should be decoded to generate chip select.

- 8085 provides two signal-IO/M' and RD'– to indicate that is memory read operation MEMR'. MEMR' control signal that can be used to enable output buffer by connecting to memory signal RD'. (Similarly signal-IO/M' and WR'– indicates memory write operation MEMW').

- Memory places data byte from address register during T2 and that is read by the microprocessor before the end of T3.

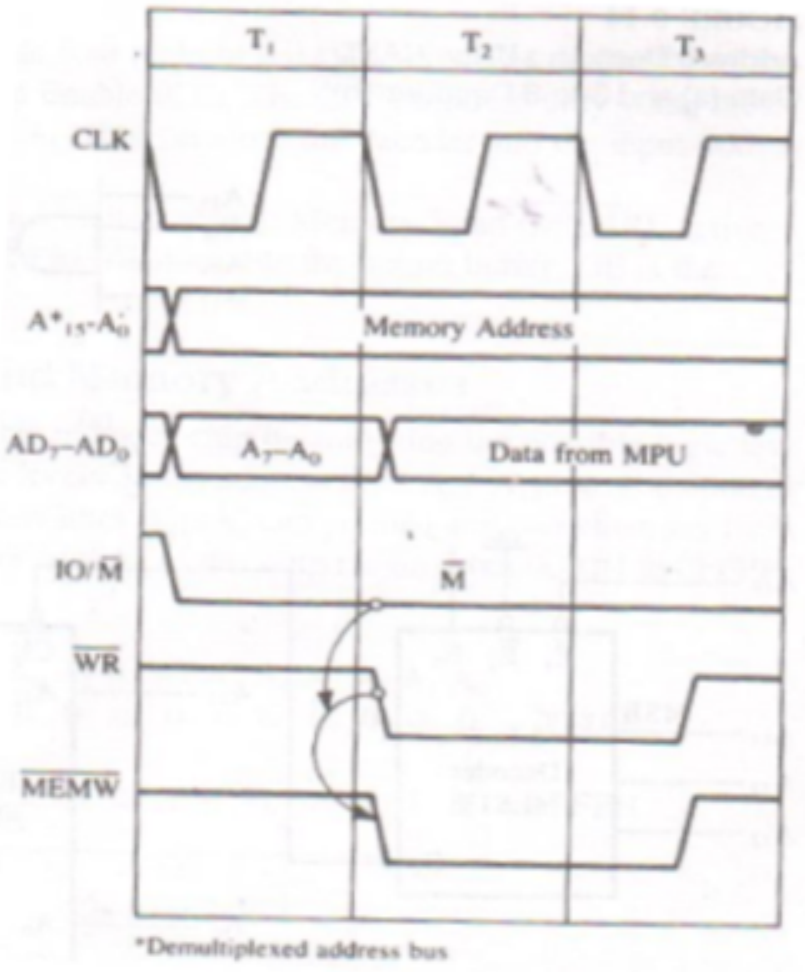
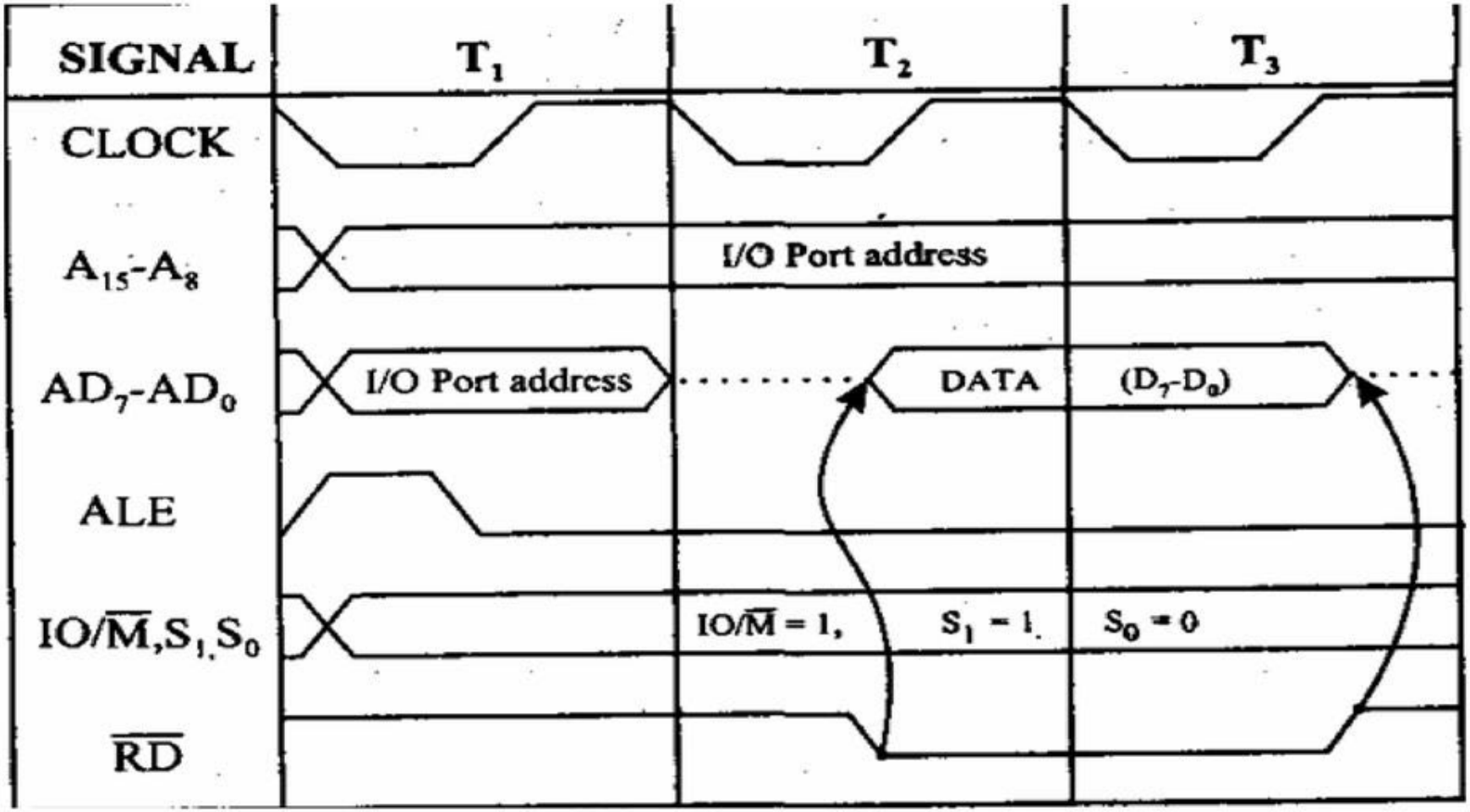


Fig: Timing Diagram of Memory Write Cycle

I/O READ CYCLE OF 8085



I/O WRITE CYCLE OF 8085