95µW 802.11g/n Compliant Fully-Integrated Wake-Up Receiver with -72dBm Sensitivity in 14nm FinFET CMOS

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***Abstract*—A 2.4GHz fully-integrated Wi-Fi compliant wake-up receiver in 14nm FinFET technology is presented. The receiver achieves -72dBm sensitivity and +20dBr adjacent channel interference rejection for 62.5kbps at 10^{-3} BER while consuming 95µW. The OOK-modulated wake-up packet can be transmitted using any legacy OFDM Wi-Fi transmitter.**

***Index Terms*—wake-up receiver, 802.11, FinFET, Wi-Fi**

I. Introduction

Seamless connectivity is becoming a necessity in many battery-powered applications, such as wireless sensor networks (WSN), Internet of Things (IoT), and wearables. As radios typically play a dominant factor in power consumption, it is very crucial to have ultra-low power solutions in these systems. Operating the radio only when necessary is an effective power saving technique but unscheduled protocols such as those used in legacy IEEE 802.11 devices suffer from the uncertainty of when the next message will be transmitted. Event-driven radios such as ultra-low-power (ULP) wake-up receivers (WuRX) can overcome this trade-off by constantly monitoring the wireless channel with significantly less power consumption and turning on the main radio only when needed.

In order to meet the link budget with limited power, published ULP WuRXs widely use High-Q off-chip components such as SAW/BAW filters [1]-[4], inductors [5][6], and crystal oscillators [6][7]. While power levels within the vicinity of 100µW can be achieved, these bulky and costly components limit the integration, hence dense deployments and use cases. This work presents a fully-integrated, highly scaled, 802.11g/n compliant wake-up receiver design in 14nm FinFET CMOS requiring only a 32kHz Real Time Clock (RTC) reference, readily available in many digital platforms. This receiver can be utilized along with any legacy Wi-Fi transmitter without changing any hardware.

Section II presents the improvement in power saving compared to the existing 802.11 power saving modes. Section III explains how to generate a wake-up packet using a legacy Wi-Fi OFDM transmitter. Section IV discusses the proposed WuRX architecture. Section V presents the measurement results and Section VI concludes the paper.

II. 802.11 Power Saving Modes vs WuRX

Figure 1 explains the techniques such as PS-Poll (power save polling), U-APSD (unscheduled automatic power save delivery), and TWT (target wake time) which are utilized as power saving modes in current 802.11 protocols. In PS-Poll, the station (client) wakes up periodically to receive the beacon frames and check for incoming data. In U-APSD, the station wakes up periodically to transmit a trigger frame to the access point (AP) to see if there is data to receive. In TWT, the AP tells the station the next target wake-up time during the current packet exchange but this does not guarantee that there will be new data when the wake-up time comes. Although the algorithms vary, each scheme relies on turning the main radio off for a certain period of time and then turning back on periodically to monitor the channel, even when there is no data to receive. The longer the off-period is, the higher the power saving can be, at the expense of longer latency if there is data to be received.

The WuRX can break the latency/power trade-off by constantly monitoring the channel with very low power consumption and turning the main radio on immediately if data is available as shown in Figure 1 (LP-WUR). Power saving can be further improved if the WuRX is also duty-cycled as shown in Figure 1 (LP-WUR with TWT). Figure 2 shows the estimated power saving gain based on the 802.11ax Task Group power consumption models [8][9] for different latency requirements assuming a WuRX with 100µW active power. Orders of magnitude of gain can be achieved if the latency requirement is kept small.

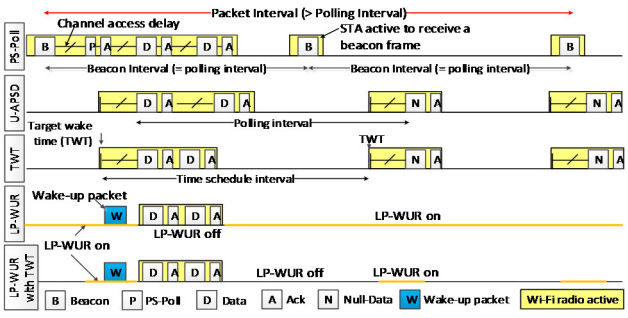

Fig. 1 Power saving modes in 802.11 and WuRX operation.

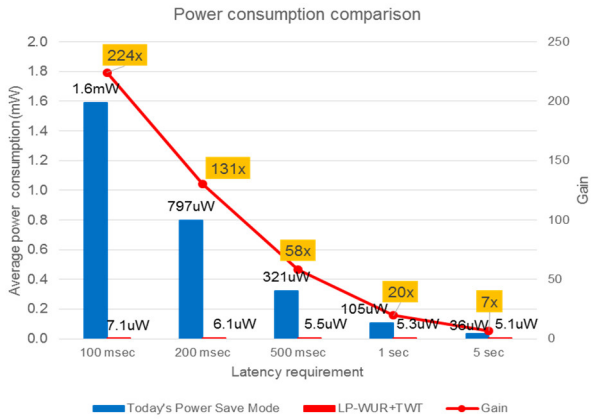

Fig. 2 Power saving gain based on 802.11ax TG power consumption model [8][9].

III. Wi-Fi Compliant Wake-Up Packet Design

Simple modulation schemes like non-coherent OOK [1]-[5] or GFSK [7] are commonly utilized in WuRX implementations, but a typical Wi-Fi transmitter does not support these modulation schemes unless the hardware is changed, which can complicate backward compatibility. However, an existing Wi-Fi transmitter firmware can be easily modified to mimic these modulations. OOK data sequence can be implemented as an OFDM signal by individually modulating some or all of the subcarriers. Similarly, different types of FSK modulations can also be implemented by activating the subcarriers sequentially from low-to-high or high-to-low frequencies.

The wake-up packet can be incorporated into an existing 802.11 packet as a payload after the legacy 802.11 preamble. Once the AP sends the preamble, which includes the length of the entire packet, the wireless medium can be secured from neighboring 802.11 devices. Following the legacy 802.11 preamble, the OOK modulated packet is sent. This contains the wake-up preamble, the MAC header, the frame body and a frame check sequence. This will wake-up the target station while appearing as noise for all the other stations without a WuRX.

The wake-up packet does not need to occupy the entire bandwidth of the acquired Wi-Fi channel. In this design, 4MHz RF bandwidth centered in the 20MHz Wi-Fi channel is allocated for the WuRX signal. The 8MHz spacing from the adjacent channels on either side is used as guard band to improve the receiver Adjacent-Channel-Interference (ACI) rejection.

IV. Wake-Up Receiver Architecture

Figure 3 presents the block level diagram of the proposed fully-integrated receiver architecture. To meet the target power budget of 100µW [5], a mixer-first architecture is selected, since it is not possible to achieve enough RF gain within this power budget without using very high-Q, external components. Input matching is implemented using a step-up integrated LC network with 1nH inductor rather than a 50ohm resistor as it provides inherent voltage gain at the receiver input and reduces the noise figure (NF).

Three fully-differential single-stage amplifiers with real output poles are used for baseband amplification and filtering. Due to the limited gain in the front-end, NF is dominated by the noise of the baseband amplifiers. It was not possible to meet the target NF with the 100µW power budget using conventional gain stages. In order to relax this noise/power trade-off, a switched-capacitor voltage multiplier with an ideal gain of 5 is implemented in this design. The kT/C noise in the multiplier can be optimized by sizing the capacitors. Technology scaling helps reducing power consumption required to drive the multiplier switches. With this additional gain, power consumption can be kept small in the following gain stages without significant impact on the NF. An additional buffer drives a low-power 6-bit SAR ADC to digitize the incoming data. The demodulation is done in the digital domain using an adaptive threshold detection algorithm. This approach gives more flexibility compared to an analog peak detector and again benefits from technology scaling.

LO signal is generated with a resistively starved ring-oscillator frequency-locked to an external 32kHz RTC. An LC oscillator is not feasible within the power budget due to

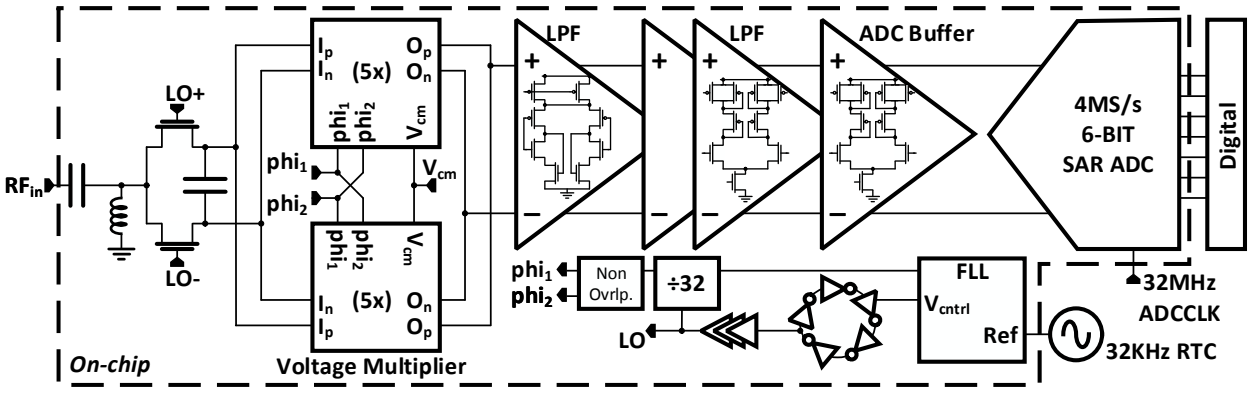

Fig. 3 Block level diagram of the proposed wake-up receiver.

limited L·Q product for on-chip inductors requiring too large current to maintain the oscillation.

A. Passive Mixer and Capacitive Voltage Multiplier

Figure 4 presents the receiver front-end. Mixer is a single-balanced voltage-mode NMOS passive mixer with a capacitive load to create RF filtering by translational pole [10]. Voltage multiplier provides level shifting to required input common mode voltage for the baseband amplifiers (V_{cm}). The common mode shift occurs only at the output nodes while all other nodes stay around 0V to minimize switch on-resistance. The multiplier block is optimized to minimize the effect of the parasitic capacitance at the top and bottom plates of the capacitors which reduces the effective voltage gain.

One potential drawback of the multiplier is the folding of the spectral content at integer multiples of the clock frequency into the baseband signal. To avoid ISM band blocker folding, the clock frequency is set at 1/32 of the carrier frequency. Moreover, a ping-pong architecture is used to double the effective folding frequency.

B. VCO and FLL

The starved 5-stage ring oscillator schematic along with the FLL is provided in Figure 5. Resistors are realized with devices in triode and are used for coarse frequency tuning. Fine tuning in the FLL is done by a varactor implemented with an open source NMOS for better C_{on}/C_{off} ratio.

The starved VCO output is buffered to create rail-to-rail swing and then is divided by 32 using low-power TSPC flip-flops. Measured phase noise is -65dBc/Hz @ 1MHz offset for 2.4GHz carrier and the measured LO leakage at the receiver input is -95dBm. The programmable divider output is compared with the reference clock and the charge pump is updated accordingly. For faster settling, instead of a bang-bang PFD approach, a period difference based charge pumping is utilized (see timing diagram in Fig. 5). An external 32kHz RTC is used as the reference rather than a crystal oscillator due to power constraints. Frequency instead of phase lock is preferred since the very small loop bandwidth (~3kHz) required to make a conventional PLL stable with such low reference frequency would have dictated very large filter components which are hard to realize on chip. Moreover, given the OOK modulation scheme, phase coherence is not required and very low-power RTC can be used as reference.

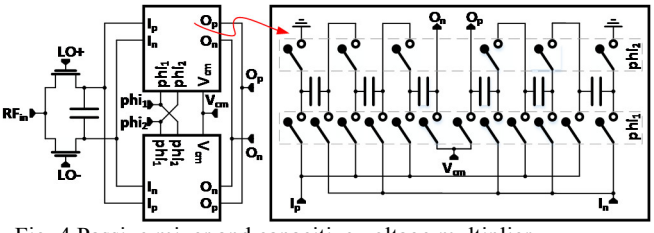

Fig. 4 Passive mixer and capacitive voltage multiplier.

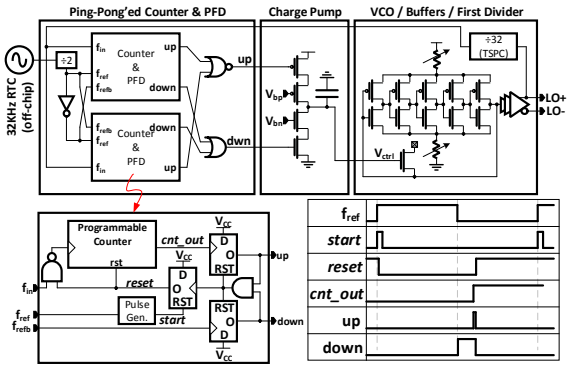

Fig. 5 FLL and VCO Schematic with timing diagram.

C. Baseband Amplifiers

Figure 6 shows the schematic of the baseband amplifiers. The first stage [Fig. 6(a)] is an inverter-based design with local common mode feedback and the latter stages are differential amplifiers with diode connected loads [Fig. 7(b)]. The second diode connected load can be bypassed using V_{gain_ctrl} signal to control the gain. The same stage with different sizing/biasing is also used as a buffer to drive the ADC. Output real poles in each stage are adjusted to create an overall 2MHz baseband bandwidth.

V. Measurement Results

Proposed design is fabricated in 14nm FinFET CMOS technology and occupies 0.19mm^2 including the front-end passive network (Fig. 7). 32MHz ADC clock is applied externally for testing purposes but it can be easily generated internally from the VCO output. The measured BER vs input power is shown in Figure 8. The RX achieves -72dBm sensitivity with a data rate of 62.5 kbps (including ¼ coding) for a BER of 10^{-3}. Measured ACI rejection is +20dBr (for 3dB de-sense) when a standard 20MHz OFDM Wi-Fi data is applied to the adjacent channel. With a wake-up packet length after the preamble of 32 bits, with 16-bit MAC header (address field), 8-bit frame body and 8-bit frame check sequence (CRC), PER is about 6.5% at sensitivity. This effectively corresponds to the miss-detection probability. False alarm rate is much lower thanks to the 8-bit CRC at the end of the wake-up packet.

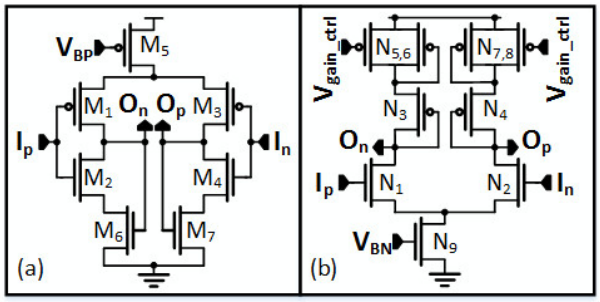

Fig. 6 Baseband Amplifiers (a) First stage, (b) Latter stages.

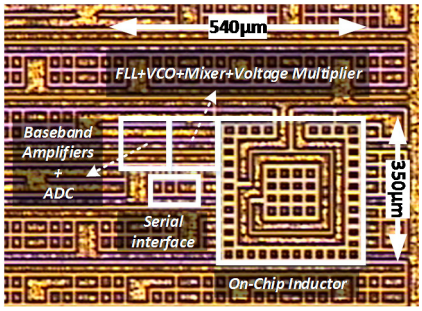

Fig. 7 Chip microphotograph.

S11 is better than -10dB in the desired band and the overall receiver gain is 37dB with a -3dB bandwidth of 3MHz (Fig. 8). The receiver dissipates 95µW from 0.95V supply. Table I summarize the power break-down for the different blocks, while Table II compares this design to current state-of-the-art.

VI. Conclusion

A fully-integrated, Wi-Fi compliant wake-up receiver in 14nm FinFET CMOS technology is presented. The wake-up packet is designed using OOK-on-OFDM based modulation scheme which can be transmitted by any legacy Wi-Fi OFDM transmitter. The receiver does not require any off-chip components and uses a low-power 32kHz RTC as the reference. It achieves -72dBm sensitivity for 10^{-3} BER at 62.5kbps while dissipating 95µW.

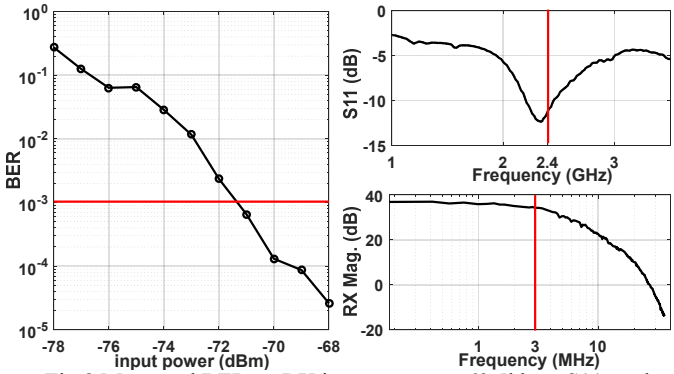

Fig.8 Measured BER vs RX input power at 62.5kbps, S11, and receiver magnitude response.

TABLE I
Wake-Up Receiver Power Breakdown

VCO	FLL + Voltage Mult.	Baseband Amplifiers	ADC
23µW	32µW	18µW	22µW

Acknowledgments

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TABLE II
State-Of-The-Art Comparison for Wake-Up Receivers

	This Work	[1]	[2]	X. Huang ISSCC'10	S. Drago ISSCC'10	[3]	J. Pandey ISSCC'11	[4]	C. Bryant ESSCIRC'14	[7]	[5]
Tech. [nm]	**14**	90	90	90	65	90	130	90	65	65	65
Carrier Freq. [GHz]	**2.4**	1.9	2	2.4/0.915	2.4	0.915	0.402	0.915	2.45	0.924	2.4
Data Rate [kbps]	**62.5**	40	100	100	500	10	200	10	250/650	50	10/50
Sensitivity [dBm]	**-72**	-50	-72	-64/-75	-82	-86	-70/-90	-56/-83	-88/-71	-87	-97/-92
Power [µW]	**95**	65	52	51	415	123	44/120	63/120	50	45.5	99
Supply [V]	**0.95**	0.5	0.5	0.5/1	1.2	1	1	1	0.75	0.7	0.5
Modulation	**OOK**	OOK	OOK	OOK	PPMIR	OOK	FSK	OOK	OOK	GFSK	OOK
LO Generation	**Ring with FLL**	Not required	Ring w/o PLL	Not required	Duty-cycled ring with PLL	Not required	Inj. locked ring	32MHz external	Ring w/o PLL	Ring+LC-DCO with PLL	LC-DCO w/o PLL
Required External Components	**32kHz RTC**	BAW filter	BAW filter Clock for calibration	High-Q inductor 20MHz clock	10MHz reference clock	SAW filter 2MHz clock	High-Q matching 44.5MHz inj. Clock	SAW filter 32MHz IF clock	Tunable resistor Clock	Matching network 32kHz crystal	High-Q inductors Clock for calibration