

Millimeter-Wave Transceivers for Wireless Communication, Radar, and Sensing

(Invited Paper)

Aritra Banerjee^{1, #}, Kristof Vaesen², Akshay Visweswaran², Khaled Khalaf², Qixian Shi², Steven Brebels², Davide Guermandi², Cheng-Hsueh Tsai^{2, 3}, Johan Nguyen^{2, 3}, Alaa Medra^{2, 3, 4}, Yao Liu², Giovanni Mangraviti², Orges Fuxrhi¹, Bert Gyselinckx¹, Andre Bourdoux², Jan Craninckx², Piet Wambacq^{2, 3, *}
¹imec USA Nanoelectronics Design Center, Kissimmee, Florida, USA; ²imec, Leuven, Belgium;
³Department of Electronics and Informatics, Vrije Universiteit Brussel, Belgium; ⁴Qualcomm, San Diego, CA, USA
Email: #aritra.banerjee.1987@ieee.org, *Piet.Wambacq@imec.be

Abstract—Due to growing demand for higher data rates in wireless communication, high resolution requirement in radars, and emerging sensing applications, mm-wave frequency bands have become very attractive in recent years. Architectures and circuits of mm-wave transceivers are described and comparison of process technologies for mm-wave IC design is presented. Critical mm-wave circuit blocks and example implementations such as 60 GHz phased array, 28 GHz front-end, 79 GHz PMCW radar and 145 GHz FMCW radar are discussed and future trends are identified.

Keywords: Millimeter wave, 5G, phased array, PA, PLL, radar, MIMO, FMCW, PMCW, imaging.

I. INTRODUCTION

Recent advances in integrated circuit technology have enabled a lot of applications in the mm-wave frequency range (30-300 GHz) at a low cost and with a small form factor in emerging areas such as high-speed wireless communication, radar, imaging and sensing. Next generation 5G wireless communication promises to increase data rate by utilizing huge bandwidth available at mm-wave frequency bands. It is expected that first the mm-wave communication products will operate at 28GHz, and then at 39GHz. When these bands get congested, similar to what is happening today in the low-GHz range, the unlicensed band around 60GHz can be widely used in commercial wireless products. In the automotive market, mm-wave radars play a critical role in advanced driver assistance system and autonomous vehicles by offering high resolution distance and speed measurement capability. Products in the 77 GHz range already exist for some years. Further, indoor radars can be used for presence detection in a room, vital signs monitoring, and gesture recognition. Other mm-wave applications include spectroscopy for chemical detection and high-resolution imaging for security, medical, and non-destructive testing applications utilizing mm-wave signal's ability to penetrate through different materials.

This paper presents an overview of recent developments in mm-wave integrated transceivers for several emerging applications. Architectures and circuits for mm-wave transceivers are discussed in Section II and III respectively. Comparison of process technologies for mm-wave circuit design is presented in Section IV. Section V discusses mm-wave transceiver design for wireless communication and

focuses on beamforming strategies, power amplifiers (PA), frequency synthesizers, front-end circuits for 60GHz and 28GHz, and future trends. Different mm-wave radar technologies are presented in Section VI followed by discussions on critical circuit blocks and example implementations of a 79 GHz phase modulated continuous wave radar and a 145 GHz frequency modulated continuous wave radar. Millimeter-wave sensing is discussed in Section VII and finally the paper is concluded in Section VIII.

II. ARCHITECTURES OF MM-WAVE SYSTEMS

As we move to higher frequencies, wavelength of the signal goes down resulting in smaller antenna size. Hence, more antennas can be placed in the same area. This opens up the possibility of shaping antenna beams into desired directions by using phased arrays. Beamforming with phased array architecture is expected to be widely used in mm-wave communication transceivers. Use of N antennas improves the signal-to-noise ratio (SNR) by $10 \log_{10}(N)$ in the receive path and on the transmit side it increases the signal strength by $20 \log_{10}(N)$ in the desired direction. Hence the overall link budget improves by $30 \log_{10}(N)$. Radars can also benefit from the smaller wavelength by using multiple-input multiple-output (MIMO) architecture where each transmitter transmits a coded radar signal and each receiver receives echo of each transmitted signal.

Both in communication systems with beamforming and in MIMO radars, the number of antennas depends on the application. For example, the number of antennas that can be placed in a mobile phone is much smaller than in a base station. In this way, the number of antennas can also impact the choice of IC technology. If the number of antennas is small, then the mm-wave circuitry and the digital processing circuitry can be placed together on a single chip. This is not possible for a massive number of antennas and in that case the choice of mm-wave IC technology can be different from the technology used for digital baseband circuitry.

III. MILLIMETER-WAVE CIRCUITS: WHAT'S DIFFERENT?

Design at mm-wave frequencies has different challenges compared to the low-GHz range. For passive components, the

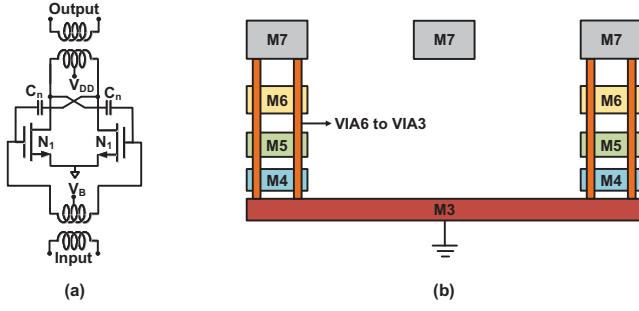


Fig. 1: (a) Differential pair with capacitive neutralization, (b) On-chip transmission line.

higher frequencies lead to smaller component values and hence a smaller footprint. On the other hand, the layout parasitics of both active and passive components and of the interconnect become relatively more important. In a metal line, parasitic capacitance of few fF to ground or series inductance of few pH plays a bigger role compared to low-GHz frequencies. As an example, at mm-wave frequencies AC coupling of differential stages is not done with capacitors, as they have significant parasitic capacitance to ground. In this case, it is preferred to use transformers, which is not possible in the low-GHz range due to their prohibitively large footprint. Moreover, self inductances of the primary and secondary windings of the transformers are typically used to resonate out the parasitic capacitances which are more critical at mm-wave frequencies compared to lower frequencies. In a differential common-source amplifier, which is a key component of many circuits, influence of the Miller effect is more prominent at mm-wave frequencies. In differential mode, the Miller effect can be mitigated by neutralization capacitors that are cross-coupled between the gate of the transistors and the drain of the other transistors resulting in a better input-output isolation as shown in Figure 1.(a). Different issues are observed at mm-wave frequencies in other widely used circuits too such as the cascode stage. While at low frequencies the noise contribution of the common-gate transistor is negligible, the degeneration seen by the noise source of this transistor is less effective at mm-wave. Moreover, a large amount of signal leaks away through the gate-source capacitance of that transistor. To alleviate this, the capacitance between the source of the common-gate transistor and the AC ground is resonated out with an inductance.

The mm-wave frequency bands that will be used initially will still be low enough such that in most cases design of passive components in a lumped fashion will lead to a more compact solution than a distributed design. As an illustration, Figure 1.(b) shows a cross section of an on-chip coplanar transmission line with a central conductor and grounded sidewalls. The wavelength ($\lambda = c/(f\sqrt{\epsilon_{eff}})$) depends on the effective dielectric permittivity (ϵ_{eff}) which in turn depends on the material and geometry of transmission line. For this coplanar transmission line, ϵ_{eff} is 5.2 which results in a

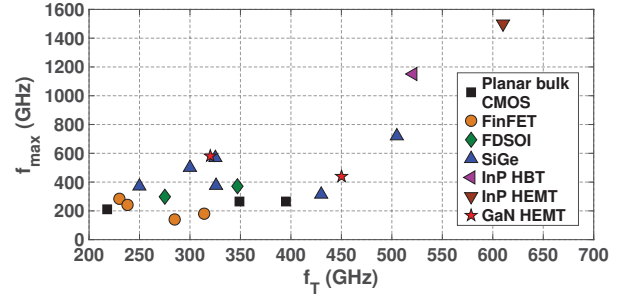


Fig. 2: f_T and f_{max} of different process technologies.

wavelength of 2.2mm at 60 GHz.

IV. COMPARISON OF IC TECHNOLOGIES

As in any domain where microelectronics is involved, the choice of an IC technology is a matter of performance, power, area, and cost. In the last two decades we witnessed conquest of planar bulk CMOS in many areas and it was not different in mm-wave applications too. Thanks to its downscaling, which came with a speed increase, CMOS has become more suitable for mm-wave applications, in spite of a decrease in the intrinsic driving capabilities due to reduced supply voltages. Other technologies were pushed to niche domains or to frequency bands which were still too high to be addressed by CMOS. Today, however, the CMOS scaling road map is slowing down and it is becoming important to explore other technologies that can provide better trade-off in performance, power, area, and cost.

Transistor parameters such as unity current gain frequency (f_T) and maximum oscillation frequency (f_{max}) are important for evaluating circuit performance at mm-wave frequencies. Figure 2 shows f_T and f_{max} of planar bulk CMOS, FinFET, FDSOI, SiGe, and III-V technologies from published literature [1]-[11]. Another important parameter of transistors is the breakdown voltage which generally decreases as f_{max} increases [12].

With the introduction of FinFETs it was seen that the intrinsic speed of the transistors even went down compared to planar CMOS devices [2]-[3]. This speed penalty is mainly due to increased parasitic capacitance caused by the three dimensional nature of the FinFET architecture. Fully-depleted SOI (FDSOI) is an alternative CMOS technology that still has a planar device architecture, which eliminates the problem of increased capacitance of FinFET. The buried oxide underneath the FDSOI device reduces the parasitic capacitance between the source / drain nodes and the ground [4]. In contrast to planar bulk, FinFET and FDSOI field-effect devices, bipolar transistors are vertical devices and feature higher speed which is generally determined by the thinness of the base [5]-[8]. When combined with CMOS in a BiCMOS process, complex circuitry can be designed. However, the CMOS part lags a few generations behind the state-of-the-art CMOS/FDSOI/FinFET processes, making this process less interesting for chips that have a complex digital part next to the analog/RF/mm-wave

functionality. On the other hand, III-V technologies such as GaN, GaAs and InP Heterojunction Bipolar Transistors (HBT) and High Electron Mobility Transistors (HEMT) can outperform CMOS and SiGe in terms of speed and power handling capabilities [9]. Out of the III-V candidates, InP is very promising as it can achieve extremely high f_T and f_{max} values ($f_{max} > 1\text{THz}$ as shown in Figure 2) due to high electron mobility and saturation velocity [10]-[11]. GaN HEMTs have lower f_T and f_{max} compared to InP [9], but they have high breakdown voltage and can provide better power and efficiency. But these III-V technologies suffer from low level of integration. As a result, front-end circuits with high output power requirements are designed on a separate III-V chip while rest of the complex electronics are made on CMOS. Co-integration of III-V devices with advanced CMOS technology [13] on the same substrate or through 3D stacking can be considered for enabling heterogeneous systems to generate more power than Si based technologies and to operate at lower THz frequencies.

V. MM-WAVE TRANSCEIVERS FOR WIRELESS COMMUNICATION

The main architectural novelty of a mm-wave wireless communication transceiver compared to its low-GHz counterpart is the addition of beamforming functionality. In the beginning of this century, after the unlicensed spectrum around 60 GHz has been made available for wireless applications, it was believed that mm-wave communication would only use low-complexity modulation thanks to the abundance of bandwidth compared to the channels in the low-GHz wireless standards. However, data rates in low-GHz communication have increased over the years thanks to MIMO. Therefore, spectral efficiency of mm-wave communication standards needs to go up in order to maintain sufficient value compared to low-GHz standards. Today, each mm-wave communication standard foresees at least a 64-QAM mode. The 5G NR standard even has a 256-QAM mode.

Complex modulation schemes lead to tighter error vector magnitude (EVM) specifications - for example, in the 64-QAM and 256-QAM modes of 5G NR the EVM should be better than 8% and 3.5%, respectively. In addition, the peak-to-average power ratio (PAPR) becomes higher in signals with more complex modulations. The EVM requirements and larger PAPR pose challenges on several circuits in a transceiver. The most affected ones are the analog-to-digital converter (ADC), the power amplifier (PA), and the phase-locked loop (PLL). ADCs suffer from increased bandwidth and tight resolution requirements. Baseband circuits such as ADCs are not discussed in detail in this paper. In mm-wave communication systems, spectral purity of the PLL limits the RX EVM. In the transmitter, the biggest challenge other than the PLL spectral purity is the design of the PA, where power consumption and linearity are critical.

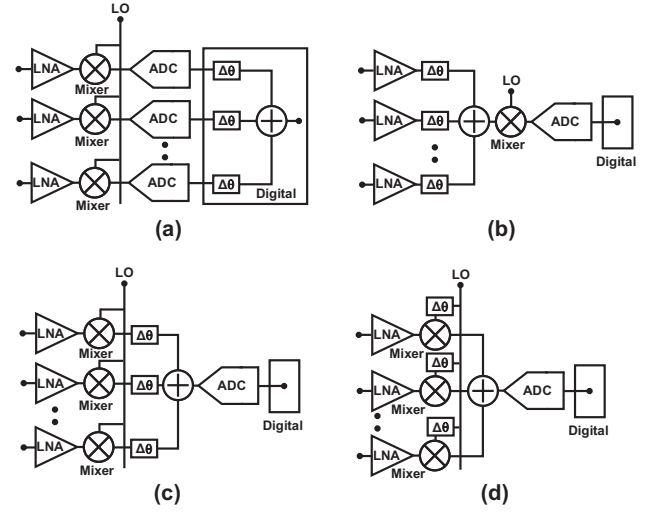


Fig. 3: Beamforming strategies (only RX side is shown): (a) digital beamforming, (b) RF beamforming, (c) analog baseband beamforming, and (d) LO phase shifting based beamforming.

A. Beamforming strategies

To determine what hardware is needed for beamforming, let us consider an electromagnetic wave that reaches a linear antenna array at the receive side with a certain angle resulting in signals in individual antenna paths being delayed with respect to each other. To let the signals combine in a constructive way, these delays have to be compensated which requires a programmable delay in each antenna path. Signals from all the paths can be added after the delays. At the transmit side, the reverse operation is needed - first, signals are split in different antenna paths and then a variable delay is implemented in each path.

Various attempts have been published to create true time delays. For example, [14] uses a trombone structure where the variable delay is achieved by switching the signal path. This is quite lossy and the loss depends on the required delay. The vast majority of beamformers replace true time delays with phase shifters. For narrowband signals and small antenna arrays, approximating a delay by a phase shift does not produce significant errors. In summary, beamforming operation requires phase shifters, signal combiners and signal splitters. The beamforming functionality needs to be combined with normal signal operations in a radio transceiver. Various beamforming approaches are shown in Figure 3.

Implementing beamforming operations digitally (Figure 3.(a)), offers the highest accuracy and flexibility, but the replication of full hardware in each signal path leads to high power consumption and large chip area.

The closer the beamforming operations are performed to the antenna, the less hardware is duplicated. The extreme case is RF beamforming (Figure 3.(b)), where phase shifting and signal combining / splitting are performed at mm-wave

frequencies. This is the preferred approach for large on-chip arrays [38]-[39], [46]. Wide variety of phase shifters can be used for implementing RF phase shifting. These phase shifters can be classified into four categories [15] - reflective-type, loaded-line, switched-delay phase shifters and vector modulators. Practical implementations of the first three types have insertion loss that varies with the required phase shift. This requires compensation by a high-resolution variable-gain amplifier and, consequently, a complex calibration procedure. Vector modulators, on the other hand, are more suitable for minimizing the dependence of insertion loss on phase shift [38]. In this case, the signal is first split into an in-phase and a quadrature component. Adding these two components with programmable weights, which depend on the required phase shift, produces the phase shifted signal. Required signal splitting and combining at mm-wave frequencies are most often done with Wilkinson splitters / combiners which are lossy. For example, in [38] a 1:8 splitter (8:1 combiner) in 28nm CMOS is reported where three stages of 1:2 splitters (2:1 combiners) are used that result in an extra loss of about 1.5dB per stage at 60GHz. This loss needs to be compensated in order to achieve a sufficiently high transmit power.

Performing beamforming operations at higher frequencies results in more loss and higher sensitivity to layout parasitics. In analog baseband beamforming (Figure 3.(c)), phase shifting and signal combining / splitting are performed in analog domain at baseband frequencies. In a direct conversion architecture, the signal at baseband is already available in IQ form. In this case, a vector modulator can be used elegantly. Signal combining in the RX can be done in the current domain instead of using a Wilkinson combiner. The parasitic capacitance, which comes from the routing necessary to bring the signals of different antenna paths together for combining, can be absorbed in the capacitors of analog baseband filters. In addition, since no lossy beamforming operations are needed at RF, the RX can have a very good noise figure (NF). The disadvantage of this approach is that downconversion and upconversion mixers are needed for each antenna path, necessitating LO distribution to each path. This is not a problem for smaller arrays. The cost of this LO distribution in terms of area and power consumption is illustrated in Figure 4 for the 4-way analog baseband beamforming 60 GHz TRX of [42]. The mm-wave circuitry still consumes most of the power and LO distribution consumes only 14% of the TX power. Clearly, the TX consumption is dominated by the 4 PAs which shows the importance of high efficiency in mm-wave PAs (discussed in Section V.B).

A fourth beamforming architecture is LO phase shifting based beamforming (Figure 3.(d)) [16]-[17]. In this case the LO signal is distributed to each antenna path. The mm-wave LO signal in each path is then phase shifted before being used for downconversion / upconversion through the corresponding mixer. Downconversion / upconversion with a phase shifted LO results in a phase shift in the signal. The advantage of this approach is that amplitude variations over different phase shifts are less problematic as the conversion gain is not very

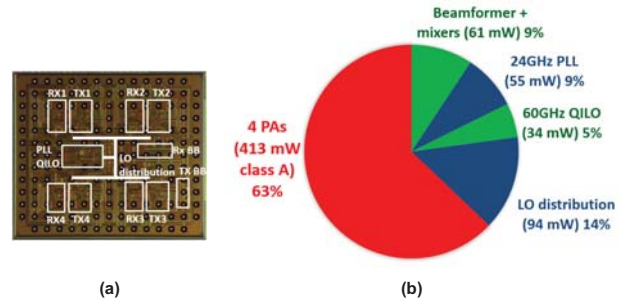


Fig. 4: 60 GHz 4-way analog baseband beamforming TRX in 28nm: (a) chip photograph, (b) power consumption in the TX.

sensitive to amplitude variations in the large LO signal.

B. mm-wave power amplifiers

One of the most critical circuits in mm-wave transceivers for wireless communication is the power amplifier. Obtaining high output power from the PA with good linearity and high efficiency in presence of modulated signals with high peak-to-average power ratio (PAPR) remains a challenge. PAs for mm-wave frequencies have been reported in both CMOS and SiGe [18]-[31]. Linear class-A PAs suffer from low efficiency and higher classes are preferred to obtain better efficiency. Starting from class-A mm-wave PAs in the early days of 60 GHz research [19], class-AB designs such as [20]-[21] and even higher classes such as class-D [22], class-E [23], and continuous mode class-F/ F^{-1} [24] PAs have been reported in literature. Different architectures have been explored to enhance back-off efficiency of mm-wave PAs such as Polar [25], Doherty [26], and Outphasing [27] architecture. Different techniques to increase output power of mm-wave PAs have also been reported such as transistor stacking [28], on-chip power combining [29], and spatial power combining [30]. Recently an approach of PA and antenna co-design has been reported for 62-68 GHz in [31] where the Doherty combiner is merged with on-chip antenna in 45nm CMOS SOI leading to P_{sat} of 19.4 dBm and 6-dB back-off PAE of 20.1%. Compared to Si based PAs, higher output power and efficiency can be obtained using InP such as 26.7dBm P_{out} and 23.4% peak PAE at 81 GHz as reported in [32].

C. mm-wave frequency synthesizers

Another challenging circuit for mm-wave transceivers is the frequency synthesizer. Lower EVM is required in the transmitter for supporting higher order modulations and low phase noise in the LO is needed to achieve good EVM. At mm-wave frequencies, phase locked loops (PLLs) suffer from poor integrated phase noise. Further, tuning range is limited by the relatively large contribution of parasitic capacitance in the LC tank of a VCO. Thirdly, in direct conversion transceivers where the VCO frequency is the same as the carrier frequency, pulling of the LO by the PA is possible. Finally, the first dividers in the division chain of a classical PLL need to

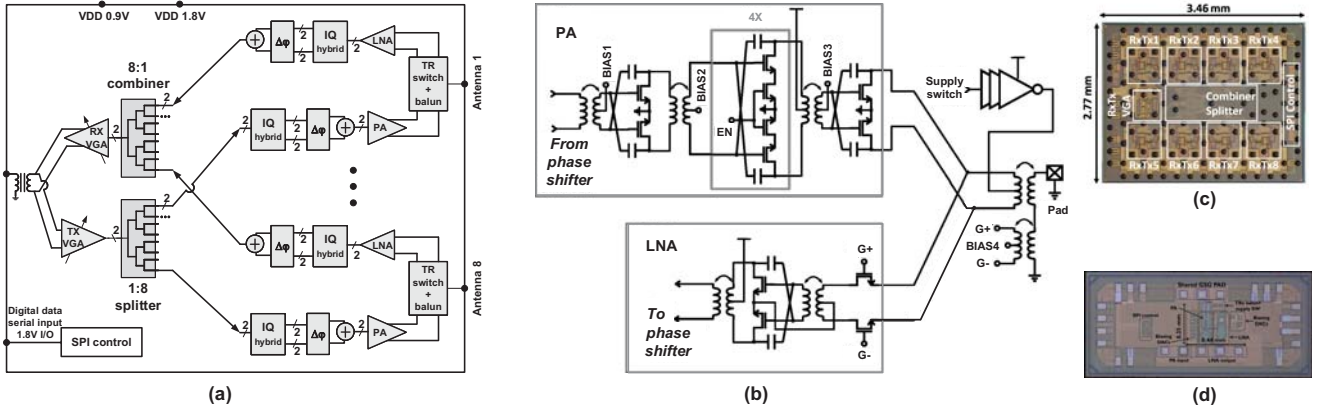


Fig. 5: (a) Block diagram of TRX front-end of 60 GHz phased array, (b) 60 GHz PA, LNA with T/R switch, (c) chip micrograph of 60 GHz phased array in 28nm CMOS, (d) chip micrograph of 28 GHz transceiver front-end in 22nm FD-SOI.

operate at mm-wave frequencies. Static mm-wave dividers consume large amount of power. Injection-locked dividers can be used as an alternative but their limited locking range poses a challenge.

To overcome these problems, a lower-frequency PLL is often implemented followed by a frequency multiplier. A well designed multiplier results in negligible increase in phase noise such that the difference in phase noise between the signal at the output and the input of the multiplier is $20 \log_{10}(M)$, with M being the harmonic number. A frequency multiplication can be obtained by extracting the right harmonic from a nonlinear amplifier (a non-oscillating circuit) [33]. Another approach is injection locking an oscillator that operates in the vicinity of the wanted harmonic [34]-[35], [42]. The result is an injection-locked oscillator (ILO) or quadrature ILO (QILO) which is used for direct conversion. The locking range increases with the amplitude of the injected subharmonic. The operating frequency of the PLL can be tuned to the frequency zone where the quality factor of the LC tank is optimal. In [42], the operating frequency has been chosen around 24 GHz.

Modern trends in low-GHz PLLs are also being adopted in mm-wave PLLs. For example, sub-sampling PLLs at mm-wave frequencies have been demonstrated [36], eliminating the phase noise contribution of the charge pump and the power hungry divider chain. Digital PLLs are also being adopted for mm-wave operation [37]. Additionally, the effect of close-in phase noise can be reduced in the digital domain at the RX side by removing the common phase error of a set of constellation points.

D. 60 GHz CMOS and 28 GHz FD-SOI implementations

As an example of RF beamforming, a 60GHz 8-way beamforming TRX front-end in 28nm CMOS [38] is discussed here. Block diagram of the phased array chip is shown in Figure 5.(a). The PCB antennas are shared between RX and TX requiring the use of an antenna switch. At mm-wave frequencies, use of a MOS transistor as a series switch results

in significant loss which is not acceptable for the RX NF. It also degrades the efficiency and output compression point in the TX. As an example, [46] shows that while a traditional switch causes almost equal insertion loss in both TX and RX mode, the proposed switch topology of [46] at 28GHz has negligible insertion loss in TX mode at the cost of degraded RX NF.

The implementation of PA, LNA, and T/R switch in the beamforming 60GHz FE are shown in Figure 5.(b). In this case, the antenna switch avoids use of any lossy physical switch in the differential signal path. The output of the last PA stage (common-source), is connected to the input of the first LNA stage (common-gate) and gate bias is used to switch each block “on” or “off”. The supply voltage is also switched in addition to the gate voltages to allow the use of an nMOS common-gate LNA instead of a pMOS one. This improves the performance and provides extra isolation by reducing the loading effect of the PA and the LNA on each other when “off”. The large inverter used to switch the supply has a negligible impact on the PA efficiency.

The PA uses three pseudo-differential transformer-coupled stages with cross-coupled capacitive neutralization. MOS capacitors are used for neutralization for better tracking of process variation in the main transistors. The output stage is biased in class-AB. The second stage of the PA consists of four parallel stages that can be enabled or disabled resulting in variable gain. The common-gate input stage of the LNA uses transformer-coupled gm-boosting that is combined with the input balun. The second LNA stage is a differential common-source stage with capacitive neutralization. The DC current of the two LNA stages is reused reducing power consumption by half at the cost of decreased transconductance of the common-gate transistors. Beamforming is implemented with a vector modulator-based phase shifter and a differential 3-stage Wilkinson combiner and splitter.

The chip micrograph of the 60GHz phased array is shown in Figure 5.(c). Measured performance of this chip is shown

TABLE I: Performance comparison of 60GHz phased arrays

References		[38]	[39]	[40]	[41]	[42]
No. of antenna paths		8	16	32	1 TX, 2 RX	4
Beamforming type		RF Active	RF Passive	RF	RF Active	Analog baseband
CMOS tech. (nm)		28	40	65	65	28
Integration		FE	FE, PLL, IF	FE, PLL, IF, BB	FE	FE, PLL, BB
Integ. T/R switch		Yes	Yes	No	No	No
TX P1dB _{out} / path (dBm)		10	5.2 (PA, w/o switch)	9 (PA)	4	>7.5
EIRP (dBm)		26 @ 5dB BO	24 @ -23dB EVM	28 @ -19dB EVM	NA	24 @ -21dB EVM
RX min. NF (dB)		6.8	5 (LNA, w/o switch)	<10	<7.2 (5.5 LNA)	4.8
Gain / path (dB)	TX	24.2	33 (PA)	22 (PA)	7.7	32
	RX	16.7	31 (LNA)	20 (LNA)	12	62
Pdc (mW)	TX	508	1190	1820	168	<546
	RX	231	960	1250	156	431
PS	Amplitude error (dB)	±0.35	NA	NA	±2	<1
	Phase resolution (°)	3.1 ¹ , 4.9 ²	5.6 ¹	NA	22.5 ¹	<5 ¹
Scan angle (°)		±46 ³	±60 ⁴	NA	NA	±45/±30
Area (mm ²)		9.6	26.3	72.7, 77.2	1.6, 1.7	7.9

¹ Average. ² Maximum. ³ In both E and H planes. ⁴ Only for vertical polarization in H-plane.

in Table I and compared with other published 60 GHz phased array chips. The vector modulator based phase shifter (PS in Table I) makes the amplitude variation as a function of the required phase shift sufficiently small such that calibration is not needed.

Comparing RF beamforming [38] with analog baseband beamforming [42] (both have been designed in the same 28nm CMOS technology), it is seen that NF in analog baseband beamforming is superior. This is partly due to the superior noise performance of the common-source stage compared to the common-gate stage used for the antenna switch functionality, and also due to the impact of the RF phase shifter on NF. The TX signal paths of both approaches use similar PAs, but the 1dB compression point is higher in the RF beamforming front-end. This implies that the switch solution does not degrade linearity. The lower compression point of the analog baseband beamforming solution is caused by the mixer nonlinearity.

The PA, LNA and switch solution discussed before has also been implemented in 22nm FD-SOI for operation at 28 GHz [43]. The chip micrograph of 28 GHz front-end is shown in Figure 5.(d). Table II summarizes performance of this front-end chip and compares with other state-of-the-art 28 GHz transceivers in different process technologies. It is seen that the NF is quite low while the maximum PAE of the PA is relatively high.

E. Future trends in mm-wave wireless communication

Adoption of mm-wave frequencies for wireless communication technologies is already taking place today such as 5G cellular communication, 60GHz WiFi (IEEE 802.11ad) and E-band (71-76GHz and 81-86GHz) point-to-point communication. This trend is going to continue in future to satisfy the demand for growing data rate. It is expected that for very high data rate applications such as augmented reality (AR) and virtual reality (VR), wireless communication technologies will start utilizing even higher frequency bands in the mm-wave spectrum. The D-band (110-170 GHz) can be used for high data rate wireless communication such as

TABLE II: Performance comparison of 28GHz transceivers

References	[43]	[44]	[45]	[46]
Integration level	PA, LNA, SW	Full TRX (24 antennas)	Full TRX (8 antennas)	Full TRX (32 antennas)
Frequency (GHz)	28	28	28	28
Technology	22nm FDSOI	28nm CMOS	28nm CMOS	0.13μm SiGe
Integ. T/R SW?	Yes	Yes	Yes	Yes
PA w/ switch				
Supply (V)	0.8	1	1.05	2.7
Gain (dB)	16.7	TX 34-44	PA 30	TX 34
OP _{1dB} (dBm)	11.2	>12	9.5	13.5
PSAT (dBm)	13.5	>14	10.5	16
PAE @6dB back-off from OP _{1dB} (%)	13.1	~7.5	N.A.	N.A.
PAE @OP _{1dB} (%)	31.1	~17.5	N.A.	N.A.
PAE _{max} (%)	33.8	20	N.A.	20
LNA w/ switch				
Supply (V)	0.8	1	1.05	1.5
Gain (dB)	17	7-16 (w/ PS)	12-24	N.A.
NF (dB)	4	3.8-4.4 (w/ PS)	5.6	6
IP _{1dB} (dBm)	-22	N.A.	N.A.	-22.5 (w/ VGA)

wireless backhaul and chip-to-chip communication [47]. An implementation of D-band circuit is shown here - a two-stage transformer coupled cascode amplifier has been designed in 0.13μm SiGe BiCMOS process for 140GHz wireless communication and a gain of 9.9dB has been obtained from measurements.

At the higher end of the mm-wave frequency range (around 300GHz), huge available bandwidth enables wireless communication with extremely high data rate of 100 Gb/s and beyond. In this range, the IEEE 802.15.3d is defined for applications such as wireless backhaul / fronthaul, wireless data center, intra-device communication, and proximity point-to-point communication including kiosk downloading and file

exchange. Integrated transceivers have been demonstrated in this frequency range [48]-[49]. At these frequencies it is difficult for silicon technologies to generate enough TX power and efficiency is very low. For example, the 40nm TX of [49] can generate -5.5dBm output with 1.4W power consumption. III-V devices can be useful to obtain higher power and efficiency numbers. For example, in [50], a PA designed with InP HBT is demonstrated operating between 180 and 265 GHz with a peak output power of 140mW and a PAE of 5.1% at 200GHz.

VI. MM-WAVE TRANSCEIVERS FOR RADARS

Using mm-wave frequencies for radar has several benefits. First, the range resolution is inversely proportional to modulation bandwidth (BW). Range resolution can be expressed as

$$R_{res} = c/(2BW) \quad (1)$$

where c is the speed of light. At high carrier frequencies such as mm-wave, a large absolute bandwidth is easily achievable, making mm-wave spectrum very attractive for high-resolution radar. Also, velocity of targets can be determined more accurately at mm-wave compared to lower frequencies as it is calculated from Doppler shift which is proportional to the frequency of operation.

Choice of the radar waveform affects its performance as well as circuit complexity. A pulse based radar [51] transmits narrow pulses of mm-wave signal. This requires high peak power which is more difficult to achieve. On the other hand, a continuous wave radar with constant envelope phase or frequency modulation leads to higher transmitter efficiency, easier implementation of the receiver and increased processing gain with intensive digital operations. Both frequency modulated continuous wave (FMCW) and phase modulated continuous wave (PMCW) type of radars have been implemented in SiGe and CMOS [52]-[61].

In a PMCW radar, a binary sequence with good periodic auto-correlation property is generated and the local oscillator (LO) signal is phase modulated with that sequence. The phase modulated signal is transmitted and the reflected signal is downconverted by the same LO signal. The received sequence is a delayed replica of the transmitted sequence where the delay corresponds to the distance of the object. The received sequence is digitized and correlated with delayed copies of the transmitted signal. A non-zero correlation represents distance of the object.

FMCW is the most popular choice of waveform for radars. In this case, a frequency domain sawtooth waveform (chirp) is generated where the frequency of the CW signal increases linearly with time and then goes back to initial frequency quickly. The received signal, which is a delayed version of the transmitted signal, is mixed with the actual transmitted signal in the receiver and it creates a low-frequency beat signal whose frequency is a measure of the distance (range) between the radar and the object. Use of multiple antennas helps in obtaining angular or spatial information. If a MIMO radar uses

N_{TX} transmit antennas and N_{RX} receive antennas where each RX can distinguish signal from each TX, a virtual $N_{TX} \times N_{RX}$ array is created. The SNR is also increased by this factor.

The trade-offs between FMCW and PMCW radars can be summarized as: (1) in MIMO PMCW radars it is easier to achieve orthogonality of TX waveforms by using binary phase codes in case of simultaneous transmission; (2) in a high phase noise situation, PMCW radar suffers slightly from range sidelobe degradation while FMCW radar suffers slightly from worse range behavior at long range; (3) it is easier to make PMCW systems robust to interference from other radars by using different codes or by code hopping; (4) FMCW radar requires relatively lower IF bandwidth, which is much smaller than the chirp bandwidth, while the analog baseband section of a PMCW receiver requires at least half of the entire modulation bandwidth; (5) it is easier to remove TX-to-RX spillover in FMCW; (6) generation of PMCW waveform is much simpler compared to FMCW waveform with linear slope.

A. Critical circuit blocks of mm-wave radar

One of the most critical components in FMCW radar is the linear chirp generator which is generally designed based on a PLL. The chirp signal has to be linear to avoid spurious tones in the receiver baseband which result in false detections. Also large chirp bandwidth is needed to achieve good range resolution. Conventionally, the modulating signal to generate the chirp is injected in the divider chain of the PLL. This approach can be extended to a two-point-modulation (TPM) scheme where the modulating signal is injected to another tuning port of the voltage controlled oscillator (VCO) [62], [64]. Large chirp bandwidth is often achieved by frequency multiplication of the output of the chirp generator which increases the chirp bandwidth by the frequency multiplication factor. For example, in [59] a $4 \times$ frequency multiplier is used. Performance of state-of-the-art PLLs for FMCW radar are summarized in Table III.

In a CW radar, the PA can be driven into saturation. The challenge in the PA design is to generate a high saturated output power (P_{sat}) with good efficiency (PAE). For a given technology, P_{sat} and PAE generally decrease when operating frequency goes up. Published 77 / 79 GHz silicon-based radar chips have shown output power in the range of 13-14.5dBm as shown in Table IV.

Design and measurement results of a PA for 140 GHz FMCW radar are shown in Figure 6. The PA consists of four common source push-pull stages with transformer based matching network as shown in Figure 6.(a). The common source stages are capacitively neutralized to ensure unconditional stability while obtaining maximum gain. The PA stages are biased in class-AB to obtain higher efficiency. 40 μ m and 80 μ m transistor width are chosen for the third and the fourth stage of the PA respectively and round table layout technique [65] is used for both of them. The output balun is designed using load-pull simulations and implemented using overlay structure in top two metal layers. The 140 GHz PA is implemented in 28nm CMOS and the chip micrograph is

TABLE III: Performance comparison of state-of-the-art PLLs for FMCW radar

References	[59]	[62]	[63]	[64]
Architecture	TPM/ FracN-PLL	TPM/ BB-PLL	Frac-N PLL	TPM/ SS-PLL
Waveform	Sawtooth	Sawtooth	Sawtooth	Sawtooth
Technology	45nm CMOS	65nm CMOS	130nm SiGe	28nm CMOS
Fast chirp ($<50\mu s$)	Y	Y	Y	Y
Ref. freq. (MHz)	1000 ¹	52	125	80
Center freq. (GHz)	19- 20.25	20.4- 24.6	18.8- 20.8	14.7- 17.2
BW _{chirp} /T _{ramp} (GHz/ μs) : rms FM error (kHz)	1/40 : 600 ²	0.2/1.2 : 124	1.25/50 : 800 ³	1.5/30 : 103 1.5/100 : 46
BW _{chirp} / Center freq. (%)	5	0.9	6.25	9.375
rms FM error / BW _{chirp} (%)	0.06 ²	0.05/0.21	0.064	0.003- 0.007
Phase noise ⁴ (dBc/Hz)	-91~-94	-92	-97	-92.6
Power (mW)	>120	20	240	44

¹ A clean-up PLL is required to generate 1 GHz reference clock.

² Only maximal error reported.

³ 5% of chirp time excluded.

⁴ Normalized to 79 GHz carrier at 1 MHz offset.

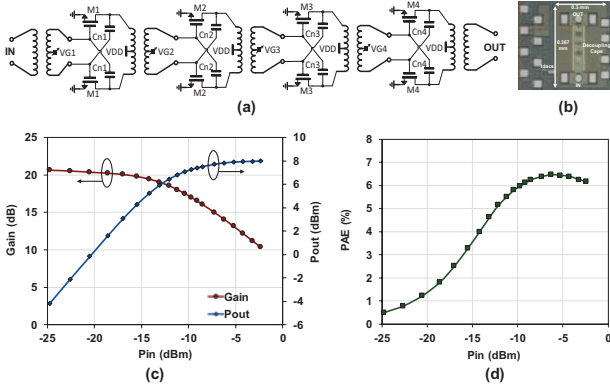


Fig. 6: 140 GHz PA for FMCW radar: (a) schematic, (b) chip micrograph, (c) gain and output power, (d) PAE.

shown in Figure 6.(b). The PA achieves a gain of 20.7dB and P_{sat} of 8dBm. Figure 6.(c) shows measured gain and output power of the PA as a function of input power. The PA has a peak drain efficiency (DE) of 7% and peak power-added efficiency (PAE) of 6.5%. Measured PAE of the PA is shown in Figure 6.(d). OP1dB of 5.2dBm and 3dB bandwidth of more than 20GHz are obtained from the PA.

B. mm-wave radar SoCs

The main driving force behind the development of integrated mm-wave radar has been the automotive industry. While the frequency band around 24GHz has been used in the past, today the frequency of choice is 76-81GHz band for automotive radars. SiGe has often been preferred for automotive radars

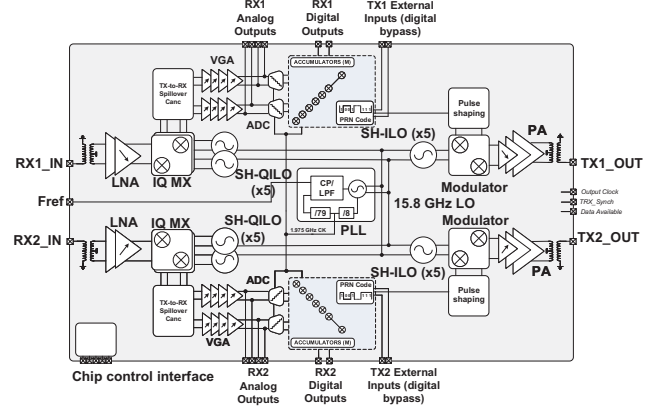


Fig. 7: Block diagram of the 79 GHz PMCW radar chip.

[52]-[55] due to its higher output power at mm-wave and its good performance over wide temperature range. However, CMOS radars are becoming popular too [56]-[61]. Both PMCW and FMCW waveforms have been used for automotive radars as shown in Table IV. The PMCW system is more suitable for a digitally intensive architecture in advanced CMOS. For example, the 79GHz PMCW radar of [61] has been designed in 28nm CMOS and it obtains a range resolution of 7.5cm. Bandwidth requirement of the analog baseband part of a PMCW radar becomes challenging if higher range resolution is needed. On the other hand, the FMCW radar of [59] achieves a chirp bandwidth of 4GHz while keeping the required baseband bandwidth as low as 15MHz.

Radars built in advanced CMOS technology can combine the analog front-end circuitry with the digital signal processing. As an example, block diagram of the 79GHz 2×2 MIMO PMCW radar SoC designed in 28nm CMOS is shown in Figure 7 [61]. This SoC uses BPSK modulation with a data rate of 2Gbps. For generating the mm-wave carrier, first 15.8 GHz signal is generated by integer-N PLL based on a class-B LC-VCO with tail inductor filtering. Then 79 GHz signal is produced by $\times 5$ frequency multiplication using subharmonic injection locked oscillators (SH-ILOs). In the TX path, sidelobes are suppressed using harmonic reject mixer technique. The PA consists of three transformer coupled common source push-pull stages with capacitive neutralization. The RX front-end has a transformer coupled two-stage LNA based on push-pull NMOS structure followed by a Gilbert cell mixer. Measured performance of the chip is shown in Table IV with other state-of-the-art 77/79 GHz radars from literature.

Automotive radars of Table IV can provide a range resolution of 3.75cm corresponding to a chirp bandwidth of 4GHz. More bandwidth is available in the 60GHz band which corresponds to finer range resolution. For example, the FMCW radar of [66] has two transmitters and four receivers in $0.35\mu m$ SiGe technology and uses 7GHz bandwidth around 60GHz for a range resolution of 2.1cm. This radar is intended for short-range, indoor applications such as gesture recognition. For

TABLE IV: Performance comparison of 77 / 79 GHz radars

References	[52]	[56]	[53]	[57]	[58]	[59]	[61]
Technology	SiGe Bipolar	CMOS 65nm	SiGe (chipset)	CMOS 65nm	CMOS 65nm	CMOS 45nm	CMOS 28nm
Modulation type	PMCW	FMCW	FMCW	PMCW	PMCW	FMCW	PMCW
Frequency (GHz)	77	77	77	79	79	79	79
#TX/#RX	1/1	1/2	1/4	1/0	0/1	3/4	2/2
PMCW: chip rate (Gbps)	2.14	1.93	-	2	2.5	4	2
FMCW: chirp BW (GHz)							
RX NF (dB)	13	5	10	-	10.5	18	12*
TX Pout (dBm)	6.2	13	13	14.5	-	10.8	8.5*
PN @ 1MHz (dBc/Hz)	-105	-81	-97	-95	-	-91	-85
Frequency synthesis	Ext LO	PLL	VCO	VCO	Ext LO	PLL	PLL
ADC / Digital processing	Part**	No	No	Part**	No	Yes	Yes
Power cons. (W)	1.2	0.343	0.79+1.75	0.16	0.057	3.5	1
Die area (mm ²)	5.9	4.64	12+6.5	1.3	0.58	22	7.9

* Including flip-chip assembly and module loss.

** Transmitted sequence generation.

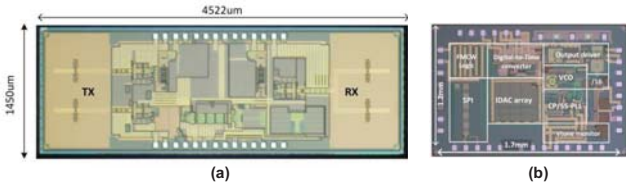


Fig. 8: Chip micrographs: (a) 145 GHz radar transceiver front-end, (b) accompanying 16 GHz chirp generator.

even finer range resolutions, the required bandwidth becomes a very high fraction of the center frequency, which makes the design of the mm-wave circuits very difficult. Instead, a higher carrier frequency can be used, although it is more challenging for silicon technologies. For example, the 0.13 μ m SiGe FMCW radar front-end of [67] operates around 240GHz and achieves RF bandwidth of 60GHz. The 145GHz FMCW transceiver front-end of [68], designed in 28nm planar bulk CMOS, achieves a bandwidth of 13 GHz. The chirp signal generated from [64] is frequency-multiplied by nine in the transceiver chip [68]. The 145GHz radar chip of [68] achieves TX EIRP of 11.5dBm, RX NF of 8dB, and uses on-chip antennas. Off-chip antennas in this case would lead to a large insertion loss and limited bandwidth. The chip micrographs of the 145GHz radar transceiver front-end [68] and the chirp generator [64] are shown in Figure 8.

VII. MM-WAVE TRANSCEIVERS FOR SENSING

Other than position and velocity detection of objects by radars as discussed in previous section, sensing applications of mm-wave include spectroscopy for chemical detection and imaging for non-destructive testing, security screening and medical diagnosis.

Rotational spectroscopy can be used for detection of different gas molecules as they show unique spectral fingerprint in mm-wave and THz frequency range. Potential applications of gas spectroscopy include breath analysis, environmental monitoring, toxic gas detection etc. In an integrated transceiver for spectroscopy, obtaining high transmit

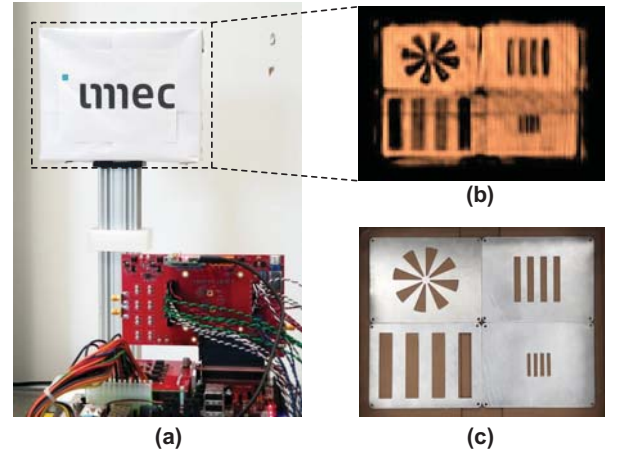


Fig. 9: (a) Millimeter-wave imaging setup with 79GHz transceiver on a scanning stage and box containing metallic objects, (b) mm-wave image obtained from the setup, (c) photograph of the metallic objects inside the box.

power, wide frequency range, high efficiency and fast scanning at the same time in mm-wave / THz frequencies is a significant challenge. Transceivers operating at 238-252 GHz and 494-500 GHz in 0.13 μ m SiGe have been demonstrated in [69]. In [70], wider bandwidth (210-305 GHz) has been reported for a receiver in 65nm CMOS. In [71], a dual comb architectures is proposed which uses 10 frequency tones and covers 220-320 GHz with a total radiated power of 5.2mW and 14.6-19.5 dB NF.

In a mm-wave imaging system, lateral resolution is defined as $\delta = \lambda D / L$ where λ is the wavelength, D is the distance of the object, and L is the length of aperture [72]. Range resolution is given by Equation (1). Operating at higher frequency is preferred as better lateral resolution can be obtained and also because higher bandwidth can be achieved leading to better range resolution. Integrated transceivers have been demonstrated for mm-wave imaging. In [72], a multistatic sparse array based imaging architecture is presented which

employs 768 transmit and 768 receive channels with SiGe front-end modules operating in 72-80 GHz. An imager with SiGe detector array and CMOS source array for 240-290 GHz has been demonstrated in [73]. Sensitivity can be improved by coherent detection architecture as shown in [74] for a 320 GHz imager in 0.13 μ m SiGe. Spectroscopic information can be obtained for each pixel of the image using hyperspectral imaging technique such as [75] which uses harmonics in the frequency range of 160GHz - 1THz, but this frequency band is not covered contiguously. A full-band hyperspectral imaging transceiver is shown in [76] in 45nm CMOS SOI which covers 90-300 GHz in transmitter and 115-325 GHz in receiver.

A Synthetic Aperture Radar (SAR) approach for mm-wave imaging is shown in Figure 9. The 79GHz radar SoC of [61] is used in a motorized linear mechanical scanning stage and metallic objects inside a box are imaged. Figure 9 shows that from the reconstructed mm-wave image, objects can be identified inside a box, which is made of material not transparent to visible light. Moving to higher frequencies beyond 100GHz and using frequency multiplication technique can widen the bandwidth used for imaging leading to a much better range resolution. Additionally, integrating more number of transceivers to build a large MIMO array or phased array with electronic beam steering combined with advanced imaging algorithms can provide much better performance and real time imaging capability at a low cost.

VIII. CONCLUSION

Multi-Gbps wireless communication and high resolution radars have been enabled by extensive research in mm-wave IC design. Both BiCMOS and CMOS solutions are being used today and co-integration of III-V devices with CMOS will be necessary in future for higher speed and power. Beyond the mass market adoption of mm-wave 5G at 28GHz and 39GHz, continued research in mm-wave circuit, antenna, and packaging will be needed for wireless communication at higher frequencies to satisfy growing data rate requirement. Integrated transceivers at 76-81GHz have been demonstrated for automotive radars. New applications such as gesture recognition, imaging, and spectroscopy will also lead to mm-wave IC research at even higher operating frequencies.

REFERENCES

- [1] M. Yang *et al.*, "RF and mixed-signal performances of a low cost 28nm low-power CMOS technology for wireless system-on-chip applications," *Symposium on VLSI Technology*, 2011, pp. 40-41.
- [2] J. Singh *et al.*, "14nm FinFET technology for analog and RF applications," *Symposium on VLSI Technology*, 2017, pp. T140-T141.
- [3] B. Sell *et al.*, "22FFL: A high performance and ultra low power FinFET technology for mobile and RF applications," *IEEE International Electron Devices Meeting*, 2017, pp. 29.4.1-29.4.4.
- [4] S. N. Ong *et al.*, "A 22nm FDSOI Technology Optimized for RF/mmWave Applications," *IEEE Radio Frequency Integrated Circuits Symposium*, 2018, pp. 72-75.
- [5] P. Chevalier *et al.*, "A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz f_T / 370 GHz f_{MAX} HBT and high-Q millimeter-wave passives," *IEEE International Electron Devices Meeting*, 2014, pp. 3.9.1-3.9.3.
- [6] J. Böck *et al.*, "SiGe HBT and BiCMOS process integration optimization within the DOTSEVEN project," *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 2015, pp. 121-124.
- [7] J. Korn *et al.*, "Experimental and theoretical study of f_T for SiGe HBTs with a scaled vertical doping profile," *IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 2015, pp. 117-120.
- [8] B. Heinemann *et al.*, "SiGe HBT with f_T/f_{max} of 505 GHz/720 GHz," *IEEE International Electron Devices Meeting*, 2016, pp. 3.1.1-3.1.4.
- [9] M. Micovic *et al.*, "High frequency GaN HEMTs for RF MMIC applications," *IEEE International Electron Devices Meeting*, 2016, pp. 3.3.1-3.3.4.
- [10] M. Urteaga *et al.*, "A 130 nm InP HBT integrated circuit technology for THz electronics," *IEEE International Electron Devices Meeting*, 2016, pp. 29.2.1-29.2.4.
- [11] X. Mei *et al.*, "First Demonstration of Amplification at 1 THz Using 25-nm InP High Electron Mobility Transistor Process," *IEEE Electron Device Letters*, vol. 36, no. 4, pp. 327-329, April 2015.
- [12] H. Hashemi, "Millimeter-wave power amplifiers & transmitters," *IEEE Custom Integrated Circuits Conference*, 2017, pp. 1-8.
- [13] N. Collaert *et al.*, "Semiconductor Technologies for next Generation Mobile Communications," *14th IEEE International Conference on Solid-State and Integrated Circuit Technology*, 2018.
- [14] J. Roderick *et al.*, "Silicon-Based Ultra-Wideband Beam-Forming," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1726-1739, Aug. 2006.
- [15] A. S. Y. Poon *et al.*, "Supporting and Enabling Circuits for Antenna Arrays in Wireless Communications," *Proceedings of the IEEE*, vol. 100, no. 7, pp. 2207-2218, July 2012.
- [16] A. Natarajan *et al.*, "A 77-GHz Phased-Array Transceiver With On-Chip Antennas in Silicon: Transmitter and Local LO-Path Phase Shifting," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2807-2819, Dec. 2006.
- [17] K. Scheir *et al.*, "A 52GHz Phased-Array Receiver Front-End in 90nm Digital CMOS," *IEEE International Solid-State Circuits Conference*, 2008, pp. 184-605.
- [18] U. R. Pfeiffer *et al.*, "SiGe transformer matched power amplifier for operation at millimeter-wave frequencies," *Proceedings of the 31st European Solid-State Circuits Conference*, 2005, pp. 141-144.
- [19] T. Yao *et al.*, "Algorithmic Design of CMOS LNAs and PAs for 60-GHz Radio," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 1044-1057, May 2007.
- [20] D. Chowdhury *et al.*, "Design Considerations for 60 GHz Transformer-Coupled CMOS Power Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 10, pp. 2733-2744, Oct. 2009.
- [21] V. Vidojkovic *et al.*, "A low-power radio chipset in 40nm LP CMOS with beamforming for 60GHz high-data-rate wireless communication," *IEEE International Solid-State Circuits Conference*, 2013, pp. 236-237.
- [22] I. Sarkas *et al.*, "A 45nm SOI CMOS Class-D mm-Wave PA with >10V_{pp} differential swing," *IEEE International Solid-State Circuits Conference*, 2012, pp. 88-90.
- [23] K. Datta and H. Hashemi, "Performance Limits, Design and Implementation of mm-Wave SiGe HBT Class-E and Stacked Class-E Power Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 10, pp. 2150-2171, Oct. 2014.
- [24] T. Li and H. Wang, "A Continuous-Mode 23.5-41GHz Hybrid Class-F/F-1 Power Amplifier with 46% Peak PAE for 5G Massive MIMO Applications," *IEEE Radio Frequency Integrated Circuits Symposium*, 2018, pp. 220-230.
- [25] K. Khalaf *et al.*, "Digitally Modulated CMOS Polar Transmitters for Highly-Efficient mm-Wave Wireless Communication," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 7, pp. 1579-1592, July 2016.
- [26] S. Hu *et al.*, "2.1 A 28GHz/37GHz/39GHz multiband linear Doherty power amplifier for 5G massive MIMO applications," *IEEE International Solid-State Circuits Conference*, 2017, pp. 32-33.
- [27] D. Zhao *et al.*, "A 60-GHz Outphasing Transmitter in 40-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3172-3183, Dec. 2012.
- [28] A. Agah *et al.*, "Multi-Drive Stacked-FET Power Amplifiers at 90 GHz in 45 nm SOI CMOS," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 5, pp. 1148-1157, May 2014.
- [29] R. Bhat *et al.*, "Large-Scale Power Combining and Mixed-Signal Linearizing Architectures for Watt-Class mmWave CMOS Power Amplifiers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 2, pp. 703-718, Feb. 2015.
- [30] J. Jayamon *et al.*, "Spatially power-combined W-band power amplifier using stacked CMOS," *IEEE Radio Frequency Integrated Circuits Symposium*, 2014, pp. 151-154.

- [31] H. T. Nguyen *et al.*, "A 62-to-68GHz linear 6Gb/s 64QAM CMOS doherty radiator with 27.5%/20.1% PAE at peak/6dB-back-off output power leveraging high-efficiency multi-feed antenna-based active load modulation," *IEEE International Solid - State Circuits Conference*, 2018, pp. 402-404.
- [32] H. Park *et al.*, "An 81 GHz, 470 mW, 1.1 mm² InP HBT power amplifier with 4:1 series power combining using sub-quarter-wavelength baluns," *IEEE MTT-S International Microwave Symposium*, 2014, pp. 1-4.
- [33] J. Kim *et al.*, "V-band $\times 8$ Frequency Multiplier With Optimized Structure and High Spectral Purity Using 65-nm CMOS Process," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 5, pp. 506-508, May 2017.
- [34] T. Siriburanon *et al.*, "A Low-Power Low-Noise mm-Wave Subsampling PLL Using Dual-Step-Mixing ILFD and Tail-Coupling Quadrature Injection-Locked Oscillator for IEEE 802.11ad," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 5, pp. 1246-1260, May 2016.
- [35] C. Tsai *et al.*, "A 54-64.8 GHz subharmonically injection-locked frequency synthesizer with transmitter EVM between -26.5 dB and -28.8 dB in 28 nm CMOS," *43rd IEEE European Solid State Circuits Conference*, 2017, pp. 243-246.
- [36] V. Szortyka *et al.*, "21.4 A 42mW 230fs-jitter sub-sampling 60GHz PLL in 40nm CMOS," *IEEE International Solid-State Circuits Conference*, 2014, pp. 366-367.
- [37] A. I. Hussein *et al.*, "A 50-66-GHz Phase-Domain Digital Frequency Synthesizer With Low Phase Noise and Low Fractional Spurs," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3329-3347, Dec. 2017.
- [38] K. Khalaf *et al.*, "A 60-GHz 8-Way Phased-Array Front-End With T/R Switching and Calibration-Free Beamsteering in 28-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 7, pp. 2001-2011, July 2018.
- [39] M. Boers *et al.*, "20.2 A 16TX/16RX 60GHz 802.11ad chipset with single coaxial interface and polarization diversity," *IEEE International Solid-State Circuits Conference*, 2014, pp. 344-345.
- [40] S. Emami *et al.*, "A 60GHz CMOS phased-array transceiver pair for multi-Gb/s wireless communications," *IEEE International Solid-State Circuits Conference*, 2011, pp. 164-166.
- [41] Y. Yu *et al.*, "A 60 GHz Phase Shifter Integrated With LNA and PA in 65 nm CMOS for Phased Array Systems," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1697-1709, Sept. 2010.
- [42] G. Mangraviti *et al.*, "13.5 A 4-antenna-path beamforming transceiver for 60GHz multi-Gb/s communication in 28nm CMOS," *IEEE International Solid-State Circuits Conference*, 2016, pp. 246-247.
- [43] Y. Liu *et al.*, "A 28-GHz Transceiver Front-End with T/R Switching Achieving 11.2-dBm OP_{1dB}, 33.8% PAE_{max} and 4-dB NF in 22-nm FD-SOI for 5G Communication," *IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference*, 2018.
- [44] J. D. Dunworth *et al.*, "A 28GHz Bulk-CMOS dual-polarization phased-array transceiver with 24 channels for 5G user and basestation equipment," *IEEE International Solid - State Circuits Conference*, 2018, pp. 70-72.
- [45] H. Kim *et al.*, "A 28GHz CMOS direct conversion transceiver with packaged antenna arrays for 5G cellular system," *IEEE Radio Frequency Integrated Circuits Symposium*, 2017, pp. 69-72.
- [46] B. Sadhu *et al.*, "7.2 A 28GHz 32-element phased-array transceiver IC with concurrent dual polarized beams and 1.4 degree beam-steering resolution for 5G communication," *IEEE International Solid-State Circuits Conference*, 2017, pp. 128-129.
- [47] S. P. Voinigescu *et al.*, "Silicon D-band wireless transceivers and applications," *Asia-Pacific Microwave Conference*, 2010, pp. 1857-1864.
- [48] S. Hara *et al.*, "A 32Gbit/s 16QAM CMOS receiver in 300GHz band," *IEEE MTT-S International Microwave Symposium*, 2017, pp. 1703-1706.
- [49] K. Takano *et al.*, "17.9 A 105Gb/s 300GHz CMOS transmitter," *IEEE International Solid-State Circuits Conference*, 2017, pp. 308-309.
- [50] Z. Griffith *et al.*, "180-265 GHz, 17-24 dBm output power broadband, high-gain power amplifiers in InP HBT," *IEEE MTT-S International Microwave Symposium*, 2017, pp. 973-976.
- [51] B. P. Ginsburg *et al.*, "A 160 GHz Pulsed Radar Transceiver in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 4, pp. 984-995, April 2014.
- [52] H. J. Ng *et al.*, "A Fully-Integrated 77-GHz UWB Pseudo-Random Noise Radar Transceiver With a Programmable Sequence Generator in SiGe Technology," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 8, pp. 2444-2455, Aug. 2014.
- [53] S. Trotta *et al.*, "An RCP Packaged Transceiver Chipset for Automotive LRR and SRR Systems in SiGe BiCMOS Technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 3, pp. 778-794, March 2012.
- [54] H. Knapp *et al.*, "Three-channel 77 GHz automotive radar transmitter in plastic package," *IEEE Radio Frequency Integrated Circuits Symposium*, 2012, pp. 119-122.
- [55] H. P. Forstner *et al.*, "A 77GHz 4-channel automotive radar transceiver in SiGe," *IEEE Radio Frequency Integrated Circuits Symposium*, 2008, pp. 233-236.
- [56] H. Jia *et al.*, "A 77 GHz Frequency Doubling Two-Path Phased-Array FMCW Transceiver for Automotive Radar," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 10, pp. 2299-2311, Oct. 2016.
- [57] J. Oh *et al.*, "A W-Band 4-GHz Bandwidth Phase-Modulated Pulse Compression Radar Transmitter in 65-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 8, pp. 2609-2618, Aug. 2015.
- [58] J. Jang *et al.*, "A 79-GHz Adaptive-Gain and Low-Noise UWB Radar Receiver Front-End in 65-nm CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 3, pp. 859-867, March 2016.
- [59] B. P. Ginsburg *et al.*, "A multimode 76-to-81GHz automotive radar transceiver with autonomous monitoring," *IEEE International Solid - State Circuits Conference*, 2018, pp. 158-160.
- [60] V. Giannini *et al.*, "A 79 GHz Phase-Modulated 4 GHz-BW CW Radar Transmitter in 28 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 12, pp. 2925-2937, Dec. 2014.
- [61] D. Guermandi *et al.*, "A 79-GHz 2×2 MIMO PMCW Radar SoC in 28-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 10, pp. 2613-2626, Oct. 2017.
- [62] D. Cherniak *et al.*, "A 23GHz low-phase-noise digital bang-bang PLL for fast triangular and saw-tooth chirp modulation," *IEEE International Solid - State Circuits Conference*, 2018, pp. 248-250.
- [63] J. Vovnoboy *et al.*, "A Dual-Loop Synthesizer With Fast Frequency Modulation Ability for 77/79 GHz FMCW Automotive Radar Applications," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 5, pp. 1328-1337, May 2018.
- [64] Q. Shi *et al.*, "A Self-Calibrated 16GHz Subsampling-PLL-Based 30 μ s Fast Chirp FMCW Modulator with 1.5GHz Bandwidth and 100kHz rms Error," *IEEE International Solid - State Circuits Conference*, 2019.
- [65] B. Heydari *et al.*, "Millimeter-Wave Devices and Circuit Blocks up to 104 GHz in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2893-2903, Dec. 2007.
- [66] I. Nasr *et al.*, "A Highly Integrated 60 GHz 6-Channel Transceiver With Antenna in Package for Smart Sensing and Short-Range Communications," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 9, pp. 2066-2076, Sept. 2016.
- [67] J. Grzyb *et al.*, "A 210-270-GHz Circularly Polarized FMCW Radar With a Single-Lens-Coupled SiGe HBT Chip," *IEEE Transactions on Terahertz Science and Technology*, vol. 6, no. 6, pp. 771-783, Nov. 2016.
- [68] A. Visweswaran *et al.*, "A 145GHz FMCW-Radar Transceiver in 28nm CMOS," *IEEE International Solid - State Circuits Conference*, 2019.
- [69] K. Schmalz *et al.*, "Gas Spectroscopy System for Breath Analysis at mm-wave/THz Using SiGe BiCMOS Circuits," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 5, pp. 1807-1818, May 2017.
- [70] Q. Zhong *et al.*, "25.2 A 210-to-305GHz CMOS receiver for rotational spectroscopy," *IEEE International Solid-State Circuits Conference*, 2016, pp. 426-427.
- [71] C. Wang *et al.*, "17.6 Rapid and energy-efficient molecular sensing using dual mm-Wave combs in 65nm CMOS: A 220-to-320GHz spectrometer with 5.2mW radiated power and 14.6-to-19.5dB noise figure," *IEEE International Solid-State Circuits Conference*, 2017, pp. 302-303.
- [72] S. S. Ahmed *et al.*, "A Novel Fully Electronic Active Real-Time Imager Based on a Planar Multistatic Sparse Array," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 12, pp. 3567-3576, Dec. 2011.
- [73] K. Sengupta *et al.*, "Silicon Integrated 280 GHz Imaging Chipset With 4×4 SiGe Receiver Array and CMOS Source," *IEEE Transactions on Terahertz Science and Technology*, vol. 5, no. 3, pp. 427-437, May 2015.
- [74] C. Jiang *et al.*, "25.5 A 320GHz subharmonic-mixing coherent imager in 0.13 μ m SiGe BiCMOS," *IEEE International Solid-State Circuits Conference*, 2016, pp. 432-434.
- [75] K. Statnikov *et al.*, "160-GHz to 1-THz Multi-Color Active Imaging With a Lens-Coupled SiGe HBT Chip-Set," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 520-532, Feb. 2015.
- [76] T. Chi *et al.*, "17.7 A packaged 90-to-300GHz transmitter and 115-to-325GHz coherent receiver in CMOS for full-band continuous-wave mm-wave hyperspectral imaging," *IEEE International Solid-State Circuits Conference*, 2017, pp. 304-305.