

# **INTEL ARRIA 10 GX DEV KIT PCIE GEN3x8 DMA ON NVIDIA XAVIER SYSTEM**

# INTEL ARRIA 10 GX DEV KIT – PCIE GEN3x8 DMA

## ■ System Set-Up

1. Nvidia Jetson Xavier PCIe Root Port
2. FPGA ARRIA 10 GX Dev Kit
3. OS: Ubuntu 18.04 Release tegra-l4t-r32.2.0
4. Quartus Prime Pro 19.2



# INTEL ARRIA 10 GX DEV KIT – PCIE GEN3x8 DMA

## GITHUB – Configuration Management

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Description

FPGA Design

Website

Website for this repository (optional)

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1 branch

0 releases

1 contributor

Branch: master

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ebots-hung First commit

Latest commit 0ef7f2c 1 hour ago

|  |              |            |
|--|--------------|------------|
| 00_FPGA_Design/Arria10_PCIEGen3x8_DMA_19_2_project | First commit | 1 hour ago |
| 01_Software_driver                                 | First commit | 1 hour ago |
| 02_Logging_Debugging                               | First commit | 1 hour ago |
| 03_Test_result                                     | First commit | 1 hour ago |

Help people interested in this repository understand your project by adding a README.

Add a README

<https://github.com/ebots-inc/FPGA>

FPGA – Hard IP PCIE Configuration

File Edit System Generate View Tools Help

Filter IP Catalog

Device Family

Project

- New Component...
- System
  - Basic Functions
  - Bridges and Adapters
  - DSP
  - Generic Component
  - Intel FPGA Interconnect
  - Interface Protocols
  - Low Power
  - Memory Interfaces and Controllers
  - Processors and Peripherals
  - University Program
- Existing IP Variants
  - media

System View Address Map Details

System: top\_hw Path: DUT

Use

Connections

clk 0

- clk
- clk\_in
- clk\_in\_reset
- clk\_reset

emif 0

- ctrl\_amm\_0
- emif\_usr\_clk
- emif\_usr\_reset\_n
- global\_reset\_n
- mem
- oct
- pll\_ref\_clk
- status

DUT

- app\_nreset\_status
- corelkout\_hip
- dma\_rd\_master
- dma\_wr\_master
- hip\_ctrl
- hip\_pipe
- hip\_serial
- npwr

DUT.hip serial

- Conduit[conduit\_end 19.2]
- Associated clock: None (asynchronous)
- Click to remove export

onchip\_memory2\_0

- clk1
- clk2
- reset1
- reset2

Remove

Name

Description

Clock Source

- Clock Output
- Clock Input
- Reset Input
- Reset Output

External Memory Interface

- Avalon Memory Mapped Slave
- Clock Output
- Reset Input
- Reset Output
- Conduit
- Conduit
- Clock Input
- Conduit

Intel Arria 10/Cyclone 10

- Reset Output
- Clock Output
- Avalon Memory Mapped Master
- Avalon Memory Mapped Master
- Avalon Memory Mapped Master
- Avalon Memory Mapped Master
- Avalon Memory Mapped Master
- Avalon Memory Mapped Master
- On-Chip Memory (RAM)
- Clock Input
- Clock Input
- Reset Input
- Reset Input

Current filter: All Interfaces

System Messages Generation Messages

| Type    | Path                              | Message                                |
|---------|-----------------------------------|--|
| Warning | 1 Component Instantiation Warning |  |
| Warning | top_hw.emif_0                     | Warnings found in IP parameterization. |

New... Edit... Add...

Component Instantiation: 0 Errors, 1 Warning, System Connectivity: 0 Errors, 0 Warnings

Parameters System Info Component Instantiation Domains

System: top\_hw Path: DUT

HDL entity name: top\_DUT IP file: ip/top\_hw/top\_DUT.ip

Any changes here will be written out to disk when the system is saved.

Intel Arria 10/Cyclone 10 Hard IP for PCI Express

- altera\_pcie\_a10\_hip
- Details
- Generate Example Design...

Design Environment

- This component supports multiple interface views:
- System

IP Settings Example Designs

PCI Express / PCI Capabilities Configuration, Debug and Extension Options PHY Characteristics

System Settings Avalon-MM Settings Base Address Registers Device Identification Registers

Application interface type: Avalon-MM with DMA

Hard IP mode: Gen3:x8, Interface: 256-bit, 250 MHz

Port type: Native endpoint

RX buffer credit allocation for received requests vs completions: Low

RX Buffer completion credits: Header:195 Data:773

Parameterization Messages

| Type    | Message                               |
|---------|---------------------------------------|
| Warning | device_family is Arria 10             |
| Warning | part_trait_device is 10AX115S2F45I1SG |
| Warning | Gen3 (8.0 Gbps) x8 256-bit            |

Sync System Infos Auto Validate System Integrity Generate HDL...

App I/F: Avalon-MM with DMA  
IP mode: Gen3:x8, i/f 256 bit, 250Mhz  
Port: Native Endpoint

FPGA – Hard IP PCIE Configuration (cont.)

System View

Address Map

Details

System: top\_hw Path: DUT

Use

Connections

Name

Description

clk\_0

clk

clk\_in

clk\_in\_reset

clk\_reset

emif\_0

ctrl\_amm\_0

emif\_usr\_clk

emif\_usr\_reset\_n

global\_reset\_n

mem

oct

pll\_ref\_clk

status

DUT

app\_nreset\_status

coreclkout\_hip

dma\_rd\_master

dma\_wr\_master

hip\_ctrl

hip\_pipe

hip\_serial

npwr

rd\_dcm\_master

rd\_dts\_slave

refclk

rxm\_bar2

txs

wr\_dcm\_master

wr\_dts\_slave

onchip\_memory2\_0

clk1

clk2

reset1

reset2

Clock Source

Clock Output

Clock Input

Reset Input

Reset Output

External Memory Interface

Avalon Memory Mapped Slave

Clock Output

Reset Output

Reset Input

Conduit

Conduit

Clock Input

Conduit

Intel Arria 10/Cyclone 10

Reset Output

Clock Output

Avalon Memory Mapped Master

Avalon Memory Mapped Master

Conduit

Conduit

Conduit

Avalon Memory Mapped Master

Avalon Memory Mapped Slave

Clock Input

Avalon Memory Mapped Master

Avalon Memory Mapped Slave

Avalon Memory Mapped Master

Avalon Memory Mapped Slave

On-Chip Memory (RAM or

Clock Input

Clock Input

Reset Input

Reset Input

System: top\_hw Path: DUT

HDL entity name: top\_DUT IP file: ip/top\_hw/top\_DUT.ip

Any changes here will be written out to disk when the system is saved.

Intel Arria 10/Cyclone 10 Hard IP for PCI Express

altera\_pcie\_a10\_hip

Details

Generate Example Design...

Design Environment

This component supports multiple interface views:

System

IP Settings

Example Designs

PCI Express / PCI Capabilities

Configuration, Debug and Extension Options

PHY Characteristics

System Settings

Avalon-MM Settings

Base Address Registers

Device Identification Register

BAR0

BAR1

BAR2

BAR3

BAR4

BAR5

Type: 64-bit prefetchable memory

Size: 0 bit

BAR0: 64-bit prefetchable memory

BAR2: 64-bit prefetchable memory

BAR1,3,4,5: disable

FPGA – Hard IP PCIE Configuration (cont.)

System ViewAddress MapDetailsSystem: top\_hw Path: DUT

UseConnectionsNameDescription

clk\_0

clk

clk\_in

clk\_in\_reset

clk\_reset

emif\_0

ctrl\_amm\_0

emif\_usr\_clk

emif\_usr\_reset\_n

global\_reset\_n

mem

oct

pll\_ref\_clk

status

Intel Arria 10/Cyclone 10

app\_nreset\_status

coreclkout\_hip

dma\_rd\_master

dma\_wr\_master

hip\_ctrl

hip\_pipe

hip\_serial

npwr

rd\_dcm\_master

rd\_dts\_slave

refclk

rxm\_bar2

txs

wr\_dcm\_master

wr\_dts\_slave

onchip\_memory2\_0

clk1

clk2

reset1

reset2

Clock Source

Clock Output

Clock Input

Reset Input

Reset Output

External Memory Interface

Avalon Memory Mapped Slave

Clock Output

Reset Output

Reset Input

Conduit

Conduit

Clock Input

Conduit

Intel Arria 10/Cyclone 10

Reset Output

Clock Output

Avalon Memory Mapped Master

Avalon Memory Mapped Master

Conduit

Conduit

Conduit

Conduit

Avalon Memory Mapped Master

Avalon Memory Mapped Slave

Avalon Memory Mapped Slave

Clock Input

Avalon Memory Mapped Master

Avalon Memory Mapped Master

Avalon Memory Mapped Master

Avalon Memory Mapped Slave

On-Chip Memory (RAM)

Clock Input

Clock Input

Reset Input

Reset Input

Current filter: All Interfaces

ParametersSystem InfoComponent InstantiationDomainsSystem: top\_hw Path: DUT

HDL entity name: top\_DUTIP file: ip/top\_hw/top\_DUT.ip

Any changes here will be written out to disk when the system is saved.

Intel Arria 10/Cyclone 10 Hard IP for PCI Express

altera\_pcie\_a10\_hip

Design Environment

This component supports multiple interface views:

System

IP SettingsExample Designs

PCI Express / PCI CapabilitiesConfiguration, Debug and Extension OptionsPHY Characteristics

System SettingsAvalon-MM SettingsBase Address RegistersDevice Identification Registers

Physical Function 0 IDs

Vendor ID: 0x00001172

Device ID: 0x0000e003

Revision ID: 0x00000001

Class code: 0x00ff0000

Subsystem Vendor ID: 0x00000000

Subsystem Device ID: 0x00000000

VF Subsystem Device ID: 0x00000000

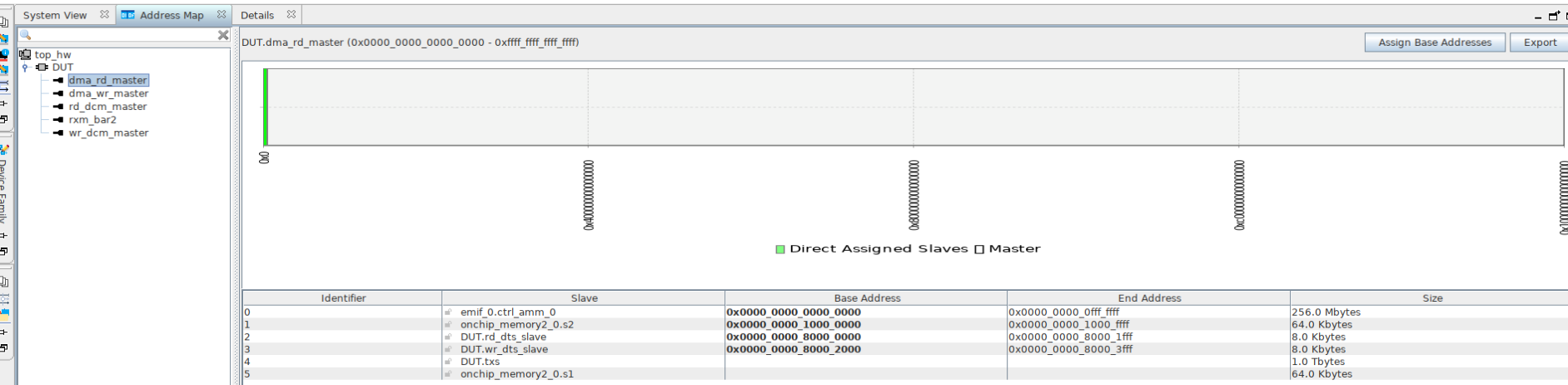
Vendor ID: 0x1172 → Intel ID

Device ID: 0xe003

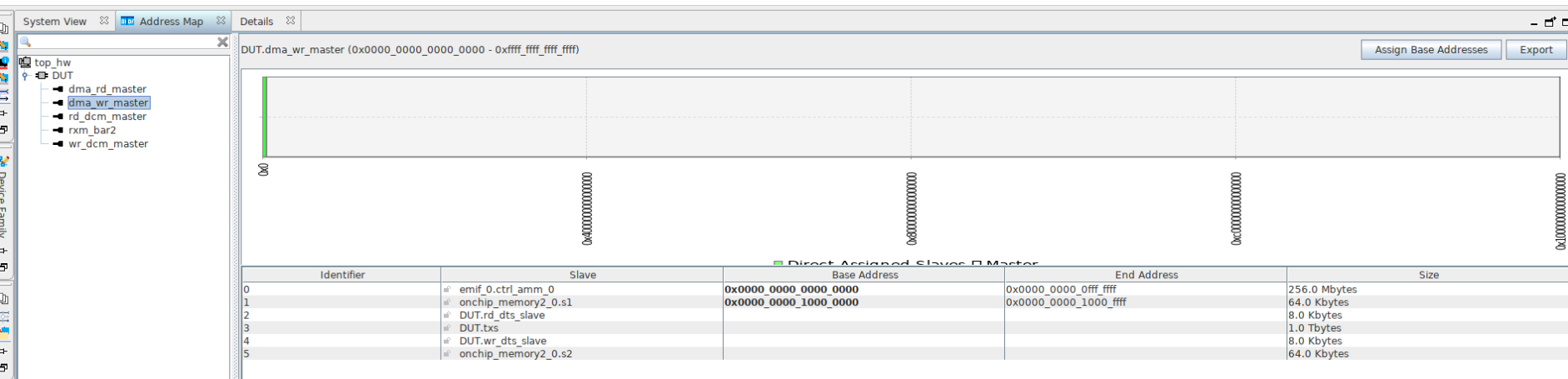
Revision ID: 0x1

Class code: 0x00ff0000

FPGA – Memory Map



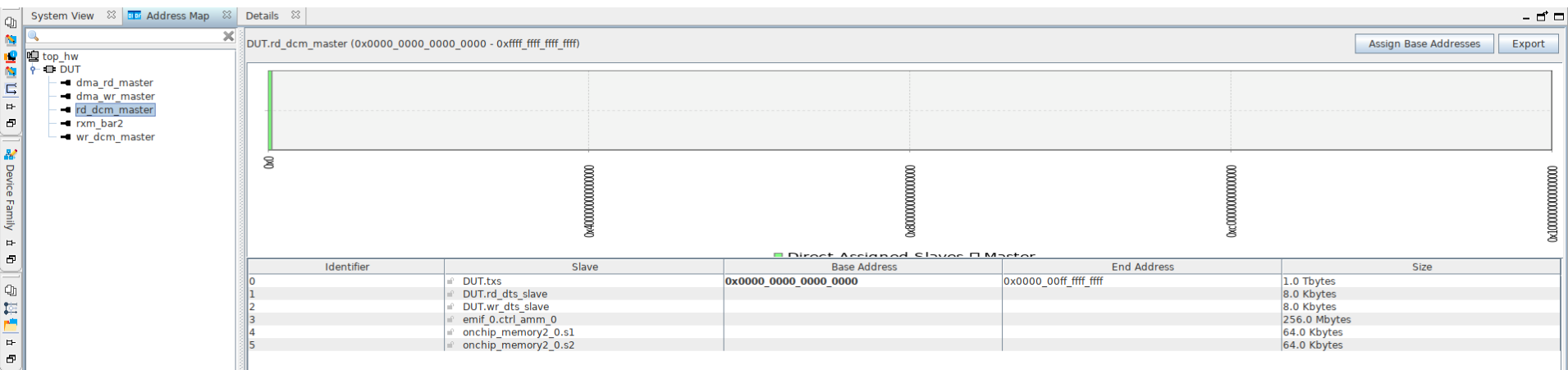
dma\_rd\_master: 0x0000\_0000\_0000\_0000 → 0xffff\_ffff\_ffff\_ffff



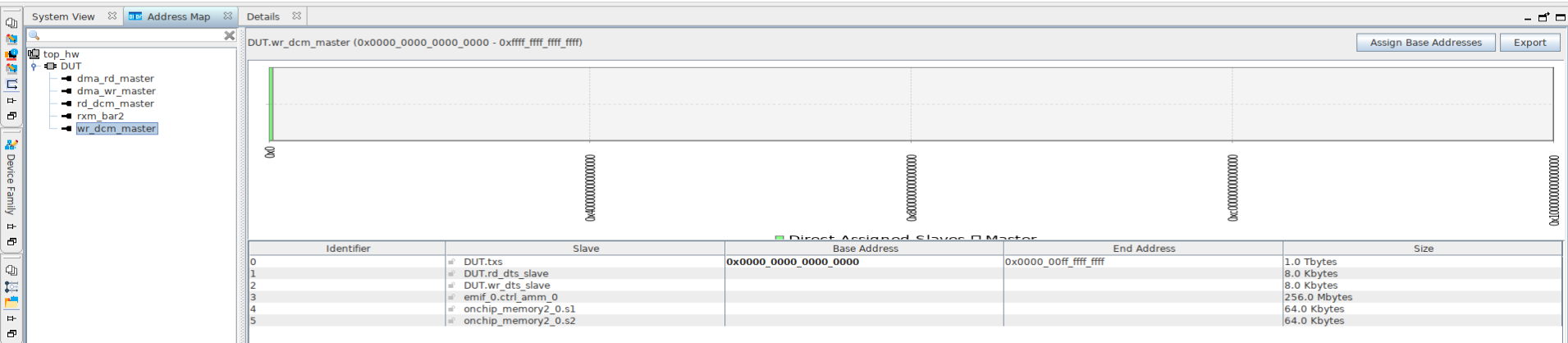
dma\_wr\_master: 0x0000\_0000\_0000\_0000 → 0xffff\_ffff\_ffff\_ffff



FPGA – Memory Map (cont.)



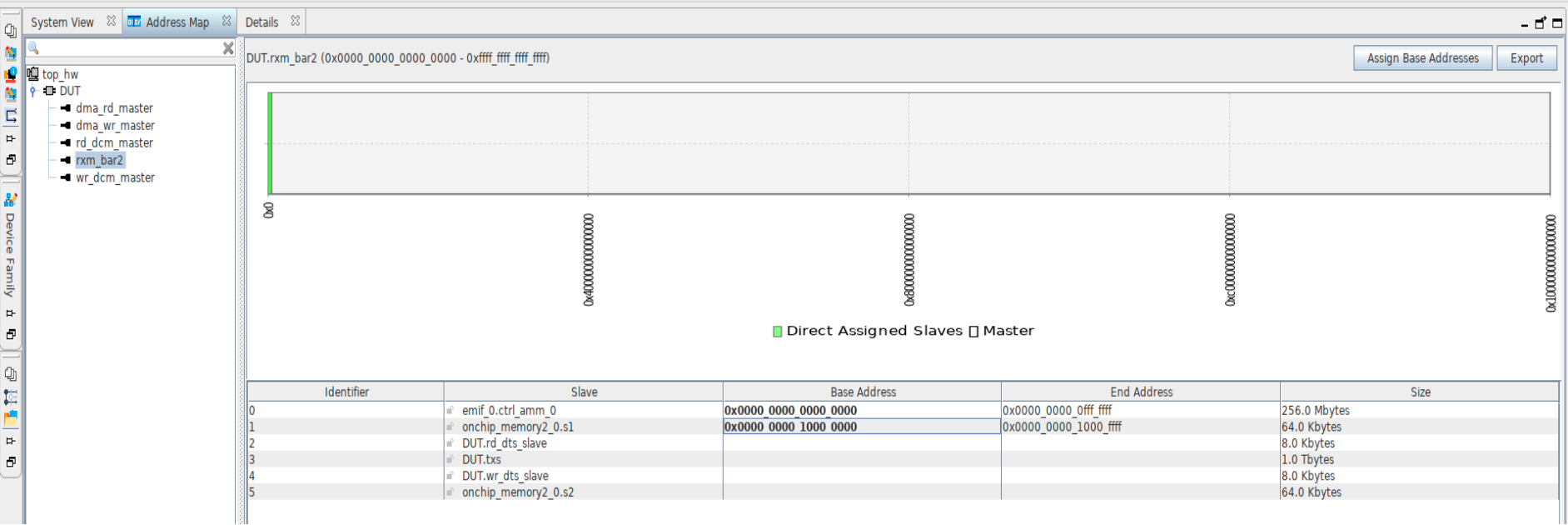
rd\_dcm\_master: 0x0000\_0000\_0000\_0000 → 0xffff\_ffff\_ffff\_ffff



wr\_dcm\_master: 0x0000\_0000\_0000\_0000 → 0xffff\_ffff\_ffff\_ffff



FPGA – Memory Map (cont.)



Rxm\_bar2: 0x0000\_0000\_0000\_0000 → 0xffff\_ffff\_ffff\_ffff

| Slave               | Base Addr.            | End Addr.             | Size  |
|---------------------|-----------------------|-----------------------|-------|
| Emif_0.ctrl_amm_0   | 0x0000_0000_0000_0000 | 0x0000_0000_0fff_ffff | 256MB |
| Onchip_memory2_0.s1 | 0x0000_0000_1000_0000 | 0x0000_0000_1000_ffff | 64KB  |
| Rd_dts_slave        |                       |                       | 8KB   |
| txs                 |                       |                       | 1TB   |

# INTEL ARRIA 10 GX DEV KIT – PCIE GEN3x8 DMA

- NVIDA JETSON XAVIER – PCIE device driver

Intel Arria 10/Cyclone 10 Hard IP for PCI Express

altera\_pcie\_a10\_hip

Details

Generate Example Design...

Design Environment

This component supports multiple interface views:

System

IP Settings

Example Designs

PCI Express / PCI Capabilities

Configuration, Debug and Extension Options

PHY Characteristics

System Settings

Avalon-MM Settings

Base Address Registers

Device Identification Registers

Physical Function 0 IDs

Vendor ID: 0x00001172

Device ID: 0x0000e003

Revision ID: 0x00000001

Class code: 0x00ff0000

Subsystem Vendor ID: 0x00000000

Subsystem Device ID: 0x00000000

VF Subsystem Device ID: 0x00000000

IDs matching

altera\_dma\_cmd.h

1 #ifndef ALTERA\_DMA\_CMD\_H

2 #define ALTERA\_DMA\_CMD\_H

3

4 #define ALTERA\_DMA\_DRIVER\_VERSION "2.02"

5

6 #define ALTERA\_DMA\_DID 0xE003

7 #define ALTERA\_DMA\_VID 0x1172

8

■ NVIDIA JETSON XAVIER – PCIE device list

BAR0, BAR2 mapped successfully

PCIe max-speed: 8GT/s

```
PTMclockGranularity: 16ns
PTMControl: Enabled- RootSelected-
PTMEffectiveGranularity: Unknown
Capabilities: [320 v1] Vendor Specific Information: ID=0004 Rev=1 Len=054 <?>
Kernel driver in use: pcieport

0005:01:00.0 Unassigned class [ff00]: Altera Corporation Device e003 (rev 01)
Control: I/O- Mem+ BusMaster+ SpecCycle- MemMIO+ VgaSnoop- ParErr- Stepping- SERR- FastB2B- DisINTx+
Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=Fast >TAbort- <TAbort- <MAbort- >SERR- <PERR- INTx-
Latency: 0
Interrupt: pin A routed to IRQ 819
Region 0: Memory at 1c20000000 (64-bit, prefetchable) [size=512M]
Region 2: Memory at 1c00000000 (64-bit, prefetchable) [size=512M]
Capabilities: [100 v1] MSI: Enable+ Count=1/4 Maskable- 64bit+
Address: 00000000ffff0000 Data: 0000
Capabilities: [78] Power Management version 3
Flags: PMEClk- DSI- D1- D2- AuxCurrent=0mA PME(D0-,D1-,D2-,D3hot-,D3cold-)
Status: D0 NoSoftRst- PME-Enable- DSel=0 DSscale=0 PME-
Capabilities: [80] Express (v2) Endpoint, MSI 00
DevCap: MaxPayload 256 bytes, PhantFunc 0, Latency L0s <64ns, L1 <1us
ExtTag- AttnBttn- AttnInd- PwrInd- RBE+ FLReset- SlotPowerLimit 0.000W
DevCtl: Report errors: Correctable- Non-Fatal- Fatal- Unsupported-
RlxdOrd- ExtTag- PhantFunc- AuxPwr- NoSnoop-
MaxPayload 256 bytes, MaxReadReq 512 bytes
DevSta: CorrErr- UncorrErr- FatalErr- UnsuppReq- AuxPwr- TransPend-
LnkCap: Port #1, Speed 8GT/s, Width x8, ASPM not supported, Exit Latency L0s <4us, L1 <1us
ClockPM- Surprise- LLActRep- BwNot- ASPMOptComp+
LnkCtl: ASPM Disabled; RCB 64 bytes Disabled- CommClk+
ExtSynch- ClockPM- AutWidDis- BWInt- AutBWInt-
LnkSta: Speed 8GT/s, Width x8, TrErr- Train- SlotClk- DLActive- BWMgmt- ABWMgmt-
DevCap2: Completion Timeout: Not Supported, TimeoutDis+, LTR-, OBFF Not Supported
DevCtl2: Completion Timeout: 50us to 50ms, TimeoutDis+, LTR-, OBFF Disabled
LnkCtl2: Target Link Speed: 8GT/s, EnterCompliance- SpeedDis-
Transmit Margin: Normal Operating Range, EnterModifiedCompliance- ComplianceSOS-
Compliance De-emphasis: -6dB
LnkSta2: Current De-emphasis Level: -6dB, EqualizationComplete+, EqualizationPhase1+
EqualizationPhase2+, EqualizationPhase3+, LinkEqualizationRequest-
Capabilities: [100 v1] Virtual Channel
Caps: LPEVC=0 RefClk=100ns PATEntryBits=1
Arb: Fixed- WRR32- WRR64- WRR128-
Ctrl: ArbSelect=Fixed
Status: InProgress-
VC0: PATOffset=00 MaxTimeSlots=1 RejSnoopTrans-
Arb: Fixed- WRR32- WRR64- WRR128- TWRR128- WRR256-
Ctrl: Enable+ ID=0 ArbSelect=Fixed TC/VC=ff
Status: NegoPending- InProgress-
Capabilities: [200 v1] Vendor Specific Information: ID=1172 Rev=0 Len=044 <?>
Capabilities: [300 v1] #19
Capabilities: [800 v1] Advanced Error Reporting
UESta: DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC- UnsupReq- ACSViol-
UEmsk: DLP+ SDES+ TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC- UnsupReq- ACSViol-
UESvrt: DLP+ SDES+ TLP- FCP+ CmpltTO- CmpltAbrt- UnxCmplt- RxOF+ MalfTLP+ ECRC- UnsupReq- ACSViol-
CESta: RxErr- BadTLP- BadDLLP- Rollover- Timeout- NonFatalErr-
CEMsk: RxErr- BadTLP- BadDLLP- Rollover- Timeout- NonFatalErr+
ASPM: First Error Pointer: 00. GenCap- CGenEn- ChkCap- ChkEn-

$ sudo lspci -vvv
```

```
altera_dma_cmd.h x altera_dma.h x
#ifndef ALTERA_DMA_H
#define ALTERA_DMA_H

#define ALTERA_DMA_DRIVER_NAME "Altera DMA"
#define ALTERA_DMA_DEVFILE "altera_dma"
```

## ■ NVIDIA JETSON XAVIER – System Log

[ 9.237954] pcie-tegra.c:nvidia,max-speed is 4 | NOTE: 1: Gen1, 2: Gen2, 3: Gen3, 4: Gen4

[ 9.238134] tegra-pcie-dw 141a0000.pcie: PCIe max-speed check

[ 9.239524] tegra-pcie-dw 141a0000.pcie: Setting init speed to max speed

[ 9.241998] OF: PCI: host bridge /pcie@141a0000 ranges:

[ 9.243436] OF: PCI: IO 0x3a100000..0x3a1fffff -> 0x3a100000

[ 9.244864] OF: PCI: MEM 0x1f40000000..0x1fffffff -> 0x40000000

[ 9.248309] OF: PCI: MEM 0x1c00000000..0x1f3fffffff -> 0x1c00000000

[ 9.877487] tegra-pcie-dw 141a0000.pcie: link is up

[ 9.879186] tegra-pcie-dw 141a0000.pcie: PCI host bridge to bus 0005:00

[ 9.880634] pci\_bus 0005:00: root bus resource [bus 00-ff]

[ 9.882050] pci\_bus 0005:00: root bus resource [io 0x300000-0x3fffff] (bus address [0x3a100000-0x3a1fffff])

[ 9.883533] pci\_bus 0005:00: root bus resource [mem 0x1f40000000-0x1fffffff] (bus address [0x40000000-0xffffffff])

[ 9.885015] pci\_bus 0005:00: root bus resource [mem 0x1c00000000-0x1f3fffffff pref]

....

[ 9.888533] pci 0005:01:00.0: [1172:e003] type 00 class 0xff0000

[ 9.888645] pci 0005:01:00.0: reg 0x10: [mem 0x00000000-0x000001ff 64bit pref]

[ 9.888717] pci 0005:01:00.0: reg 0x18: [mem 0x00000000-0x1fffffff 64bit pref]

[ 9.889528] iommu: Adding device 0005:01:00.0 to group 64

[ 9.902405] pci 0005:00:00.0: BAR 15: assigned [mem 0x1c00000000-0x1c2fffffff 64bit pref]

[ 9.904273] pci 0005:01:00.0: BAR 2: assigned [mem 0x1c00000000-0x1c1fffffff 64bit pref]

[ 9.906370] pci 0005:01:00.0: BAR 0: assigned [mem 0x1c20000000-0x1c200001ff 64bit pref]

[ 9.907790] pci 0005:00:00.0: PCI bridge to [bus 01-ff]

[ 9.909119] pci 0005:00:00.0: bridge window [mem 0x1c00000000-0x1c2fffffff 64bit pref]

[ 9.910515] pci 0005:00:00.0: Max Payload Size set to 256/ 256 (was 256), Max Read Rq 512

[ 9.911969] pci 0005:01:00.0: Max Payload Size set to 256/ 256 (was 128), Max Read Rq 512

## ■ NVIDIA JETSON XAVIER – System Log

```
[ 317.624493] altera_dma: loading out-of-tree module taints kernel.  
[ 317.625486] Altera DMA: altera_dma_init(), Aug 14 2019 10:45:01  
[ 317.625831] Altera DMA 0005:01:00.0: enabling device (0000 -> 0002)  
[ 317.625867] Altera DMA 0005:01:00.0: pci_enable_device() successful  
[ 317.626173] Altera DMA 0005:01:00.0: pci_enable_msi() successful  
[ 317.626206] Altera DMA 0005:01:00.0: using a 64-bit irq mask  
[ 317.626213] Altera DMA 0005:01:00.0: irq pin: 1  
[ 317.626219] Altera DMA 0005:01:00.0: irq line: 0  
[ 317.626225] Altera DMA 0005:01:00.0: irq: 819  
[ 317.626231] Altera DMA 0005:01:00.0: request irq: 0  
[ 317.626240] Altera DMA 0005:01:00.0: BAR[0] 0x1c20000000-0x1c200001ff flags 0x0014220c, length 512  
[ 317.626258] Altera DMA 0005:01:00.0: BAR[1] 0x00000000-0x00000000 flags 0x00000000, length 0  
[ 317.626272] Altera DMA 0005:01:00.0: BAR[2] 0x1c00000000-0x1c1ffffff flags 0x0014220c, length 536870912  
[ 317.626286] Altera DMA 0005:01:00.0: BAR[3] 0x00000000-0x00000000 flags 0x00000000, length 0  
[ 317.626295] Altera DMA 0005:01:00.0: BAR[4] 0x00000000-0x00000000 flags 0x00000000, length 0  
[ 317.626303] Altera DMA 0005:01:00.0: BAR[5] 0x00000000-0x00000000 flags 0x00000000, length 0  
[ 317.627586] Altera DMA 0005:01:00.0: BAR[0] mapped to 0xfffff800dbfc000, length 512  
[ 317.627766] Altera DMA 0005:01:00.0: BAR[2] mapped to 0xfffff8060000000, length 536870912
```

## ■ DMA Test Result – PCIe Gen1x8

- Length of Transfer: **2048KB**
- Read Throughput: **1.53GB/s**
- Write Throughput: **1.61GB/s**
- Simultaneous Throughput: **2.9GB/s**

```
*****
** ALTERA 256b DMA driver                      **
** version 2.02                                **
** 1) start DMA                                **
** 2) enable/disable read dma                  **
** 3) enable/disable write dma                 **
** 4) enable/disable simul dma                 **
** 5) set num dwords (256 - 4096)              **
** 6) set num descriptors (1 - 127)            **
** 7) toggle on-chip or off-chip memory        **
** 8) loop dma                                **
** 10) exit                                    **
*****
Access On Chip RAM      ? 1
Run Read                 ? 1
Run Write                ? 1
Run Simultaneous        ? 1
Read Passed              ? 1
Write Passed             ? 1
Simultaneous Passed     ? 1
Read EPLast timeout     ? 0
Write EPLast timeout    ? 0
Number of Dwords/Desc   : 4096
Number of Descriptors   : 128
Length of transfer      : 2048 KB
Rootport address offset : 0
Read Time                : 0 s and 1274 us
Read Throughput          : 1.533589 GB/S
Write Time               : 0 s and 1211 us
Write Throughput         : 1.613371 GB/S
Simultaneous Time       : 0 s and 1344 us
Simultaneous Throughput : 2.907429 GB/S
# Press ESC to stop
█
```



## ■ DMA Test Result – PCIe Gen3x8

- Length of Transfer: **2048KB**
- Read Throughput: **4.59GB/s**
- Write Throughput: **6.30GB/s**
- Simultaneous Throughput: **7.74GB/s**

```
*****
** ALTERA 256b DMA driver                               **
** version 2.02                                           **
** 1) start DMA                                           **
** 2) enable/disable read dma                             **
** 3) enable/disable write dma                           **
** 4) enable/disable simul dma                           **
** 5) set num dwords (256 - 4096)                         **
** 6) set num descriptors (1 - 127)                       **
** 7) toggle on-chip or off-chip memory                  **
** 8) loop dma                                            **
** 10) exit                                               **
*****
Access On Chip RAM      ? 1
Run Read                 ? 1
Run Write                ? 1
Run Simultaneous         ? 1
Read Passed              ? 1
Write Passed             ? 1
Simultaneous Passed      ? 1
Read EPLast timeout     ? 0
Write EPLast timeout     ? 0
Number of Dwords/Desc   : 4096
Number of Descriptors   : 128
Length of transfer      : 2048 KB
Rootport address offset : 0
Read Time                : 0 s and 426 us
Read Throughput          : 4.586366 GB/S
Write Time               : 0 s and 310 us
Write Throughput         : 6.302555 GB/S
Simultaneous Time        : 0 s and 505 us
Simultaneous Throughput  : 7.737790 GB/S
# Press ESC to stop
█
```



■ DMA Test Result – PCIe Gen3x8 with External Memory DDR3 ( 2133Mbps, x64 bus width)

- Length of Transfer: **2048KB**
- Read Throughput: **4.65GB/s**
- Write Throughput: **3.54GB/s**
- Simultaneous Throughput: **4.57GB/s**

**Throughput Differences for On-Chip and External Memory**

*This reference design provides a choice between on-chip memory implemented in the FPGA fabric and external memory available on the PCB. The on-chip memory supports separate read and write ports. Consequently, this memory supports simultaneous read and the write DMAs.*

*The external memory supports a single port. Consequently, the external memory does not support simultaneous read DMA and write DMA accesses. In addition, the latency of external memory is higher than the latency of on-chip memory. These two differences between the on-chip and external memory result in lower throughput for the external memory implementation.*

Source @AN 829: PCI Express\* Avalon®-MM DMA Reference Design

```
*****
** ALTERA 256b DMA driver                               **
** version 2.02                                         **
** 1) start DMA                                         **
** 2) enable/disable read dma                          **
** 3) enable/disable write dma                        **
** 4) enable/disable simul dma                       **
** 5) set num dwords (256 - 4096)                     **
** 6) set num descriptors (1 - 127)                   **
** 7) toggle on-chip or off-chip memory               **
** 8) loop dma                                         **
** 10) exit                                             **
*****
Access On Chip RAM      ? 0
Run Read                ? 1
Run Write               ? 1
Run Simultaneous        ? 1
Read Passed             ? 1
Write Passed            ? 1
Simultaneous Passed     ? 0
Read EPLast timeout     ? 0
Write EPLast timeout    ? 0
Number of Dwords/Desc   : 4096
Number of Descriptors   : 128
Length of transfer      : 2048 KB
Rootport address offset : 0
Read Time               : 0 s and 420 us
Read Throughput         : 4.651886 GB/S
Write Time              : 0 s and 552 us
Write Throughput        : 3.539478 GB/S
Simultaneous Time       : 0 s and 856 us
Simultaneous Throughput : 4.564935 GB/S
#
```

# INTEL ARRIA 10 GX DEV KIT – PCIE GEN3x8 DMA

▪ Comparison table – PCIe Gen3x8 DMA ( RP: x86 vs ARM, DMA: OCM vs DDR3/DDR4)

|                         | On-Chip-Memory     |          | DDR3       |          | DDR4               |            |
|-------------------------|--------------------|----------|------------|----------|--------------------|------------|
|                         | X86 <sup>(1)</sup> | ARM      | x86        | ARM      | x86 <sup>(2)</sup> | ARM        |
| Read                    | 6.38GB/s           | 4.59GB/s | Not tested | 4.65GB/s | 6.62GB/s           | Not tested |
|                         | 79.75%             | 57.38%   |            | 58.12%   | 82.75%             |            |
| Write                   | 6.34GB/s           | 6.3GB/s  | Not tested | 3.54GB/s | 6.26GB/s           | Not tested |
|                         | 79.25%             | 78.75%   |            | 44.25%   | 78.25%             |            |
| Simultaneous Read/Write | 11.69GB/s          | 7.74GB/s | Not tested | 4.56GB/s | 4.05GB/s           | Not tested |

**NOTE**

DDR3 Specification: Running at 1066Mhz, BW at 2133Mbps, Bus width x64  
DDR4 Specification: Running at 1200Mhz, BW at 2400Mbps, Bus width x64  
ARM based System: Nvidia Jetson Xavier

Source @  
(1) AN 829: PCI Express\* Avalon®-MM DMA Reference Design  
(2) AN708: PCI Express DMA Reference Design Using External Memory

# THANK YOU