Notice of Violation of IEEE Publication Principles

"LDPC Decoder: A Cognitive Radio Perspective for Next Generation (XG) Communication,"
by Abu Baker, S Soumik Ghosh, Ashok Kumar, and Magdy Bayoumi,
in IEEE Circuits and Systems Magazine,
Third Quarter 2007, Vol. 7, Issue 3, pp. 24-37

After careful and considered review of the content and authorship of this paper by a duly constituted expert committee, this paper has been found to be in violation of IEEE's Publication Principles.

This paper contains significant portions of original text from the papers cited below. The original text was copied without attribution (including appropriate references to the original authors and/or paper titles) and without permission. The misconduct was committed specifically by Abu Baker, and his actions were done without the knowledge or approval of his coauthors.

Due to the nature of this violation, reasonable effort should be made to remove all past references to this paper, and future references should be made to the following two articles:

"Energy/power estimation for LDPC decoders in software radio systems,"
By C.-H. Lee, W. Wolf,
in the Proceedings of the IEEE Workshop on Signal Processing Systems Design and Implementation,
November 2005, pp. 48-53.

"Next generation/dynamic spectrum access/cognitive radio wireless networks: A survey,"
by I. F. Akyildiz, W.-Y. Lee, M. C. Vuran, S. Mohanty,
in Computer Networks Journal, Elsevier,
September 2006, Vol. 50, pp. 2127-2159

Abstract

With the rapid growth of multimedia communication systems during the last decade, there has been an increasing demand for improved technology for Error Correcting Code (ECC) to enable the communication systems to have a reliable transmission over noisy channels. Low Density Parity Check (LDPC) codes are the best known ECC codes that can achieve data rates very close to the Shannon limit. In addition, superior error correction performance and parallelizable decoding algorithms have made LDPC codes a powerful competitor to turbo codes for reliable high speed communication applications.

Recently, Cognitive Radio (CR) has been proposed as a promising technology to solve today's spectrum scarcity problem. CR promises to alleviate this spectrum shortage problem by dynamically accessing free spectrum resources. This implies that the radio has to work in multi-band, cope with various wireless channels and support various services such as voice, data and video. The basic requirement for CR is that it has a reconfigurable architecture to support multi-band and frequency adaptive operations.

One of the ambitious design goals of future wireless systems, including 4G, IEEE 802.11n/802.16 standards, is to provide reliably very high data rate transmission in hostile environments: for example, around 100 Mb/s peak rate for downlink and around 30 Mb/s sum rate for uplink transmission with a low frame error rate (FER), typically less than 5×10^{-4}. To ensure reliable and error-free communication, there is a demand to consider implementing LDPC decoders in CR and frequency agile environments. In this article we discuss the design of adaptable as well as efficient LDPC decoders with low bit-error rate (BER) in low signal-to-noise ratio (SNR) channels for CR environments.

Abu Baker, Soumik Ghosh, Ashok Kumar, Magdy Bayoumi

LDPC Decoder: A Cognitive Radio Perspective for NeXt Generation (XG) Communication

Abu Baker is with the University of Louisiana at Lafayette. Soumik Ghosh is with the Research Faculty at the Center for Advanced Computer Studies at the University of Louisana, Lafayette. Ashok Kumar is an Assistant Professor in the Department of Computer Science, University of Louisana, Lafayette. Magdy Bayoumi is the Director of the Center for Advanced Computer Studies and Department Head of the Computer Science Department, University of Louisana, Lafayette.

 1531-636X/07/$25.00©2007 IEEE

I. Introduction

Over the past 15 years, notions about radios have been evolving away from pure hardware-based radios to radios that involve a combination of hardware and software. In the early 1990s, the idea of Software Defined Radios (SDRs) was introduced. These radios typically have a Radio Frequency (RF) front end with a software-controlled tuner. Baseband signals are passed into an analog-to-digital converter. The quantized baseband is then demodulated in a digital signal processor (DSP), or commodity personal computer (PC) and reconfigurable device such as a field-programmable gate array (FPGA). The reconfigurability of the modulation scheme makes it an SDR. Mitola took the SDR concept one step further, coining the term cognitive radio [1]. CRs are essentially SDRs with intelligence, capable of sensing and reacting to their environment. This radio is able to sense the current spectral environment, and have some memory of the past transmitted and received packets along with their power, bandwidth, and modulation, and which can make better decisions about how to optimize best for some overall goals. Possible goals include achieving an optimal network capacity, minimizing interference with other signals, providing robust security or jamming protection, or providing the reliable high speed communication applications which require a high performance error correcting decoder. However, error correcting decoder demands error correcting codes which are used to format the transmitted information so as to increase its immunity to noise. This is accomplished by inserting controlled redundancy into the transmitted information stream, allowing the receiver to detect and possibly correct errors.

LDPC codes are a special case of error correcting codes that have recently been receiving a lot of attention because of their high throughput and very good decoding performance. Traditionally, LDPC decoders were implemented in hardware [2]–[5]. The emergence of software radio concept enables the scientific community to consider implementing decoders in software, and therefore, allows the possibility of dynamically switching between different decoding algorithms to adapt to the environment and channels [6]–[9]. It would be advantageous to be able to select an algorithm which works most efficiently in a given spectrum sensing environment.

This article highlights how different LDPC algorithms measure up for CR environments. The outline of this article is as follows. In Section II, we introduce the cognitive radio. In Section III, we discuss the characteristics of CR for 4G communications. In Section IV, we illustrate the importance of ECC in CR. In Section V, we present the Low Density Parity Check code. In Section VI, we analyze the implementation of LDPC decoder in CR. Finally, Section VII concludes the paper.

II. Cognitive Radio

Cognitive radio technology is the key technology that enables a network to use spectrum in a dynamic manner. The term, cognitive radio, can be formally defined as follows:

"A *Cognitive Radio* is a radio that can change its transmitter parameters based on interaction with the environment in which it operates" [10].

From this definition, two main characteristics of the cognitive radio are defined as follows [11], [12]:

- Cognitive capability: Cognitive capability refers to the ability of the radio technology to capture or sense the information from its radio environment. This capability cannot simply be realized by monitoring the power in some frequency band of interest but more sophisticated techniques are required in order to capture the temporal and spatial variations in the radio environment and to avoid interference with other users. Through this capability, the portions of the spectrum that are unused at a specific time or location can be identified. Consequently, the best spectrum and appropriate operating parameters can be selected.
- Reconfigurability: The cognitive capability provides spectrum awareness whereas reconfigurability enables the radio to be dynamically programmed according to the radio environment. More specifically, cognitive radios can be programmed to transmit and receive over a broad range of frequencies and to use different transmission access technologies supported by their hardware [13].

In other words, a *Cognitive Radio* is a radio that is able to sense the spectral environment over a wide frequency band and exploits this information to opportunistically provide wireless links that best meet the user communication requirements. Figure 1 graphically contrasts traditional radio with software radio and cognitive radio.

III. Characteristics of Cognitive Radio for Next Generation Networks

Today's wireless networks are characterized by a fixed spectrum assignment policy. However, a large portion of the assigned spectrum is used sporadically and geographical variations in the utilization of assigned spectrum ranges from 15% to 85% with a high variance in time. The limited available spectrum and the inefficiency in the spectrum usage necessitate a new communication paradigm to exploit the existing wireless spectrum opportunistically.

Digital Object Identifier 10.1109/MCAS.2007.904180

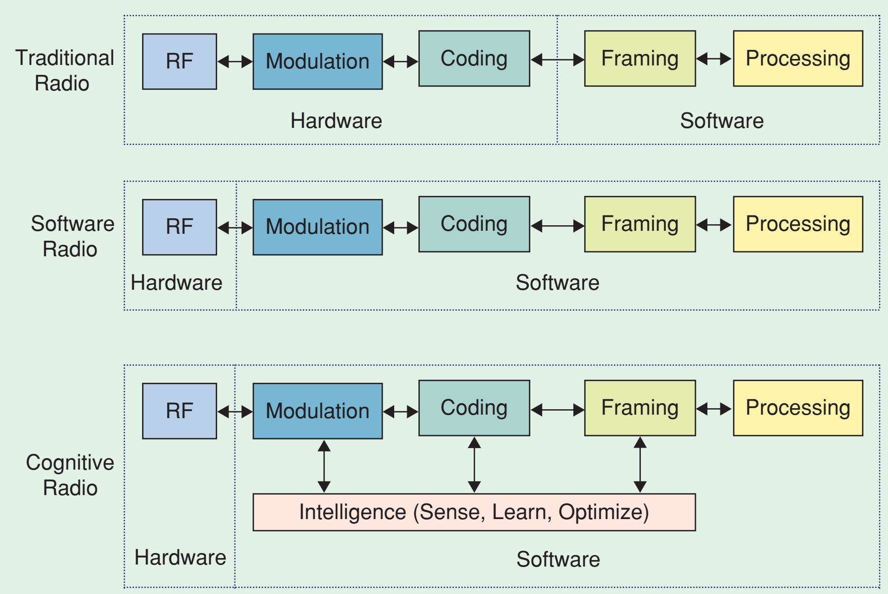


Figure 1. Logical diagram contrasting traditional radio and cognitive radio.

This new networking paradigm is referred to as NeXt Generation (xG) Networks as well as Dynamic Spectrum Access (DSA) and Cognitive Radio Networks [14]–[16]. Cognitive radio techniques provide the capability to use or share the spectrum in an opportunistic manner. DSA techniques allow the cognitive radio to operate in the best available channel. More specifically, the cognitive radio technology will enable the users (a) to determine which portions of the spectrum is available and detect the presence of licensed users when a user operates in a licensed band (spectrum sensing), (b) to select the best available channel (spectrum management), (c) to coordinate access to this channel with other users (spectrum sharing), and (d) to vacate the channel when a licensed user is detected (spectrum mobility).

Once a cognitive radio supports the capability to select the best available channel, the next challenge is to make the network protocols adaptive to the available spectrum. Hence, new functionalities are required in an xG network to support this adaptability. In summary, the main functions for cognitive radios in xG networks can be summarized as follows:

- Spectrum sensing: Detecting unused spectrum and sharing the spectrum without harmful interference with other users.
- Spectrum management: Capturing the best available spectrum to meet user communication requirements.
- Spectrum mobility: Maintaining seamless communication during the transition to better spectrum.
- Spectrum sharing: Providing a fair spectrum scheduling method among coexisting xG users.

These functionalities of xG networks form spectrum-aware communication.

Since the cognitive (unlicensed) users utilize the licensed band, they must detect the presence of licensed (primary) users in a very short time and must vacate the band for the primary users. Therefore, one of the major challenges that confront this technology is: *how do the cognitive (unlicensed) radios sense the presence of the primary (licensed) user?* Since the radio environments is highly variable due to different types of *primary user system, propagation losses*, and *interference*, the implementation of the spectrum sensing functions requires a high degree of flexibility. In other words, different classes of primary users would require different sensitivity and different rates of sensing for detection. For instance, TV broadcast signals are much easier to detect than Global System for Mobile Communications (GSM) signals, since the TV receiver sensitivity is tens of dBs worse than GPS receiver.

The design issues can be broadly categorized into the following two problems:

- How to define RF and analog architecture with right trade-offs among linearity, sampling rate, accuracy, and power so that digital signal processing techniques can be utilized for spectrum sensing, cognition, and adaptation.
- How to detect the presence of primary user through continuous *spectrum sensing* with the knowledge of the signal characteristics. However, this spectrum sensing could be *direct* or *cooperative sensing*.

Due to multipath fading and shadowing, the performance of direct sensing is limited by received signal strength. On the other hand, cooperative sensing scenario [17] may alleviate the problem of detecting the primary user by reducing the probability of interference to a primary user. Figure 2 describes the cooperative sensing scenario.

It is mentioned that although sophisticated cooperative schemes have the advantage of low interference, it is noted that various users may have different sensitivities and sensing times which is troublesome. Cooperation also introduces the need for a control channel [18]. In order to improve radio front-end sensitivity and to detect primary user, there is a need for signal processing. So, in this section we discuss detection features, identification of these features and implementation at abstract level.

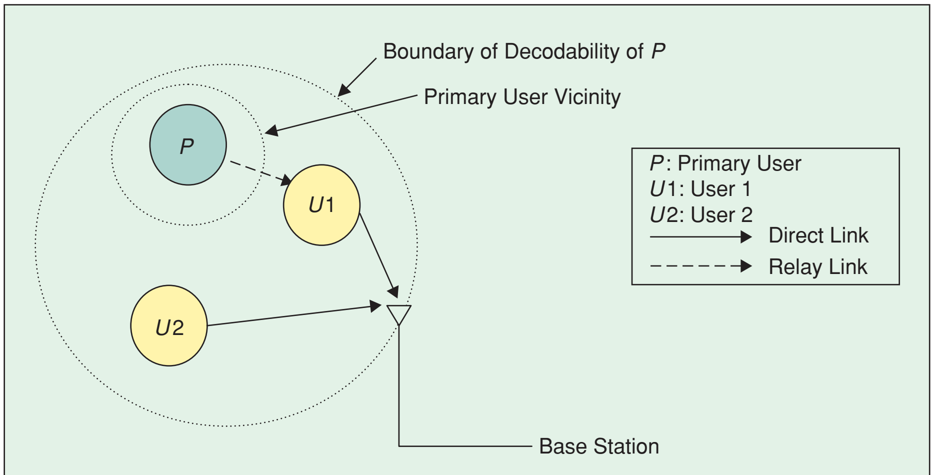


Figure 2. Cooperation in cognitive radio.

What features have to be considered as detection parameters in order to be used in Cognitive Radio for intelligence? The new radio functionality will involve the design of various analog, digital and network processing techniques in order to meet challenging radio sensitivity requirements and wideband frequency agility. The most sought after detection features are: *number of signals, their modulation types, energy detection, SNR, symbol rate, and presence of interference.*

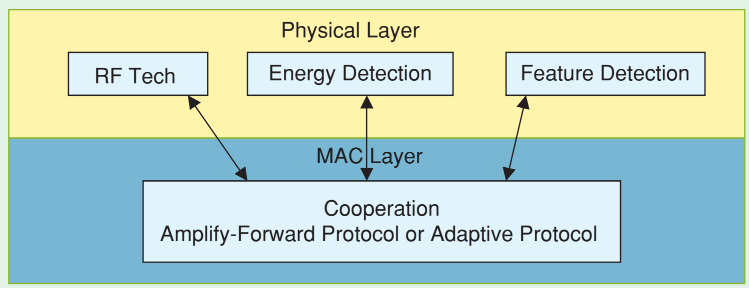


Figure 3. Cross layer functionalities for spectrum sensing.

There are three techniques for spectrum sensing:

I. *Match Filter:* It is an optimal and simple way to detect the signal, since it maximizes the received signal-to-noise ratio. It requires the coherency with the primary signal by performing timing, carrier synchronization, and channel equalization which demand for demodulation. *Advantages:* Due to coherency it requires less time to achieve high processing gain and only O (1/SNR) samples are needed to meet a given probability of detection constraint. *Disadvantages:* A significant drawback of a matched filter is that a cognitive radio would need a dedicated receiver for every primary user.

II. *Energy Detection:* Filter detection does not require coherent detection, hence it is a sub-optimal techniques. But it has some drawbacks. *Advantages:* It requires only O (1/SNR^2) samples as well as FFT processor. *Disadvantages:* Its implementation is complex. It demands for threshold and it is not clear how to set the threshold with respect to channel notches. A significant drawback of this technique is that energy detection does not differentiate between modulated signals, noise, and interference. Moreover, energy detection does not work for spread spectrum signals: direct sequence and frequency hopping. More sophisticated algorithms are based on spread spectrum signals.

III. *Cyclostationary Feature Detection:* Since modulated signals are coupled with sine wave carriers, pulse trains, repeating spreading, hopping, a receiver can exploit it for: parameter estimation such as carrier phase, pulse timing, or direction of arrival. The basic formula behind this technique is *Spectral Correlation Function* (SCF) which can be used for detection of a random signal with detection features. This is because different types of modulated signals (such as BPSK, QPSK, SQPSK or QAM) have distinct spectral correlation functions. Furthermore, stationary noise and interference exhibit no spectral correlation.

Spectrum Sensing is best addressed as a cross-layer design. Cognitive radio sensitivity can be improved by enhancing radio RF front-end sensitivity, exploiting digital signal processing gain for specific primary user signal, and network cooperation where users share their spectrum sensing measurements [19]. Figure 3 illustrates physical and Media Access Control (MAC) functions that are linked to spectrum sensing.

Until now we have discussed the novel characteristic of cognitive radio and implementation aspects of spectrum sensing which enables real-time measurements of spectrum information from radio environment. In the following section we will discuss how channel coding can play an important role in cognitive radio networks and how this coding can be suited into these agile circumstances.

IV. How ECC Can Play an Important Role in Cognitive Radio Networks

There is a vision that generations beyond 3G will be able to achieve seamless, always-best-connected wireless services. This means that users of mobile devices will be able to connect to the "best" wireless infrastructure available (cellular, WiFi, WiMAX) anytime and anywhere, where "best" could be perceived as best quality of service, best price, best security, etc. In other words, xG is the capability of adjusting operating parameters for the transmission on the fly without any modifications on the hardware components. This capability enables the cognitive radio to adapt easily to the dynamic radio environment. There are several reconfigurable parameters that are being incorporated into the cognitive radio as explained below [20]:

- Operating frequency: A cognitive radio is capable of changing the operating frequency. Based on the information about the radio environment, the most suitable operating frequency can be determined and the communication can be dynamically performed on this appropriate operating frequency.
- Modulation: A cognitive radio can reconfigure the modulation scheme adaptive to the user requirements and channel conditions. For example, in the case of delay sensitive applications, the data rate is more important than the error rate. Thus, the modulation scheme that enables the higher spectral efficiency should be selected. Conversely, the loss-sensitive applications focus on the error rate, which necessitates modulation schemes with low bit error rate.
- Transmission power: Transmission power can be reconfigured within the power constraints. Power control enables dynamic transmission power configuration within the permissible power limit. If higher power operation is not necessary, the cognitive radio reduces the transmitter power to a lower level to allow more users to share the spectrum and to decrease the interference.
- Communication technology: A cognitive radio can also be used to provide interoperability among different communication systems.

Recently many standards proposals, namely TGnSync [21], [22], or WWise [23] for IEEE 802.11n, together with IEEE 802.16e [24], have considered LDPC coding schemes as a key component of their system features. The adoption by such standard activities proves the increasing maturity of the LDPC related technology, especially the affordable joint complexity from encoder and decoder implementation. From sub-optimal lower-complexity decoding algorithms [25] to complete flexible architecture design [26], [27], some pragmatic and realistic implementation solutions allow LDPC codes to be more and more attractive as enhancement of current (B3G) or next generation wireless systems (4G) [28]. One of the most interesting potential applications of an xG network is in a military radio environment [29]. xG networks can enable the military radios to choose arbitrary, intermediate frequency (IF) bandwidth, modulation schemes, and coding schemes, adapting to the variable radio environment of the battlefield. In this article more specifically we focus on the coding scheme particularly LDPC. Our main objective is how to make channel coding more adaptive and reconfigurable to the variable radio. Therefore, in the following section we investigate design complexity, performance analysis and power consumption of channel coding which are important to achieve less BER as well as less SNR, meaning less transmitter and receiver power in order to provide a seamless transmission.

V. Low Density Parity Check Code

Error correcting code (ECC) enables communication systems to have reliable transmission over noisy channels. Figure 4 depicts a classical block diagram of a digital communication system. Several types of codes exist, each of which is suitable for some special applications. The encoding/decoding algorithm for each code should be modified to fit into the space of practical hardware implementation. Moreover, each ECC has several algorithms and there exists a large design space with trade-offs among performance, complexity and power consumption. In this article we address trade-offs for a particular type of error correcting codes, namely, *Low Density Parity Check Code* (LDPC). These codes have proved to have very good performance over noisy channels [30].

LDPC codes were invented by R. G. Gallager in 1962 [31]. He devised an iterative decoding algorithm which he applied to a new class of codes. He named these codes LDPC codes since the parity-check matrices had to be sparse to perform well. Yet, LDPC codes were ignored for a long time mainly due to the need for higher complexity computations, if very long codes are considered.

In 1993, C. Berrou invented the turbo codes and their associated iterative decoding algorithm [32]. The remarkable performance observed with the turbo codes raised many questions and generated much interest in iterative techniques. In 1995, D. J. C. MacKay and R. M. Neal rediscovered the LDPC codes, and set up a link between their iterative algorithms to Pearl's belief algorithm using Bayesian networks. At the same time, M. Sipser and D. A. Spielman used the first decoding algorithm of R. G. Gallager to decode expander codes [31].

Graphs are becoming a standard representation of error correcting codes: F. R. Kschischang denotes by factor graphs a wide class of graph associated with the sum-product algorithm, which aim at describing many different algorithms by the same formalism. This work has its origin in the work of Tanner, and N. Wiberg, Loeliger [30], [33].

LDPC codes are at the confluence of two major changes in the channel coding community: the graph-based code-description, and the iterative decoding techniques. An LDPC code, which is a linear block code defined by a very sparse parity-check matrix, can be represented effectively by a bi-partite graph called a "*Tanner*" graph [34], [35]. A bi-partite graph is a graph (nodes or vertices are connected by undirected edges) whose nodes may be separated into two classes, and where edges connect two nodes not residing in the same class.

The two classes of nodes in a Tanner graph are "*Variable Nodes*" and "*Check Nodes*". The Tanner graph of a code is drawn according to the following rule: Check Node $f_j, j = 1, \ldots\ldots n-k$ is connected to Variable Node $x_i, i = 1, \ldots\ldots n$ whenever element h_{ji} in H (parity-check matrix) is a "1". Figure 5 shows a Tanner graph made for a simple parity check matrix H. In this graph each Variable Node is connected to *two* Check Nodes (Variable degree = 2) and each check node has a degree of *four.*

Figure 6 illustrates the basic scheme for channel encoding/decoding where the source block delivers information by the means of sequences which are row vectors x of length k. The encoder block delivers the codeword y of length n, which is the coded version of x. The code rate is defined by the ratio R = k/n. The codeword y is sent over the channel and the vector $\hat{y}$ is the received word: a distorted version of y.

LDPC codes have several advantages over turbo codes: First, Sum-Product decoding algorithm [36], [37] for these codes has inherent parallelism which can be exploited to achieve a greater speed of decoding. Second, unlike turbo codes, decoding error is a detectable event which results in a more reliable system. Third, very low complexity decoders such as Modified Min-Sum algorithm [33] that closely approximate Sum-Product in performance can be designed for these codes.

There are different errors correcting codes: Viterbi, Turbo, and LDPC etc. The block and convolutional/viterbi codes are structured codes. Their performance generally improves with the increase in the code length. However, the decoding complexity increases exponentially with the increase in the code length. Thus, the performance of these codes is limited by the computational resources available. It was commonly believed that approaching the Shannon limit which requires a large code length was practically impossible due to infeasible amount of computations. The success of turbo codes is attributed to its ability to integrate the structured code design in a pseudo-random

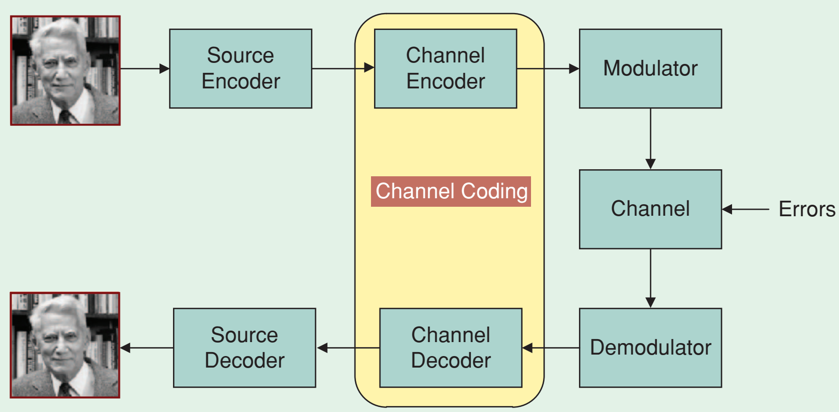


Figure 4. A classical block diagram of a digital communication system.

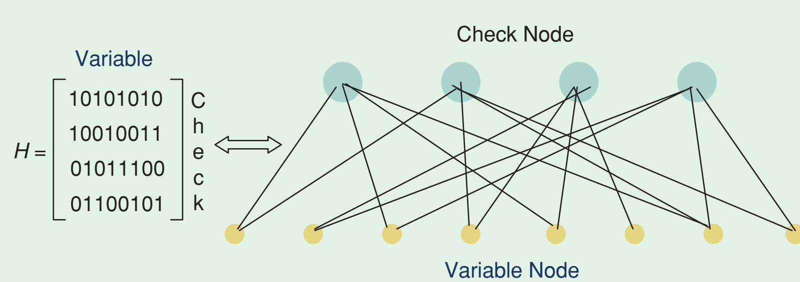


Figure 5. Tanner graph of a parity check matrix.

Table 1.
Performance comparison of different type of the channel codes [31].

Year	Type of Channel Codes (Code Rate 1/2)	SNR Required for BER $< 10^{-5}$
1948	SHANNON	0dB
1967	(255,123) BCH*	5.4dB
1977	Convolutional Code	4.5dB
1993	**Iterative** Turbo Code 1	0.7dB or less
2001	**Iterative** LDPC Code	0.0245dB

*BCH (Bose, Ray-Chaudhuri, Hocquenghem)

Table 2.
Complexity comparison among Viterbi, Turbo and LDPC encoders/decoders [31, 32].

Code Type	Encoder	Decoder
Convolutional/Viterbi	$O(N_d)$	$O(N2^d)$
Turbo	$O((N(d_1+1+d_2))$	$O(JN(1+2^{d_1}+2^{d_2}))$
LDPC	$O(NW_r^2)$	$O(JN(W_r+W_c))$

fashion which nearly achieves the Shannon Capacity limit while keeping low decoding complexity. Prompted by its exceptional performance, the turbo code has been used to solve numerous communications problems. The performance of various error correcting codes are compared by referring to their gap to the Shannon limit.

Table 1 shows a comparison between the best known error correcting codes. This table shows that for very large block lengths, LDPC is the best known code in terms of performance. Complexity in iterative decoding has three parts. The first is the complexity of the computations at each node. The second is the complexity of the interconnection. And the third is the number of times that local computations need to be repeated, usually referred to as the number of iterations. Table 2 shows a comparison among the combined complexities of the encoder and the decoders for three different types of coding. In this table N is the code length, d is the constraint length, J is the maximum number of the decoding iterations, Wr is the row degree and Wc is the column degree of the nodes in the parity check matrix of a LDPC decoder. Comparisons show that LDPC decoding is linear with the block length, whereas in turbo codes, it has exponential relation with the constraint length.

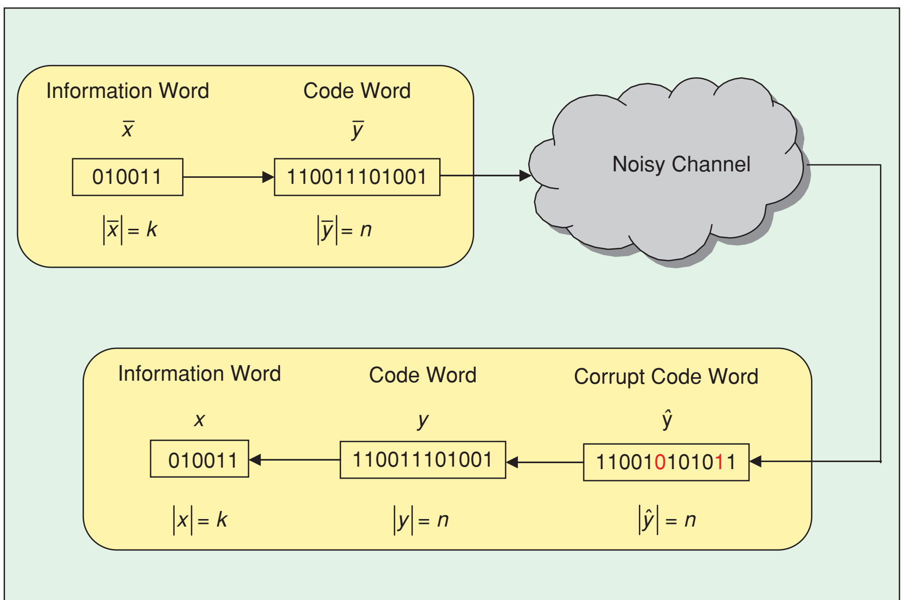


Figure 6. The basic scheme for channel encoding/decoding.

VI. LDPC Decoder in Cognitive Radio Networks Platform

The cognitive capability of a cognitive radio enables real time interaction with its environment to determine appropriate communication parameters

Table 3.
Operations for one variable node [42]–[46].

Logic Functions	Populated H- Matrix Row (W_r)
Tanh(x/2)	SP (W_r)
multiply	SP ($W_r - 1$); MMS(W_r)
divide	SP(W_r)
2atanh	SP(W_r)
abs	Log-SP(W_r); MS(W_r)
sign	Log-SP(W_r); MS(W_r)
add	Log-SP($W_r - 1$); WBF/MWBF($2W_r - 1$); RRRWBF($W_r - 1 +^{i} (W_r - 1)$)
sub	Log-SP(W_r)
xor	Log-SP($2W_r - 1$); MS($2W_r - 1$)
Log(tanh(x/2))	Log-SP(W_r); $^{i}(W_r - 1)$
min	MS ($W_r(W_r - 2)$); WBF/MWBF($^{i}(W_r - 1)$)
mux	WBF/MWBF (W_r); RRRWBF(W_r)

^{i}( ) denotes that function is only used at initialization step.

and adapts to the dynamic radio environment. There are several reconfigurable parameters that can be incorporated into the cognitive radio. They are operating frequency, modulation, transmission power, and communication technology. BER and Signal-to-Noise Ratio (SNR) are the most important parameters for determining these characteristics if the channel type is known. If the communication quality is critical, a solution is to increase the transmit power. For example, let the required BER be 10^{-4}. We have to be aware which algorithms will be energy efficient as opposed to the ones that will be performance efficient. Therefore, we have to investigate the following issues that have to be addressed if LDPC decoders have to be implemented in CR environments. It is worth mentioning that BER, SNR, and the channel type can be known from the dynamic spectrum sensing.

- *Algorithmic Complexity:* It has been observed that the usage of logic functions vary for different decoding algorithms. For instance, multiplication and division operations are usually more computationally intensive than other operations, so it is expected that we have to be aware of algorithmic complexity.
- *Performance Analysis:* Some algorithms give best error-correction as expected since they are optimal decoding algorithms for LDPC codes. While BER is vulnerable to noise, performance is an important issue for these environments.
- *Power Analysis:* While energy consumption is related to battery lifetime, power consumption is responsible for heating up the circuits. So, we have to investigate power consumption of different algorithms if chip cooling is an issue.

A. Algorithmic Complexity Analysis of LDPC Decoding Algorithm

Iterative decoding of LDPC codes falls into two main categories: belief propagation (BP) based and bit-flipping (BF)based. The most well-known BP-based algorithms are *sum-product* (SP) [38] and its logarithm domain variant-*log sum product* (log-SP) [39], [40]. Most of the computation in these algorithms is done in the calculation of phi-function $\psi = \ln\left(\tanh\left|\frac{x}{2}\right|\right) = \ln\frac{1+e^{-|x|}}{1-e^{-|x|}}$. To alleviate this, a much simpler algorithm called *min-sum* (MS) [41] and its modified version- *modified min-sum* (MMS) [42] were proposed to remove totally this function. Bit-flipping-based algorithms, on the other hand, are based on flipping the least unreliable bit after each iteration. *Weighted bit-flipping* (WBF) [43] is a modified version of the original bit-flipping algorithm proposed by Gallager. *Modified weighted bit-flipping* (MWBF) [44] and the revised version of *reliability ratio based weighted bit-flipping* (RRRWBF) [45], [46] algorithms try to narrow the gap between bit-flipping and sum-product algorithms by incorporating more information into bit-flipping decision step.

The connection between variable and check nodes is fixed for a particular LDPC code. Therefore, we can divide the problem of LDPC decoder implementation into two sub problems: *node processing* and *node connection*. What mainly makes decoding complexity of those algorithms different is how messages are processed at nodes. The power dissipation overhead for node connections is nearly the same for all algorithms as the connectivity is determined by a fixed H-Matrix for any given algorithm. So, we concentrate on comparing power dissipation in logic functions needed for check and variable nodes in order to evaluate the difference in power consumption, especially when the

Table 4.
Operations for one check node [42]–[46].

Logic Functions	Populated H-Matrix Columns (W_c)
add	SP (W_c); Log-SP (W_c); MS/MMS (W_c); WBF/MWBF ($W_c - 1$); RRRWBF ($W_c - 1$)
sub	SP (W_c); Log-SP (W_c); MS/MMS (W_c); MWBF (1)
sign	Log-SP (W_c)
log(tanh(x/2))	Log-SP (W_c)
change sign	WBF/MWBF (W_c)
abs	WBF/MWBF(${}^{i}1$); RRRWBF(${}^{i}1$)
scale	MWBF (1)
divide	RRRWBF (1)

Table 5.
Processor parameters.

Clock Rate	Vector Thread Units	# of Clusters	# of Registers (per cluster)	Datapath
400 MHz	4	16	32 (Virtual) 16 (Physical)	16

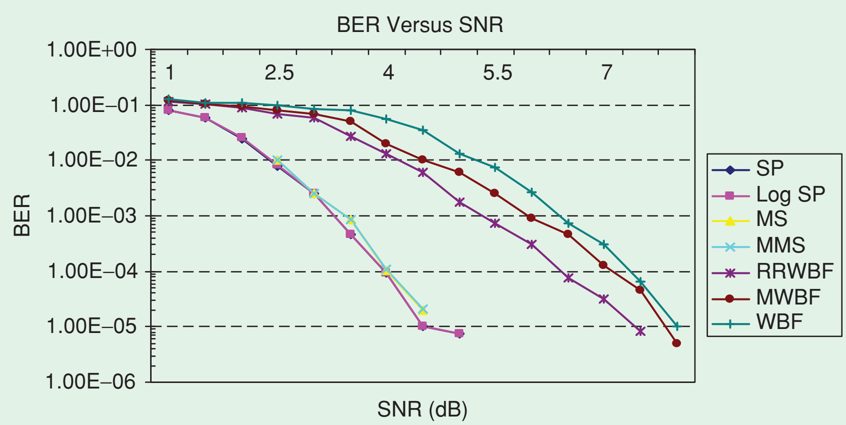


Figure 7. Bit-error-rate (BER) for different decoding algorithms for a (603, 301) code under Raleigh channel.

decoder is implemented in software. In this article, we have focused on the comparison of irregular LDPC codes. Table 3 and Table 4 show the usage of logic functions at variable and check nodes respectively for different decoding algorithms. Multiplication and division operations usually consume more power than the other operations, so it is expected that SP algorithm will consume more power. Since most bit-flipping-based algorithms have simple operations, the power consumption should be small compared to SP, log-SP, MS, and MMS algorithms.

B. Performance Analysis of LDPC Decoding Algorithm

In order to compare the performance of different decoding algorithms, we have chosen the (603, 301) irregular LDPC code recently proposed by Dinoi [47], as it has a very good correction properties and in addition the IEEE 802.16e committee has selected it for the forthcoming wireless MAN international standard targeting BER of 10^{-5}. The stopping criterion we have used is to stop iteration if $\hat{y}H^T = 0$ or 200 iterations are reached. Raleigh channel is assumed. The performance results are shown in Figure 7 in term of bit-error-rate (BER). It has been observed that SP and log-SP algorithms give best error-correction as expected since they are optimal decoding algorithms for LDPC codes.

The performance of MS is close to the SP algorithm, and the MMS algorithm performs slightly better than the MS. RRRWBF algorithm performs best among bit-flipping based algorithms, but it is still worse than BP-based algorithms.

C. Power Analysis of LDPC Decoding Algorithm

LDPC codes have been demonstrated to achieve information rates very close to the Shannon limit when iteratively decoded and, in general, LDPC decoders are known to require an order of magnitude less arithmetic computations than turbo decoders that provide similar bit-error performance. Therefore, architectures for low-density parity check decoders have been discussed with methods to reduce their complexity. There have been several proposed architectures for LDPC Decoder. A fully parallel architecture provides potentially the fastest decoding throughput. However, from an implementation point of view, it is infeasible for large block length codes. An architectural solution can be found in *vector-thread architectures* [48] which could provide a solution for a fully parallelized LDPC implementation. The vector-thread (VT) architectural paradigm describes a class of architectures that unify the vector and multi-threaded execution models. In other words, VT architectures compactly encode large amounts of structured parallelism in a form which allows simple micro-architectures attain high-performance at low power by avoiding complex control and datapath structures, and by reducing activity on large wires. The VT paradigm aims to provide high performance at low power for a wide range of embedded applications while using only a small area. Figure 8 shows briefly the VT architecture. We feed our LDPC decoder on the VT architecture with some parameters shown in Table 5 which includes a MIPS-RISC control processor, 32 Kbytes of cache, and a four-lane vector-thread unit that can execute 16 operations per cycle and support up to 128 simultaneously active virtual processor threads.

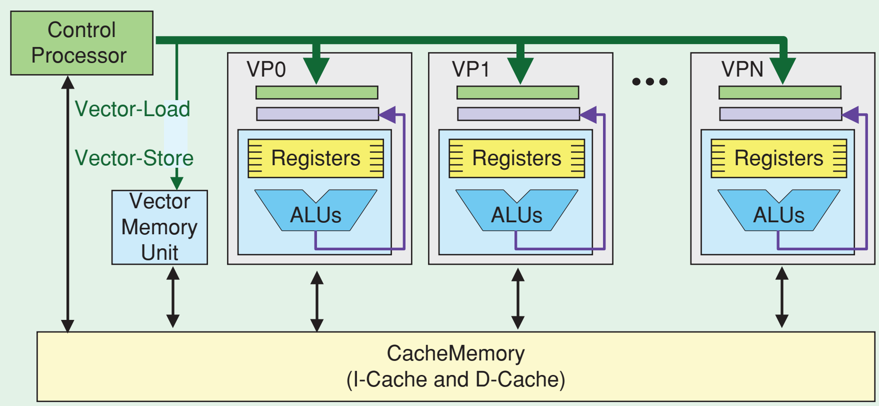


Figure 8. Vector-Thread architecture [48].

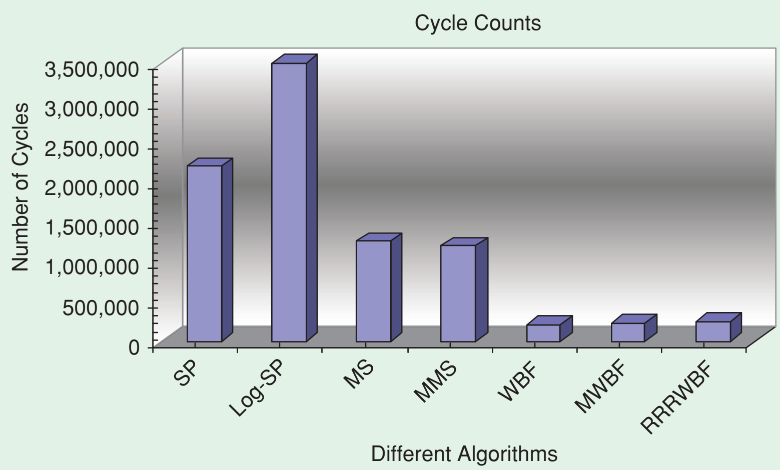


Figure 9. Total number of cycles required to finish each algorithm.

Figure 9 shows total VT cycles and Figure 10 shows total energy consumption for different decoding algorithms. An interesting result is: although log-SP algorithm is more popular than SP in hardware implementation [40], it is inefficient for decoders implemented in software in terms of energy consumption. In hardware implementation, $log(tanh(x/2))$ can be easily implemented using a lookup table (since messages are quantized), so it would be advantageous to have extra $log(tanh(x/2))$ functions at variable nodes and extra log(x) functions at check nodes to trade for multiplications and divisions. The software implementation of log and *tanh* functions, however, takes much longer time than multiplication operation, so log-SP behaves worse. MS and MMS algorithms remove the need of $tanh(x/2)$ and some adders or multipliers, which results in a huge drop in VT execution cycle count, and therefore, total energy consumption. The PDP consumption of bit-flipping algorithms is only about 1/6 of SP and 1/2 of MS algorithms. Results from Figure 9 also suggest that if delay constraint is a critical problem, bit-flipping-based algorithms are better candidates than BP-based algorithms.

Simulation result shows the following:

- RRRWBF has the highest power consumption which is undesirable if chip cooling is an issue.
- The power consumption of bit-flipping based algorithm is larger than that of MS and SP algorithms.
- Bit-flipping algorithms dissipate more power than other algorithms in instruction window, instruction cache, level-1 data cache, ALU, result bus, and clock units. As a result, this concludes that pipleline stall resulted from cache miss penalty happened less.

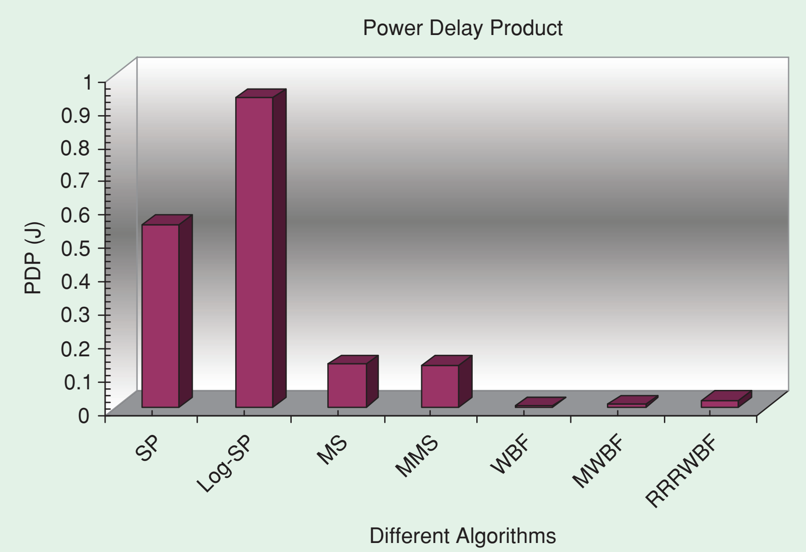


Figure 10. Total energy consumption.

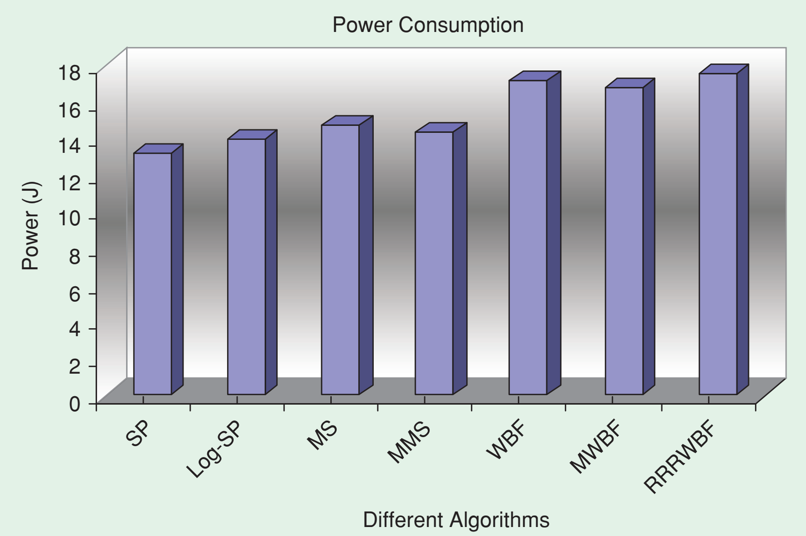


Figure 11. Power consumption.

- The power consumption of WBF, MWBF, and RRRWBF is much higher than that of SP and log-SP algorithms.
- The result shows the WBF algorithm is the most energy-saving algorithm for LDPC decoders, and MWBF and RRRWBF algorithms consume slightly more energy. However, RRRWBF's error correcting power is much better than WBF; it is thus a better energy consumption and performance trade-off than WBF.

Different decoding algorithms require different number of iterations to successfully decode a codeword. Even for a particular decoding algorithm, number of iterations varies depending on the received bits. Therefore, the main idea is to gather the statistics information by simulating the average number of iterations needed to decode a LDPC code under different SNR and different algorithms. The process is summarized below:

The (603, 301) irregular LDPC code was used to simulate the energy consumption of different decoding algorithms using a fixed number of iterations shown in Figure 11. To further investigate this, the power dissipated in each VT hardware unit was computed as shown in Figure 12. BER versus SNR plot tells us how much power is needed to achieve specific BER. We can view this as how much needed power is transmitted in a *transmitter* if the channel type is known. Having this information, it is then possible to have an energy/power management scheme shown in Figure 13 again. Suppose the following scenario that implements the algorithm diversity: To save power and extend battery life, the decoding algorithm is switched from SP to the one with less energy consumption, for example, RRRWBF. A solution is to increase the transmit power. For example, let the required BER be 10^{-4}. Switching from SP to RRRWBF saves energy consumption at the transmitter, but degrades its error-correcting performance. To maintain the same quality, the transmit power must be 2.2dB more.

VII. Conclusions

In the context of cognitive radios, the error-correcting codes would have the ability to operate close to the Shannon limit under constraints in delay and/or energy/power consumption to be efficient. For instance, if the energy source on a mobile device is getting low, it would be undesirable to use power consuming decoding algorithms even if they have good error-correcting performance. Under these circumstances, the decoder can trade performance for power consumption. If using a powerful but complex decoding algorithm that cannot meet the delay requirements, switching to a simpler algorithm with less error-correcting capability could be desired. We have compared seven LDPC decoding algorithms in terms of error-correcting performance, complexity, cycle count, and energy/power consumption for decoders implemented in software. The results reveal that bit-flipping-based algorithms are best for decoders with strict delay-constraints. While RRRWBF algorithm shows the best trade-off between energy consumption and error-correcting performance, its power consumption is the highest. The key enabling technology of xG networks is the Cognitive Radio. Implementation of error-correcting codes, particularly LDPC, in software,supported by custom hardware, will enable an xG network to use different decoding algorithms in a dynamic manner in order to adapt to the environment and channels in which it operates.

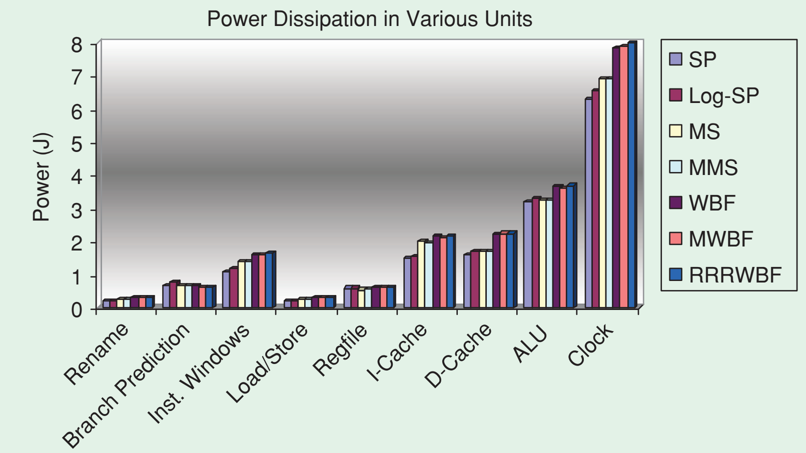


Figure 12. Power dissipation in various function units.

Acknowledgement

The authors acknowledge the support of the Governor's Information Technology Initiative, the U.S Department of Energy award and Louisiana Board of Regents contract DOE/LEQSF (2004-07)-ULL, and the NSF, INF 6-001-006, INF 9-001-001, OISE-0512403.

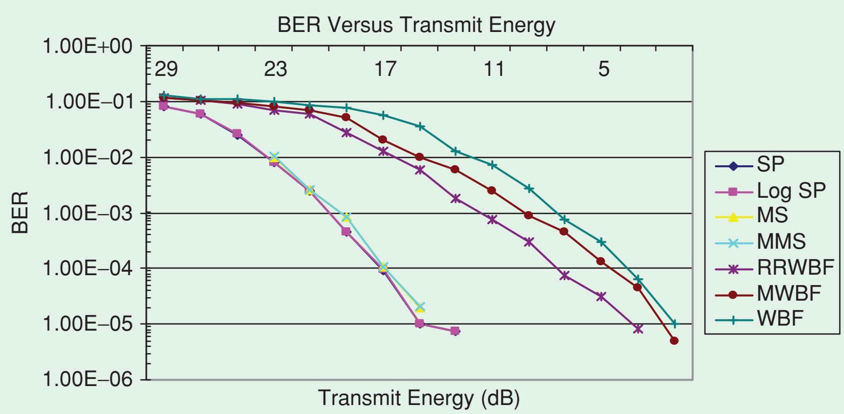


Figure 13. BER versus transmit energy.

References

[1] J. Mitola III, Ph.D. dissertation, "Cognitive Radio: an integrated agent architecture for Software Defined Radio," Royal Institute of Technology (KTH) Stockholm, Sweden, ISSN 1403–5286, May 8 2000.

[2] C. Cordeiro, K. Challapali, D. Birru, S. Shankar, "IEEE 802.22: the first worldwide wireless standard based on cognitive radios," in *Proc. IEEE DySPAN 2005*, pp. 328–337, Nov. 2005.

[3] F. Digham, M. Alouini, M. Simon, "On the energy detection of unknown signals over fading channels," in *Proc. IEEE ICC 2005*, vol. 5, pp. 3575–3579, May, 2003.

[4] E. Esteves, "*The high data rate evolution of the cdma2000 cellular systemMobility and Teletraffic for Wireless Communication*s," vol. 5, Kluwer Academic Publishers, pp. 61–72, 2000.

[5] R. Etkin, A. Parekh, D. Tse, "Spectrum sharing for unlicensed bands," in *Proc. IEEE DySPAN 2005*, pp. 251–258, Nov. 2005.

[6] G. Ganesan, Y.G. Li, "Cooperative spectrum sensing in cognitive radio networks," in *Proc. IEEE DySPAN 2005*, pp. 137–143, Nov. 2005.

[7] G. Ganesan, Y.G. Li, "Agility improvement through cooperative diversity in cognitive radio networks," in *Proc. GLOBECOM,* pp. 2505–2509, Nov. 2005.

[8] A. Ghasemi, E.S. Sousa, "Collaborative spectrum sensing for opportunistic access in fading environment," in *Proc. IEEE DySPAN 2005*, pp. 131–136, Nov. 2005.

[9] D. Grandblaise, D. Bourse, K. Moessner, P. Leaves, "Dynamic spectrum allocation (DSA) and reconfigurability," in *Proc. Software-Defined Radio (SDR) Forum*, Nov. 2002.

[10] FCC, ET Docket No 03-222 Notice of proposed rule making and order, Dec. 2003.

[11] R.W. Brodersen, A. Wolisz, D. Cabric, S.M. Mishra, D. Willkomm, "*Corvus: a cognitive radio approach for usage of virtual unlicensed spectrum*," Berkeley Wireless Research Center (BWRC) White paper, 2004.

[12] T.X. Brown, "An analysis of unlicensed device operation in licensed broadcast service bands," in *Proc. IEEE DySPAN 2005*, pp. 11–29, Nov. 2005.

[13] M.M. Buddhikot, P. Kolody, S. Miller, K. Ryan, J. Evans, "DIMSUMNet: new directions in wireless networking using coordinated dynamic spectrum access," in *Proc. IEEE WoWMoM 2005*, pp. 78–85, Jun. 2005.

[14] D. Cabric, R.W. Brodersen, “Physical layer design issues unique to cognitive radio systems,” in *Proc. IEEE Personal Indoor and Mobile Radio Communications (PIMRC) 2005*, Sep. 2005.

[15] J. Mitola, “Software radios-survey, critical evaluation and future directions,” *National Telesystems Conference, 1992, NTC-92*, pp. 13/15–13/23, May, 1992.

[16] L. Cao, H. Zheng, “Distributed spectrum allocation via local bargaining,” in *Proc. IEEE Sensor and Ad Hoc Communications and Networks (SECON) 2005*, pp. 475–486, Sep. 2005.

[17] L. Berlemann, S. Mangold, B.H. Walke, “Policy-based reasoning for spectrum sharing in cognitive radio networks,” in *Proc. IEEE DySPAN 2005*, pp. 1–10, Nov. 2005.

[18] M.M. Buddhikot, K. Ryan, “Spectrum management in coordinated dynamic spectrum access based cellular networks,” in *Proc. IEEE DySPAN 2005*, pp. 299–307, Nov. 2005.

[19] D. Cabric, S.M. Mishra, R.W. Brodersen, “Implementation issues in spectrum sensing for cognitive radios, in *Proc. 38th Asilomar Conference on Signals, Systems and Computers 2004*, pp. 772–776, Nov. 2004.

[20] I.F. Akyildiz, Y. Li, “OCRA: OFDM-based cognitive radio networks,” Broadband and Wireless Networking Laboratory Technical Report, Mar. 2006.

[21] IEEE 802.11n, “Structured LDPC Codes as an Advanced Coding Scheme for 802.11n,” IEEE Doc. 802.11-04/884r0, Aug. 2004.

[22] TGn Sync proposal. Available: http://www.tgnsync.org/home

[23] WWISE proposal. Available: http://www.wwise.org/

[24] IEEE 802.16e, “LDPC coding for OFDMA PHY,” IEEE Doc. C802-16e-05/066r3, Jan. 2005.

[25] J. Chen and M. Fossorier, “Near Optimum Universal Belief Propagation Based Decoding of Low-Density Parity Check Codes,” *IEEE Transactions on Communications*, vol. 50, no. 3, pp. 406–414, Mar. 2002.

[26] T. Zhang, “Efficient VLSI Architectures for Error-Correcting Coding”, University of Minnesota, Ph.D Thesis, Jul. 2002.

[27] H. Zhong, and T. Zhang, “Block-LDPC: A Practical LDPC Coding System Design Approach,” *IEEE Trans. on Circuits and Systems -I*, vol. 52, no. 4, Apr. 2005.

[28] WINNER FP6. Available: https://www.ist-winner.org/

[29] R. Murty, “Software-defined reconfigurability radios: smart, agile, cognitive, and interoperable,” *Technology Intel Magazine*, Jul. 2003.

[30] R.M. Tanner, “A recursive approach to low complexity codes,” *IEEE Transactions on Information Theory*, vol. 27, no. 5, pp. 533–547, Sep. 1981.

[31] R. Gallager, “Low-density parity-check codes,” *IRE Transactions on Information Theory*, pp. 21–28, Jan. 1962.

[32] Y. Kou, S. Lin, and M. Fossorier, “Low-density parity-check codes based on finite geometries: a rediscovery and new results,” *IEEE Trans. on Information Theory*, pp. 2711–2736, Nov. 2001.

[33] N. Wiberg, *Codes and decoding on general graphs*. LinKoping, Sweden, Ph.D. Thesis, Linkoping University, 1996.

[34] A. Viterbi, “Error bounds for convolutional codes and an asymptotically optimum decoding algorithm,” *IEEE Trans. Information Theory*, vol. 13, pp. 260–269, Apr. 1967.

[35] B.J. Frey, F.R. Kschischang and H.A. Loeliger, “Factor graphs and the sum-product algorithm,” *IEEE Transactions on Information Theory*, vol. 47, no. 2, pp. 498–419, Feb. 2001.

[36] D.J.C. MacKay, “Good error-correcting codes based on very sparse matrices,” *IEEE Trans. Inf. Theory*, vol. 45, no. 2, pp. 399–431, 1999.

[37] F. Guilloud, E. Boutillon, and J. Danger, “[ab24]λ-min decoding algorithm of regular and irregular LDPC codes,” *Proc. 3rd Int. Symp. Turbo Codes & Related Topics*, Brest, France, Sep. 2003.

[38] D.J.C. MacKay and R.M. Neal, “Near Shannon limit performance of low density parity check codes,” *Electron. Letter*, vol. 33, no. 6, pp. 457–458, 1997.

[39] M. Chiani, A. Conti, and A. Ventura, “Evaluation of low-density parity check codes over block fading channels,” *2000 IEEE International Conference on Communications,* pp. 1183–1187, 2000.

[40] T. Zhang and K. Parhi, “Joint (3,k)-regular LDPC code and decoder/encoder design,” *IEEE Trans. on Signal Processing*, vol. 52, no. 4, pp. 1065–1079, Apr. 2004.

[41] L. Bahl, J. Cocke, F. Jelinek, and J. Raviv, “Optimal decoding of linear codes for minimizing symbol error rate,” *IEEE Trans. Inf. Theory*, vol. 20, no. 3, pp. 284–287, 1974.

[42] J. Heo, “Analysis of scaling soft information on low density parity check codes,” *Electronics Letters*, no. 2, pp. 219–221, Jan. 2003.

[43] M. Luby, M. Mitzenmacher, M. Shokrollahi, and D. Spielman, “Improved low-density parity-check codes using irregular graphs and belief propagation,” in *Proc. IEEE International Symposium on Information Theory*, Cambridge, Mass, USA, p. 117, Aug. 1998.

[44] J. Zhang and M. Fossorier, “A modified weighted bit-flipping decoding of low-density parity-check codes,” *IEEE Communications Letter*, no. 3, pp. 165–167, Mar. 2004.

[45] F. Guo and L. Hanzo, “Reliability ratio based weighted bit-flipping decoding for low-density parity-check codes,” *Electronics Letters*, no. 21, pp. 1356–1358, Oct. 2004.

[46] O.B. Akan, I.F. Akyildiz, “ATL: an adaptive transport layer for next generation wireless internet,” *IEEE Journal on Selected Areas in Communications (JSAC)*, vol. 22, no. 5, pp. 802–817, 2004.

[47] L. Dinoi, F. Sottile, and S. Benedetto, “Design of variable-rate irregular LDPC codes with low error floor,” in *Proc. IEEE International Conference Communications (ICC 2005)*, May 2005.

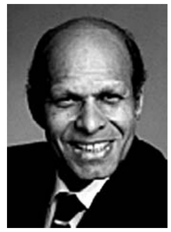
[48] R. Krashinsky, C. Batten, M. Hampton, S. Gerding, B. Pharris, J. Casper, and K. Asanovic, “The Vector-Thread architecture”, *31st International Symposium on Computer Architecture (ISCA-31)*, Munich, Germany, Jun. 2004.

Abu Baker received the B.Sc. degree from Bangladesh University of Engineering, Dhaka, Bangladesh, in 1997, and the M.S. degree from Okalahoma State University, Stillwater, in 2001. After that he worked with Rifcos-Textron Corporation in California. He is currently working toward his Ph.D. degree in Computer Engineering at the Center for Advanced Computer Studies (CACS) at University of Louisiana at Lafayette. His research interests are in the field of VLSI implementation and communication systems such as low density parity check and orthogonal frequency division multiplexing design, application specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), and mixed signal VLSI design. He has been with the student chapter of IEEE at UL Lafayette.

Soumik Ghosh obtained the B.Tech. degree in Electrical Engineering from Jamia Millia University, India in 1994. He obtained the M.S. and Ph.D. degrees from the Center for Advanced Computer Studies (CACS) at the University of Louisiana at Lafayette in 2002 and 2007, respectively. From 1998 to 2000, he worked with Schlumberger's Smart Cards & Terminals division as an R&D engineer Currently he is a Research Faculty at CACS. His areas of research include digital signal processing, energy-efficient sensor networks design, asynchronous systems, energy-recycling circuits and systems, and CMOS-MEMS.

Ashok Kumar obtained the B.Tech. degree in Computer Science & Engineering from the Institute of Technology, BHU Varanasi, India in 1990. He obtained the M.S. and Ph.D. degrees from the Center for Advanced Computer Studies (CACS) at the University of Louisiana (UL) at Lafayette in 1997 and 1999, respectively. From 1990 to 1994, he worked with Uptron India Limited, Lucknow in the capacities of Engineer and Senior Engineer. After getting his Ph.D., Dr. Kumar worked with Cadence Design Systems, USA for nearly four years in the capacity of a Senior Member of Technical Staff for R&D operations. Subsequently, he was a Research Faculty at CACS for four years. Currently he is an Assistant Professor in the Department of Computer Science at UL Lafayette. His areas of research include power and noise efficient circuit design, development of algorithms for CAD tools, digital signal processing, energy-efficient wireless sensor networks and their deployment.

Dr. Kumar has served on the program committees of ten conferences as well as on the proposal-evaluation committees of the National Science Foundation.



Magdy A. Bayoumi is the Director of the Center for Advanced Computer Studies (CACS) and Department Head of Computer Science Department, University of Louisiana at Lafayette. He is also the Edmiston Professor of Computer Engineering and Lamson Professor of Computer Science at the Center for Advanced Computer Studies, University of Louisiana at Lafayette, where he has been a faculty member since 1985. Dr. Bayoumi received the B.Sc. and M.Sc. degrees in Electrical Engineering from Cairo University, Egypt; M.Sc. degree in Computer Engineering from Washington University, St. Louis; and the Ph.D. degree in Electrical Engineering from the University of Windsor, Canada. Dr. Bayoumi's research interests include VLSI design methods and architectures, low power circuits and systems, digital signal processing architectures, parallel algorithm design, computer arithmetic, image and video signal processing, neural networks and wideband network architectures.

Dr. Bayoumi was the vice president for the technical activities of the IEEE Circuits and Systems Society. He is the chairman of the Technical Committee on Circuits and Systems for Communication and the TC on Signal Processing Design and Implementation. He was a founding member of the VLSI Systems and Applications Technical Committee and was its chairman. He is a member of the Neural Network and the Multimedia Technology Technical Committees. He has been on the technical program committee for ISCAS for several years, and he was the publication chair for ISCAS'99. He was the general chairman of the 1994 MWSCAS and he is a member of the Steering Committee of this symposium. He was the general chairman of ISCAS 2007. He was an associate editor of the Circuits and Devices Magazine, the Transaction on VLSI Systems, the Transaction on Neural Networks, and the Transaction on Circuits and Systems II. He was the co-chairman of the Workshop on Computer Architecture for Machine Perception, 1993 and is a member of the Steering Committee of this workshop. He was the general chairman for the 8th Great Lake Symposium on VLSI, 1998. He was also the general chairman of the 2000 Workshop on Signal Processing Design and Implementation. Dr. Bayoumi is an Associate Editor of INTEGRATION, the VLSI Journal, and the Journal of VLSI Signal Processing Systems. He is a regional editor for the VLSI Design Journal and on the Advisory Board of the Journal on Microelectronics Systems Integration. Dr. Bayoumi has edited and co-edited three books in the area of VLSI Signal Processing. Dr. Bayoumi served on the Distinguished Visitors Program for the IEEE Computer Society, 1991–1994 and he is on the Distinguished Lecture program of the Circuits and Systems society. He is the faculty advisor for the IEEE Computer student chapter at UL Lafayette. He won the UL Lafayette 1988 Researcher of the Year award and the 1993 Distinguished Professor award at UL Lafayette.