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Efficient Implementation of QRD-RLS Algorithm using Hardware-Software Co-design

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***Abstract*— This paper presents the implementation of QR Decomposition based Recursive Least Square (QRD-RLS) algorithm on Field Programmable Gate Arrays (FPGA) using hardware-software co-design. The system has been implemented on Xilinx Spartan 3E FPGA with Microblaze soft core processor. The hardware part consists of a custom peripheral that solves the part of the algorithm with higher computational costs and the software part consists of an embedded soft core processor that manages the control functions and rest of the algorithm. The speed and flexibility of FPGAs render them viable for such computationally intensive application. This paper also presents the implementation results and their analysis.**

Keywords: **Co-design, Microblaze, recursive least square (RLS), Xilinx.**

I. Introduction

QR based Recursive Least Square (RLS) is a well established technique for solving the Least Mean Squares (LMS) problem by calculating adaptive weights and is extensively used in applications like Adaptive beamforming, Multiple-Input-Multiple-Output (MIMO) and Software Defined Radio (SDR) [1],[2]. There is considerable research devoted to algorithms and VLSI architectures for RLS filtering [3-6], with the aim of reducing computational complexity. Much of this work has been concentrated on calculating the inverse of a matrix, in a more stable and less computational manner rather than simple matrix inversion.

The standard RLS algorithm recursively updates the weights using the matrix inversion lemma. A commonly used alternate solution is based on set of orthogonal rotations on the incoming data wherein, the the over-specified rectangular data matrix is transformed into an upper triangular form. The weights are then obtained by back substitution. This method is known as *QR decomposition based RLS*. The numerical performance achieved by implementing the algorithm using *Givens Rotation* is better than the standard RLS algorithm. An efficient implementation of RLS algorithm achieves much faster convergence than the LMS algorithm. However, its complexity increases in proportion to the square of the number of parameters to be estimated [7]. In order to circumvent this problem, our architecture is based on a pipelining technique referred to as systolic array.

Typically, the different architectures address different ends of the performance spectrum. At one end, there is a general purpose processor which provides flexibility but implements software algorithms in the order of milliseconds. At the other end there exists a fixed dedicated custom hardware which can execute algorithms in the order of nanoseconds, but is highly inflexible. However, in practice, a balance between high performance provided by hardware and the flexibility of software reconfigurable logic devices such as FPGAs is necessary in order to have high speed, and at the same time, to possess the additional degree of freedom for upgrqading the system. Moreover, FPGAs with embedded processors are flexible by nature and allow reconfiguration of logic with optimum use of resources. Hence, programmable logic and reconfiguration is now seen as a suitable solution for the rapidly changing wireless technologies. The hardware software co-design term refers to the integration of hardware and software components at the design and development stages [8]. This approach takes advantage of both the flexibility of processors and power and speed of a dedicated hardware. One of the goals of co-design is to shorten the time-to-market while reducing the design effort and costs of the designed products. The evolution of hardware-software co-design concepts has also accelerated the developments of systems on single chip. It is based on an architecture that implements an embedded processor and one or more dedicated hardware co-processors to improve the system efficiency.

In this work, we have adopted hardware software co-design methodology for implementing QRD-RLS, an adaptive filter algorithm. This algorithm is divided into two parts. The 1^{st} part involving matrix computations is made as a custom peripheral as it is computationally more expensive. The 2^{nd} part involves back substitution and other control functionalities which are executed on the processor. Interfacing between the processor and the peripheral is done using interfacing buses. Thus, such a design will enable us to make a complete system on programmable chip (SoPC). Also, it will enable us to achieve an optimum trade off between speed and flexibility.

The rest of the paper is organized as follows. Section II mentions the key points of QRD-RLS algorithm. Section III presents the architecture of the algorithm including Coordinate Rotation Digital Computer (CORDIC) algorithm and systolic arrays. Implementation methodology and results are presented in section IV and Secton V respectively. Section VI provides

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the conclusion of this work.

II. QRD-RLS Algorithm

A. QR Decomposition

QR Decomposition is an elementary operation which decomposes a matrix into an orthogonal and a triangular matrix [7]. QR decomposition of a real square matrix U is as $U = Q \times R$, where Q is an orthogonal matrix (Q^TQ = I) and R is an upper triangular matrix.

B. Givens Rotations

Givens Rotation is used to find an operator which rotates each vector through a fixed angle and this operator can be represented as a matrix [7]. Givens method is useful when adaptive algorithms like RLS are considered because in order to obtain the triangular form, the entries in the matrix are zeroed in a particular manner. This leads to a simple implementation which combined with its numerical stability results in an efficient algorithm.

C. QR decomposition based RLS

Fig. 1 shows QR decomposition based RLS algorithm. The least squares approach attempts to find the set of coefficients w_n that minimizes the sum of squares of error. Equation (1) refers to the least square solution,

$$U\mathbf{w} = \mathbf{d} + \mathbf{e} \tag{1}$$

where U is an input matrix ($m \times n$ with $m > n$), **d** is a known desired sequence and **w** is the coefficients vector to be computed such that the error vector **e** is minimized. Direct computation of coefficient vector **w** involves matrix inversion, which is undesirable for hardware implementations. QR decomposition based least square methods avoid such explicit matrix inversions and are more robust for hardware implementation.

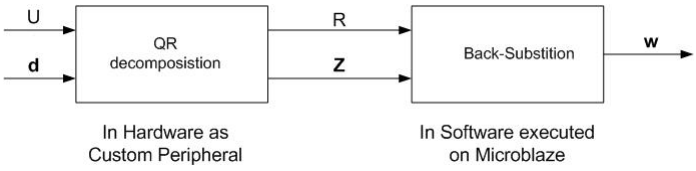

Fig. 1. QR Decomposition based RLS

The QRD is used to solve the least square problem as follows. Equation (2) shows the QR decomposition of the compound matrix [U|**d**] as,

$$[U\,|\,\mathbf{d}] = [Q\,|\,\mathbf{q}] \cdot \left[\begin{array}{c|c} R & \mathbf{z} \\ \hline 0 & \varsigma \end{array}\right] \tag{2}$$

where [Q|q] is orthogonal and $\left[\begin{array}{c|c} R & \mathbf{z} \\ \hline 0 & \varsigma \end{array}\right]$ is triangular matrix and $\mathbf{z} = Q^T\,\mathbf{d}$. Once the QRD is available, **w** is easily available through the process of back-substitution in (3)

$$R\mathbf{w} = \mathbf{z}. \tag{3}$$

Givens Rotation is applied to compound U matrix to calculate QRD. This gives QRD solution at time k. Now, in order to calculate QRD at time $k+1$ computations do not start from the beginning. QRD is recursively computed at time $k+1$ from time k by updating it as in (4),

$$\left[\begin{array}{c|c} R(k) & \mathbf{z}(k) \\ \hline \mathbf{u}_{k+1}^T & \mathbf{d}_{k+1} \end{array}\right] = Q(k+1).\left[\begin{array}{c|c} R(k+1) & \mathbf{z}(k+1) \\ \hline 0 & * \end{array}\right] \tag{4}$$

where * is a don't care entry, left hand side matrix is a *"triangular-plus-one-row-matrix"* and right hand is an orthogonal times triangular matrix. The next value of coefficient **w** follows from the back substitution in (5). This constitutes the complete QRD-RLS algorithm [7].

$$R(k+1)\mathbf{w}(k+1) = \mathbf{z}(k+1). \tag{5}$$

III. QRD-RLS Architecture

A. CORDIC in QRD

CORDIC describes a method to perform a number of mathematical functions. The algorithm is iterative and uses only additions, subtractions and shift operations [9]. This makes it more suitable for hardware implementations. CORDIC cells are used to calculate and apply the unitary transformation represented by Givens rotation.

B. Systolic Arrays

Systolic arrays have two types of processing nodes: Boundary cells and Internal cells. Boundary cells are used to calculate the Givens rotation that is applied across a particular row in a matrix. The unitary transform which is calculated by the boundary cells, is taken as an output and applied to the remainder of the row containing internal cells [5-6].

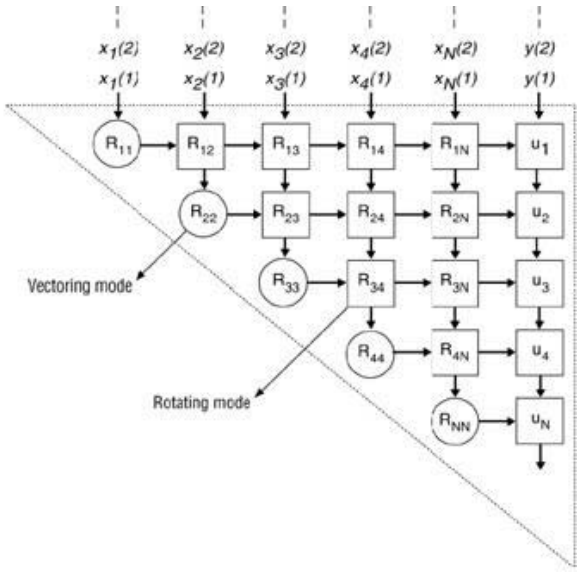

Fig. 2. Systolic Array Architecture

Fig. 2 shows the use of systolic array architecture for performing the QR decomposition of the input matrix X. Each of

the cells in the array can be implemented as a CORDIC block. Direct mapping of the CORDIC blocks to the systolic array in fully parallelized mode consumes a significant number of logic blocks but at the same time yields very fast performance. The resources required to implement the array can be reduced by trading throughput for resource consumption via mixed and discrete mapping schemes, which map multiple nodes on a single instantiation of hardware [1],[4].

C. Back Substitution

The back substitution procedure primarily involves multiplication and division operations. The Microblaze embedded soft core processor can be configured with its optional functionalities like hardware multiplier and division unit. This feature makes it ideal to implement back substitution. The CORDIC block performs the QR decomposition and stores the R and $\mathbf{z}$ values in registers accessible to the Microblaze processor, which then calculates coefficient values and stores the results back into memory.

IV. Implementation Methodology

A. Profiling and hardware-software partitioning

The complete algorithm has been programmed in C. It was executed on a 2 GHz Intel Dual Core high performance processor. As the profiler showed, matrix decomposition part took almost 94% of the total time, indicating that it is the most expensive operation in terms of computational cost, while back-substitution represented remaining 6% of the time. So, we chose to implement matrix decomposition in hardware by means of a custom peripheral. Back-substitution was executed in software on Microblaze.

B. Hardware Flow

Hardware platform describes the flexible, embedded processing subsystem which is created according to the demands of the application. The hardware platform consists of one or more processors and peripherals connected to the processor buses [10].

1) **Microblaze**: Microblaze is 32 bit Reduced Instruction Set Computer (RISC) architecture. A "Harvard" style bus architecture is used which includes 32 bit general purpose registers and separate instructions and data buses.

2) **Fast Simplex Link (FSL) bus**: FSL is a unidirectional point-to-point communication channel bus used to perform fast communication between any two design elements on the FPGA when implementing an interface to the FSL bus [10]. One FSL link was configured for communicating between Microblaze and custom peripheral.

C. Software Flow

A software platform is a collection of software drivers, libraries and, optionally, the operating system on which to build an application. The Library Generator tool configures libraries, device drivers, file systems and interrupt handlers for the embedded processor system by taking Microprocessor Software Specification (MSS) file as an input [11].

V. Implementation Results

QRD-RLS algorithm was implemented in Matlab, in order to verify its functionality. The desired data vector was obtained by reading a wave file. The input matrix was obtained by filtering this data through a channel and adding white Gaussian noise. The outputs obtained were the coefficient vectors and the error vector in modeling the channel.

A. Verification of our design

An example scenario of 3×3 matrix $(M = 3, N = 3)$ was considered because of the ease in implementing the algorithm, targeting the given Spartan 3E FPGA device. 16 bit real inputs to CORDIC blocks were considered. Fixed point representation was used to represent real numbers. The input data was the same which was used for Matlab implementation. Table I shows the comparison between the output coefficient values obtained from our design and the values obtained from Matlab for two updates of the coefficients. Update implies when all cells in the systolic array are updated with their new R and $\mathbf{z}$ values.

TABLE I
Comparison between Matlab and H/W-S/W Co-design Results

Weight Coefficients	MATLAB Results	H/W-S/W Co-design Results	Error
w1 (update1)	0.58e-2	0.65e-2	-6.071e-4
w2 (update1)	0.275e-1	0.269e-1	6.767e-4
w1 (update2)	-0.89e-2	-0.88e-2	-1.245e-4
w2 (update2)	0.255e-1	.0254e-1	1.371e-4

We see that the coefficient values obtained from our design i.e. Hardware Software (H/W-S/W) Co-design, do not match exactly with Matlab values. Table 1 also shows the error computed between both results. There is a small error value because our design is tailor made to work for four decimal places, while Matlab is a simulation software which uses IEEE double precision. Such a precision is very difficult to obtain in hardware due to resource constraints.

B. Analysis of our design

The custom peripheral was described in a high level description language like Verilog. The design was synthesized on a Xilinx Spartan-3E $XC3S500E - 4FG320$ FPGA. CORDIC blocks were used with the speed of 170 MHz. Two mapping schemes were used:- Direct mapping and Discrete mapping. In Direct mapping, where each cell of the systolic array was mapped to a CORDIC block, 5 CORDIC blocks were required for 3×3 matrix. The update time obtained was $387ns$. Update time refers to the time required before all the cells in the systolic array are updated with their R and $\mathbf{z}$ values. But it led to huge consumption of resources, amounting to 5262 slices. This number even exceeded the number of slices available in targeted FPGA device (4656). So discrete mapping was adopted. In this scheme, two CORDIC

blocks are used; one for translation operations and the other for rotation operations. The resource consumption reduced to 1689 slices, which is less than 40% of the available resources. The update time obtained was $454ns$, which is slightly higher than direct mapping.

Table II gives the resource estimates of *'Pure Hardware'* approach compared with our *'Hardware-Software Co-design'* approach for two matrix sizes of 3×3 and 4×4.

TABLE II
RESOURCE ESTIMATES OF COMPLETE DESIGN

Matrix Size	Method	Slices	LUT's	Flip Flops
3x3	Pure Hardware	3416	4588	6259
	H/W-S/W Co-design	3791	5247	5685
4x4	Pure Hardware	3844	5322	7473
	H/W-S/W Co-design	3821	5286	6190

It can be seen that for $N = M = 3$, the resource estimates of "H/W-S/W Co-design" approach and "Pure Hardware" approach differ by only a small number. For $N = M = 4$, the resource estimates of our approach are less than "Pure Hardware" approach. Thus our approach is scalable to larger matrix sizes with only a minor increase in resources, while there is a significant increase in resources for "Pure Hardware" approach. This is because in "Pure Hardware" approach back substitution part also takes resources, but this does not hold true for "H/W-S/W Co-design" approach where back substitution is executed in software. The software part of the design also lends flexibility, which is an important requirement for continually evolving standards of design cycle.

The back substitution part of the algorithm was coded in C language and it was executed on Microblaze soft core processor with clock frequency of 50 MHz. For $N = 3$, the Microblaze processor took 64 clock cycles or 1.28 μs which is acceptable for many applications. Though it is slower than a pure hardware approach, the presence of Microblaze processor lends flexibility to the whole system. Moreover, as matrix size increases, the execution time of custom peripheral which contains complex logic increases considerably as compared to software time, thereby allowing Microblaze to implement other data and control functions on the FPGA.

This QRD-RLS architecture achieves a throughput of 1.68 μs or 0.59M updates per second, which is a significant improvement over the results in [12], as shown in Table III. In addition, the resource consumption for our design is less as compared to [12]. The design is easily extendable to other matrix sizes of $N \times M$ by changing the control unit. Also, there is a trade off between area of the design and throughput by using different mapping schemes. The abundant resources of newer and bigger FPGA families support the realization of a fully parallel hardware design, should the throughput requirements of the target application demand extremely high performance.

TABLE III
COMPARISON BETWEEN H/W-S/W CO-DESIGN AND REFERENCE [12] RESULTS

Parameter	H/W-S/W Co-design	Ref.[12]
Execution time	1.68 μs	3.76 μs
Resources(Total Logic Cells)	14723	14876

VI. CONCLUSION

A novel design methodology of Hardware Software Co-design has been proposed in this paper. QRD-RLS algorithm has been implemented using Xilinx Spartan 3E FPGA with embedded Microblaze soft core processor. This QRD-RLS architecture achieves a throughput of 1.68 μs or 0.59M updates per second. The interfacing of the peripheral with Microblaze embedded processor provides an element of flexibility, which cannot be achieved in pure hardware approach. The flexibility will allow the system to configure adaptively for varying wireless conditions and external requirements. Moreover, it facilitates to create a SoPC. The independent custom unit which does the decomposition of the matrix can be used in any application depending upon different conditions.

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