

Lab 05 - Combinatorial Logic

In this lab, you've learned real world applications of digital logic, as well as how to assemble your own Verilog modules. In addition, you've learned how the constraints file maps your inputs and outputs to real pins on the FPGA.

Rubric

Item	Description	Value
Summary Answers	Your writings about what you learned in this lab.	25%
Question 1	Your answers to the question	25%
Question 2	Your answers to the question	25%
Question 3	Your answers to the question	25%

Lab Summary

This lab was more focused on combinational logic and how the gates can be combined to make something more complex than we originally thought. The stairway light example was a situation of how "common knowledge" is not as simple as you think and it uses the XOR logic. We also used the XOR logic to do addition in binary. We built a 1-bit adder for the sum and the carry and combined multiple adders to create a 2-bit full adder. The lab helped reinforce how to practically use the logic gates and use them as building blocks for bigger operations.

Lab Questions

1 - Explain the role of the Top Level file.

It acts as the main module that connects all of the smaller functional files. It reminds me of the main() method in JAVA. It connects all the different modules to form a working program. It is also where all the variables are declared for the inputs and outputs.

2 - Explain the function of the Constraints file.

It maps the signals to physical pins to ensure the hardware connections are set properly. It can give the pin locations and voltage standards to match the board. It can also set constraints on timing. In this lab it was used to assign switches and LEDs to the proper pins.

3 - How might one add more than two bits together?

If you wanted to add more than two bits you would just use multiple full adders. You could pass the carry-out of one of the adders as the carry-in to the next.

Code Submission

Upload a .zip of all your code or a public repository on GitHub.