Lab 09 - Synchronous Circuits

In this lab, you've learned about behavioral Verilog and how to use it to implement circuits with memory. You've also learned how to utilize this memory in conjunction with multiplexers and demultiplexers to make a simple storage system.

Rubric

Item	Description	Value
Summary Answers	Your writings about what you learned in this lab.	25%
Question 1	Your answers to the question	25%
Question 2	Your answers to the question	25%
Question 3	Your answers to the question	25%

Lab Summary

This lab was about the logic behind synchronous circuits and how to make memory work on an FPGA. We start with a D-Latch and used that to build the 4-byte memory system. We also had to use demuxes and muxes to control what data went where. The idea was learning how memory works in digital system and how to make it update.

Lab Questions

1 - Why can we not just use structural Verilog to implement latches?

I believe it can not be used for latches because it creates combinational loops and the tools don't like that. It will simulate but you can not actually build it. Using the behavioral reg and always make memory that works.

2 - What is the meaning of `always @(*)` in a sensitivity block?

It means the block should run anytime any input inside of it changes. The (*) is just an all.

3 - What importance is memory to digital circuits?

It lets the circuits store values instead of just reacting to inputs. Without memory you can not keep track of the past information. It is what lets you do more than basic logic.

Code Submission

https://github.com/HunterMcCallister/SynchronousCircuits-Hunter-McCallister-Diego-Dominguez