ASM1053 Datasheet

SuperSpeed USB to SATA Bridge Controller

Environmentally hazardous materials are not used in this product.

Revision History

Rev.	Date	Description
0.1	April 8, 2011	Initial Release
0.2	June 29, 2011	Update the name of pinout Update the electrical spec Update the package information to 6x6 QFN48
0.3	Oct. 4, 2011	Update the general description and feature to support SATA3.0 Update the electrical spec of Absolute Maximum Ratings and Recommended Operating Conditions
0.4	Oct. 27, 2011	Update the pin description Add the Strapping Table Add the ESD specification Add the electrical specification of 30MHz clock input Update the Package Mechanical Specification
0.5	Dec. 23, 2011	Remove the feature of SATA3.0 Add the pin 49 into pin description Update the maximum spec of core power Update the electrical spec of IO power and internal regulator

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General Description

ASM1053 is the ASMedia 2nd generation single chip solution to bridge the SuperSpeed USB (USB3.0) and High Speed USB (USB2.0) to Serial ATA host interface. It is highly integrated with ASMedia SuperSpeed USB3.0, High Speed USB2.0 and SATA1.5/3.0 Gbps self-design PHYs. Customers can easily enhaced their storage device performace via ASM1053 since it is also integrated 8-bit micro-processor and embedded RAM to provide a leading edge solution in USB to SATA device enclosure market.

Features

- ◇ Compliant with USB3.0 Specification Revision 1.0
- ◇ Compliant with USB Specification Revision 2.0
- ◇ Support USB Super-Speed, High-Speed and Full-Speed Operation
- ◇ Support USB Mass Storage Class, Bulk-Only Transport Specification Revision 1.3
- ◇ Support UAS Attached SCSI Protocol Specification Revision 1.0
- ◇ Compliance with Serial ATA Specification Revision 2.6
- ◇ Support Spread Spectrum Control of USB3.0 and SATA interface to improve the EMI performance
- ◇ Support ATA/ATAPI Packet Command Set
- ◇ Support ATA/ATAPI LBA48 addressing mode
- ◇ Integrated 8-bit micro-processor with embedded program RAM and ROM
- ◇ Support SPI NVRAM for Vender Specific Application of USB Device Controller
- ◇ Support multi-GPIO pins
- ◇ Support two programmable PWM controller
- ◇ Support 20/25/30MHz with external crystal mode or 30MHz with Clock input mode via strapping
- ◇ Integrated internal 5V to 3.3V and 3.3V to 1.2V voltage regulator
- ◇ Support 3.3V IO power and 1.2V core power
- ◇ HBM ESD 2KV

Package Type

- ◇ Green Package 6x6 QFN 48L (Pb-free)

Functional Diagram
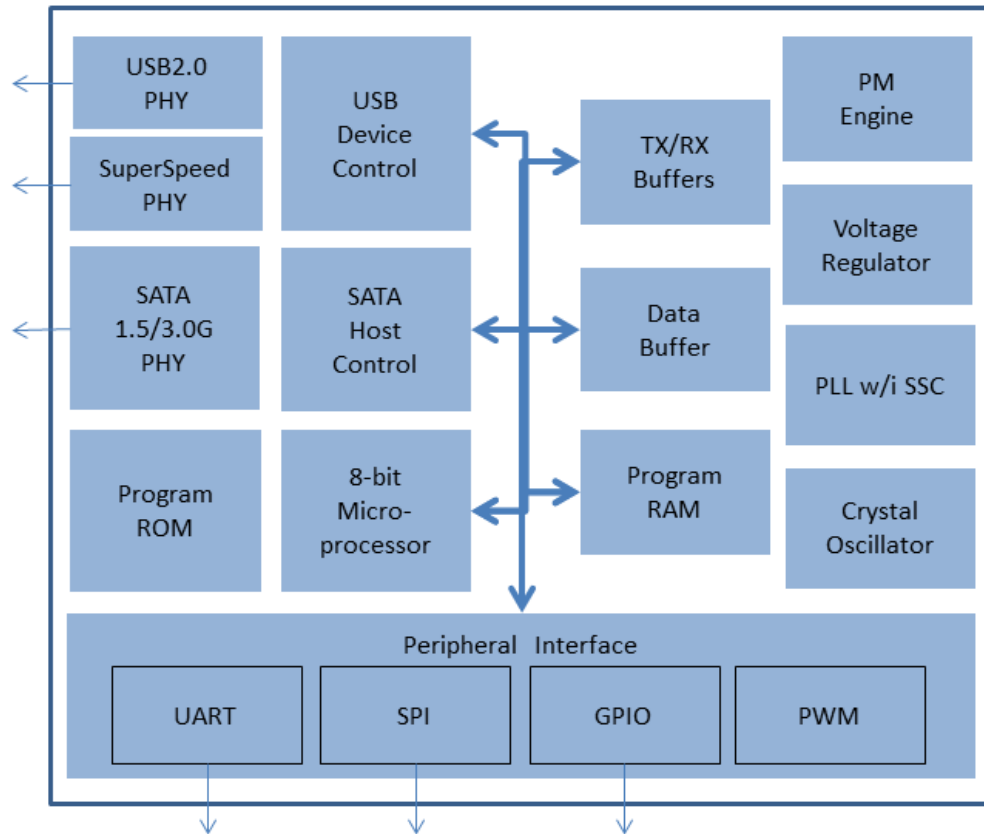
Figure 1: Functional Diagram of ASM1053

Pinout Diagrams
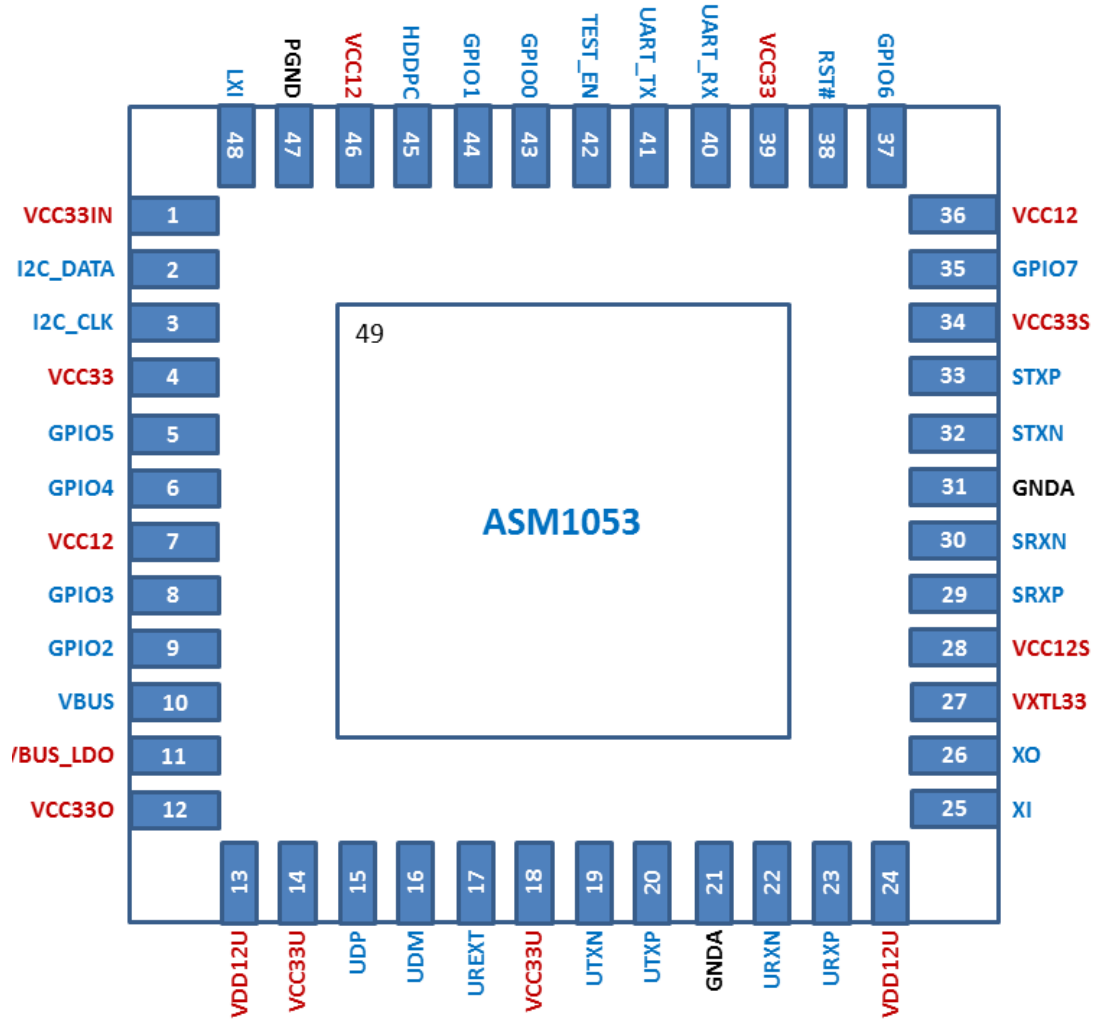
Figure 2: ASM1053 Pinout

Pin Descriptions

This section provides a detailed description of each signal. The following notations are used to describe the signal type.

I/O Type	Definition
I	Input pin
O	Output pin
B	Bi-directional pin
P	Power pin
G	Ground pin
OD	Open Drain

Pin No.	Name	TYPE	Descriptions
USB interface			
16	UDM	DB	USB2.0 negative Data Signal
15	UDP	DB	USB2.0 positive Data Signal
19	UTXN	DO	SuperSpeed USB negative Transmitter Signal
20	UTXP	DO	SuperSpeed USB positive Transmitter Signal
22	URXN	DI	SuperSpeed USB negative Receiver Signal
23	URXP	DI	SuperSpeed USB positive Receiver Signal
SATA interface			
29	SRXP	DI	SATA positive Receiver Signal
30	SRXN	DI	SATA negative Receiver Signal
32	STXN	DO	SATA negative Transmitter Signal
33	STXP	DO	SATA positive Transmitter Signal
System Signals			
42	TEST_EN	I	Test Enable Signal, with internal pull-down resistor 0: Normal Mode (Default) 1: Test Mode Enable
2	I2C_DATA	B	Used as I2C_DATA signal or SPI_DI signal, defined by strapping pin 37 GPIO6. Used as General Purpose IO after power on. Integrated pull-up resistor.
3	I2C_CLK	B	Used as I2C_CLK signal or SPI_CLK signal, defined by strapping pin 37 GPIO6. Used as General Purpose IO after power on. Integrated pull-up resistor.
5	GPIO5	B	General Purpose IO, used as SPI_DO, with internal pull-up resistor.
6	GPIO4	B	General Purpose IO, used as SPI_CS0, with internal pull-up resistor.
8	GPIO3	B	General Purpose IO, used as strapping pin for clock source select while power on. Refer to the strapping table. Integrated pull-up resistor.
9	GPIO2	B	General Purpose IO, used as SPI_CS1, with internal pull-up resistor.
35	GPIO7	B	General Purpose IO, use as strapping for clock source select while power on. Refer to the strapping table. Integrated pull-up resistor.
37	GPIO6	B	General Purpose IO, used as strapping for external ROM enabling via SPI interface. Refer to the strapping table. Integrated pull-up resistor.
40	UART_RX	B	URAT_RX while debug mode, Used as General Purpose IO after power on. Integrated pull-up resistor.
41	UART_TX	B	UART_TX while debug mode, Used as General Purpose IO after power on. Integrated pull-up resistor.
43	GPIO0	B	General Purpose IO. Integrated pull-up resistor.
44	GPIO1	B	General Purpose IO. Integrated pull-up resistor.
45	HDDPC	B	HDD power control pin, use as General Purpose IO. Integrated pull-up resistor. 0: Hard Drive Power Off 1: Hard Drive Power On
10	VBUS	I	USB Cable Power Detector
17	UREXT	P	External Reference Resistor with 12.1Kohm +/-1%

Pin No.	Name	TYPE	Descriptions
38	RST#	I	Power Reset pin
Clock Interface			
25	XI	I	Crystal input or Clock input pin
26	XO	O	Crystal output or Clock output pin
27	VXTLH	P	Power for Crystal and PLL circuit for 3.3V or 2.5V
Voltage Regulator			
11	VBUS_LDO	P	VBUS 5V voltage regulator input
12	VCC33O	P	3.3V regulator output
1	VCC33IN	P	3.3V regulator input
48	LXI	P	Connect with external inductor
47	PGND	G	Ground for voltage regulator
Power and Ground			
14, 18	VCC33U	P	USB 3.3V power pin
34	VCC33S	P	SATA 3.3V power pin
13, 24	VDD12U	P	USB 1.2V power pin
28	VCC12S	P	SATA 1.2V power pin
7, 36, 46	VCC12	P	1.2V Core power
4, 39	VCC33	P	IO power for 3.3V
21, 31, 49	GNDA	G	Analog Ground Pin 49 is the exposed pad connected to ground on PCB

Strapping Table

Pin	Function	Description
GPIO6	SPI Interface Select	0: SPI for External ROM 1: I2C (Default)
GPIO[3,7]	Clock Select	00: 25MHz Crystal 01: 30MHz Clock Input 10: 20MHz Crystal 11: 30MHz Crystal (Default)

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Range	Units
Power Supply for 1.2V	-0.5~+1.6	V
Power Supply for 3.3V	-0.5~+4.5	V
DC Input Voltage	-0.5~+4.5	V
Output Voltage	-0.5~+4.5	V
Storage Temperature	-65~150	^{0}C
HBM ESD	+/-2	KV
MM ESD	+/-200	V

Recommended Operating Conditions

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{CC33}	3.3V IO Power Supply	3.0	3.3	3.6	V
V_{CC33U}	USB 3.3V Analog Power Supply	3.0	3.3	3.6	V
V_{CC33S}	SATA 3.3V Analog Power Supply	3.0	3.3	3.6	V
V_{CC12}	1.2V Core Power Supply	1.05	1.1	1.2	V
V_{CC12U}	USB 1.2V Power Supply	1.05	1.1	1.2	V
V_{CC12S}	SATA 1.2V Power Supply	1.05	1.1	1.2	V
V_{BUS_LDO}	5V to 3.3V LDO input voltage	4.5	5	5.5	V
V_{CC33IN}	3.3V to 1.2V Switching Regulator Input	3.0		3.6	V
T_C	Operating Case Temperature	0	25	95	^{0}C
T_J	Operating Junction Temperature	0	25	120	^{0}C

DC Electrical Characteristics for VBUS pins (Temperature = 55°C)

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Level	2			V
V_{IL}	Input Low Level			0.8	V
V_{HYS}	Input Hysteresis	0.57	0.6	0.65	mV
V_{TH-L2H}	VTH of Schmitt Trigger low to high	1.4		1.8	V
V_{TH-H2L}	VTH of Schmitt Trigger high to low	0.85		1.10	V

DC Electrical Characteristics for GPIO pins (Temperature = 55°C)

Symbols	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input High Level	2			V
V_{IL}	Input Low Level			0.8	V
V_{HYS}	Input Hysteresis	0.57	0.6	0.65	V
V_{TH-L2H}	VTH of Schmitt Trigger low to high	1.38		1.8	V
V_{TH-H2L}	VTH of Schmitt Trigger high to low	0.82		1.15	V
R_{UP}	Internal Pull-up resistance while Vin=0V	67	98.3	140	KΩ
	Internal Pull-up resistance while Vin=VCCH/2 V	37.85	55	77	KΩ
I_{IL}	Input pull-up leakage current while Vin=0V	21.4	33.6	53.7	uA
	Input pull-up leakage current while Vin=VCCH/2 V	19.5	30	47.6	uA

Symbols	Parameter	Min.	Typ.	Max.	Units
V$_{OH}$	Output High Voltage	2.64			V
V$_{OL}$	Output Low Voltage			0.66	V
I$_{OH}$	Driving Current of Output High		12		mA
I$_{OL}$	Driving Current of Output Low		12		mA

DC Electrical Characteristics for RST# pins (Temperature = 55°C)

Symbols	Parameter	Min.	Typ.	Max.	Units
V$_{IH}$	Input High Level	2.6			V
V$_{IL}$	Input Low Level			1.4	V
V$_{HYS}$	Input Hysteresis	0.218	0.235	0.25	V
V$_{TH-L2H}$	VTH of Schmitt Trigger low to high	1.88		2.58	V
V$_{TH-H2L}$	VTH of Schmitt Trigger high to low	1.65		2.35	V
I$_{IL}$	Input pull-up leakage current while Vin=0V			1	uA

External Crystal Electrical Specification

Note: please refer to the figure 3

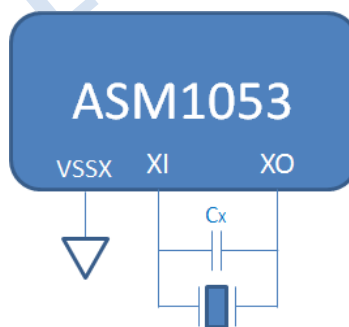| Symbol	Parameter	Min.	Typ	Max.	Unit
f$_{XTAL}$	Frequency		20/25/30		MHz
Δf$_{XTAL}$	Long Term Stability (at 25^{0}C)	-30		30	ppm
T$_C$	Temperature Stability	-30		30	ppm
F$_A$	Aging	-5		5	ppm
C$_L$	Load Capacitance (Single-end mode)		16		pF
C$_0$	Shunt Capacitance	1	3	7	pF

Figure 3: Differential Crystal Design

Differential Clock Oscillator Electrical Specification

Note: please refer to the figure 3

Symbol	Parameter	Min.	Typ	Max.	Unit
f$_{CLK}$	Frequency		20/25/30		MHz
Δf$_{CLK}$	Long Term Stability (all condition)	-150		150	ppm

Symbol	Parameter	Min.	Typ	Max.	Unit
C$_X$	External Load Capacitance (Differential mode)		8		pF
C$_{TOTAL}$	Total External Equivalent Capacitance from XI pin to XO pin (Differential mode)	9	11	15	Pf
R$_{TOTAL}$	Total External Equivalent Series Resistance from XI pin to XO pin			60	Ω

External Clock Input Electrical Specification

Symbol	Parameter	Min.	Typ	Max.	Unit
f$_{CLK}$	Frequency		30		MHz
Δf$_{CLK}$	Long Term Stability (all condition)	-100		100	ppm
Jitter	Input Clock cycle to cycle jitter Tolerance			150	ps
	Duty Cycle	45		55	%
t$_R$	Rising Edge rate	1.0		2.0	V/ns
t$_F$	Falling Edge rate	1.0		2.0	V/ns
V$_{IH}$	Clock Input High Level	2			V
V$_{IL}$	Clock Input Low Level			1.00	V

Internal Linear Regular Electrical Specification

Symbol	Parameter	Min.	Typ	Max.	Unit
V$_{IN\_LINEAR}$	Input Voltage Range for internal linear regulator	4.5	5	5.5	V
V$_{OUT\_LINEAR}$	Output Voltage Range for internal linear regulator	3.2	3.45	3.6	V

Internal Switching Regular Electrical Specification

Symbol	Parameter	Min.	Typ	Max.	Unit
V$_{IN\_SWITCH}$	Input Voltage Range for internal switching regulator	3.0		3.6	V
V$_{OUT\_SWITCH}$	Output Voltage Range for internal switching regulator	1.05	1.1	1.2	V
ΔV$_N$ (p-p)	3.3V input voltage noise/ripple Range	-8		8	%
F$_{OSC}$	OSC frequency		1.7		MHz
IP$_{(LM)}$	P-channel current limiter		1		A

➢ **Strong recommend to have 10uF decoupling capacitor placed close to pin3 to filter the noise/ripple of 3.3V switching regulator input.**

Power Consumption Characteristics

Symbols	Parameter	Condition	USB3.0			USB2.0			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I$_{33}$	Total Consumption Current for 3.3V Power	U0	36	38	40	47	50	53	mA
		Idle	23	25	28	34	38	42	mA
		U1/U2	9	10	11	N/A	N/A	N/A	mA
		U3	0	0	0	0	0	0	mA

Symbols	Parameter	Condition	USB3.0			USB2.0			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{12}	Total Consumption Current for 1.2V Power	U0	205	215	225	135	143	150	mA
		Idle	135	150	165	68	75	83	mA
		U1/U2	85	94	104	N/A	N/A	N/A	mA
		U3	2.3	3	4	2.3	3	4	mA
P_{VBUS}	Total Power Consumption for 5V VBUS	U0	590	620	650	500	535	570	mW
		Idle	390	430	470	310	340	370	mW
		U1/U2	205	235	265	N/A	N/A	N/A	mW
		U3	5.8	7.5	10	5.8	7.5	10	mW

Package Information

TOP VIEW

BOTTOM VIEW

SIDE VIEW
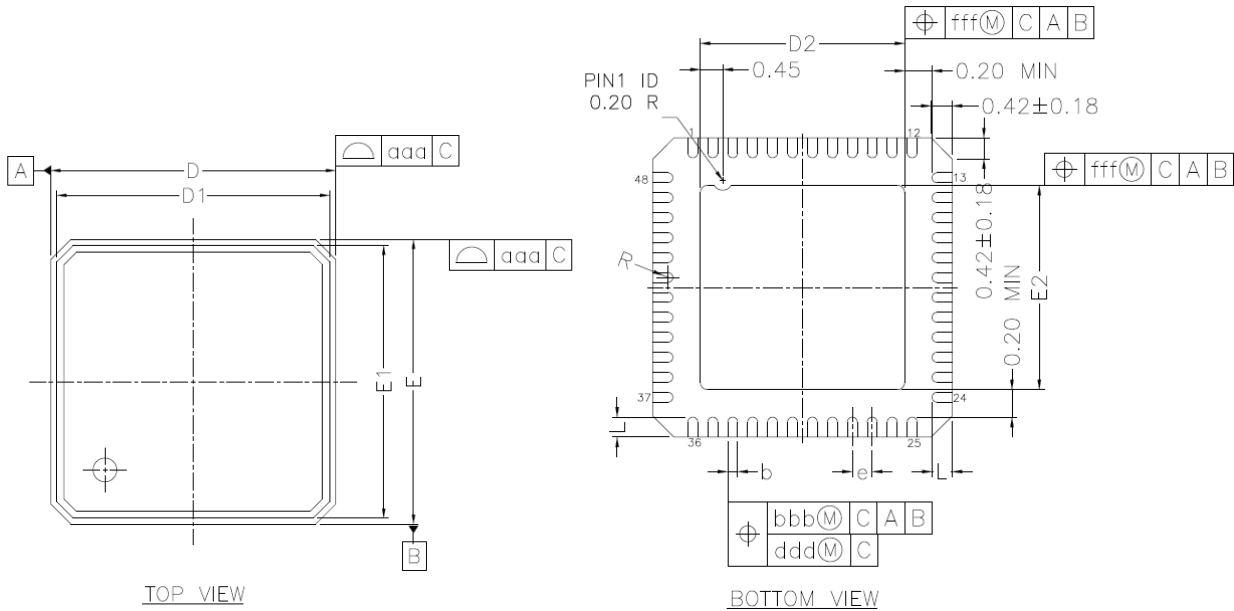
* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.00	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	6.00 bsc			0.236 bsc		
D1	5.75 bsc			0.226 bsc		
D2	3.95	4.10	4.25	0.156	0.161	0.167
E	6.00 bsc			0.236 bsc		
E1	5.75 bsc			0.226 bsc		
E2	3.95	4.10	4.25	0.156	0.161	0.167
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.40 bsc			0.016 bsc		
$\theta1$	0°	———	14°	0°	———	14°
R	0.075	———	———	0.003	———	———
TOLERANCES OF FORM AND POSITION						
aaa	———	———	0.10	———	———	0.004
bbb	———	———	0.07	———	———	0.003
ccc	———	———	0.10	———	———	0.004
ddd	———	———	0.05	———	———	0.002
eee	———	———	0.08	———	———	0.003
fff	———	———	0.10	———	———	0.004
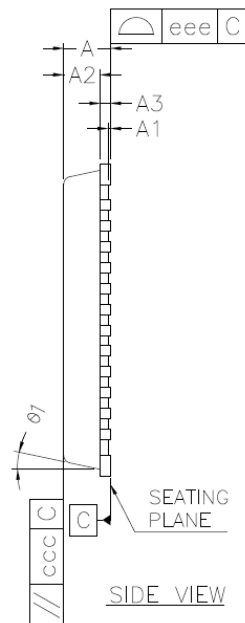
NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. —1994.
4.DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED
　BETWEEN 0.20 AND 0.25 mm FROM TERMINALTIP.
5.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE
　PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7.PACKAGE WARPAGE MAX 0.08 mm.
8.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED
　PAD FROM MEASURING.
9.APPLIED ONLY TO TERMINALS.
10.PACKAGE CORNERS UNLESS
　OTHERWISE SPECIPIED
　ARE R0.175±0.025 mm.

Figure 4:   Mechanical Specification – QFN 48L