6. I/O Features in the Cyclone III Device Family

CIII51007-3.4

This chapter describes the I/O features offered in the Cyclone® III device family (Cyclone III and Cyclone III LS devices).

The I/O capabilities of the Cyclone III device family are driven by the diversification of I/O standards in many low-cost applications, and the significant increase in required I/O performance. Altera's objective is to create a device that accommodates your key board design needs with ease and flexibility.

The I/O flexibility of the Cyclone III device family is increased from the previous generation low-cost FPGAs by allowing all I/O standards to be selected on all I/O banks. Improvements to on-chip termination (OCT) support and the addition of true differential buffers have eliminated the need for external resistors in many applications, such as display system interfaces. Altera's Quartus® II software completes the solution with powerful pin planning features that allow you to plan and optimize I/O system designs even before the design files are available.

This chapter contains the following sections:

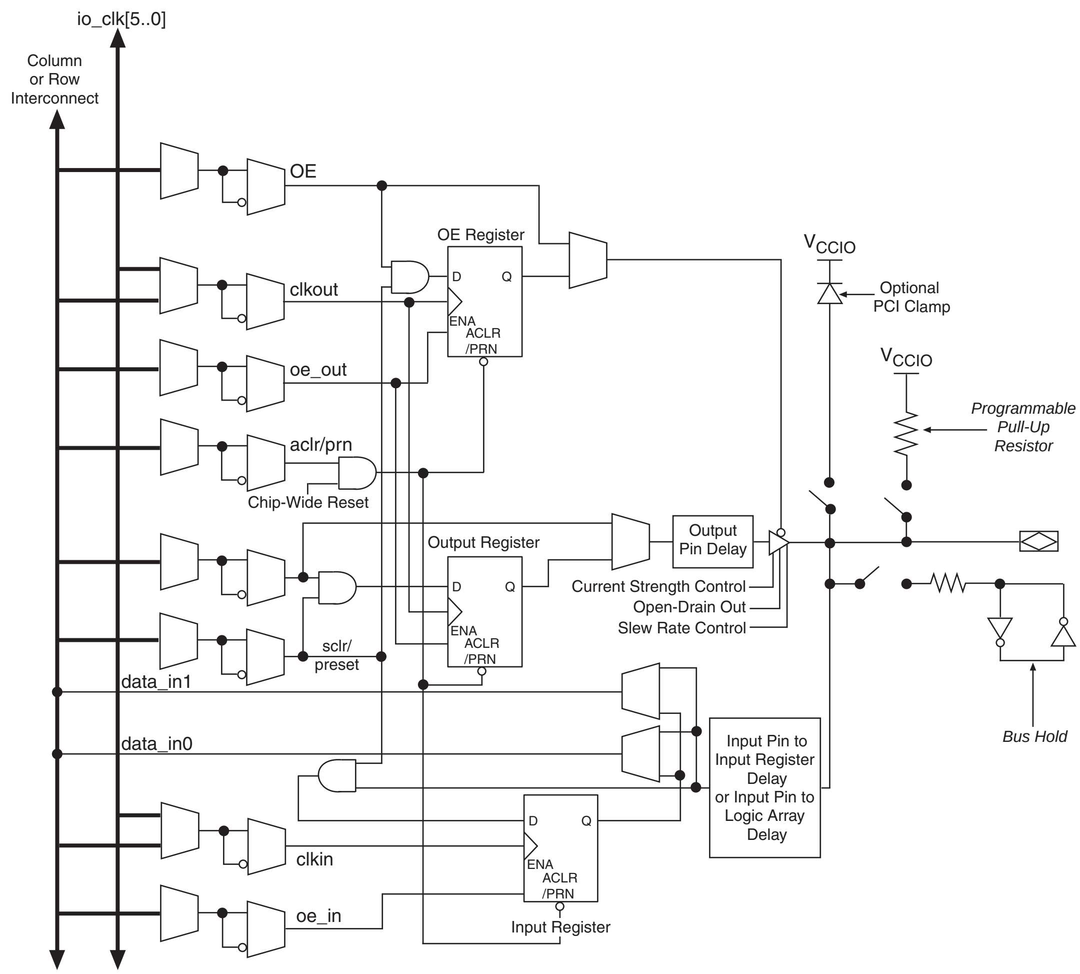
Cyclone III Device Family I/O Elements

Cyclone III device family I/O elements (IOEs) contain a bidirectional I/O buffer and five registers for registering input, output, output-enable signals, and complete embedded bidirectional single-data rate transfer. I/O pins support various single-ended and differential I/O standards.

The IOE contains one input register, two output registers, and two output-enable (OE) registers. The two output registers and two OE registers are used for DDR applications. You can use input registers for fast setup times and output registers for fast clock-to-output times. Additionally, you can use OE registers for fast clock-to-output enable timing. You can use IOEs for input, output, or bidirectional data paths.

Figure 6–1 shows the Cyclone III device family IOE structure.

Figure 6–1. Cyclone III Device Family IOE in a Bidirectional I/O Configuration



I/O Element Features

The Cyclone III device family IOE offers a range of programmable features for an I/O pin. These features increase the flexibility of I/O utilization and provide an alternative to reduce the usage of external discrete components to on-chip, such as a pull-up resistor and a diode.

Programmable Current Strength

The output buffer for each Cyclone III device family I/O pin has a programmable current strength control for certain I/O standards.

The **LVTTL**, **LVCMOS**, **SSTL-2 Class I** and **Class II**, **SSTL-18 Class I** and **Class II**, **HSTL-18 Class I** and **Class II**, **HSTL-15 Class I** and **Class II**, and **HSTL-12 Class I** and **Class II** I/O standards have several levels of current strength that you can control.

Table 6–1 lists the possible settings for I/O standards with current strength control. These programmable current strength settings are a valuable tool in helping decrease the effects of simultaneously switching outputs (SSO) in conjunction with reducing system noise. The supported settings ensure that the device driver meets the specifications for `IOH` and `IOL` of the corresponding I/O standard.

When you use programmable current strength, on-chip series termination is not available.

Table 6–1. Programmable Current Strength *(1)*

I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)	
	Top and Bottom I/O Pins	Left and Right I/O Pins
1.2-V LVCMOS	2, 4, 6, 8, 10,12	2, 4, 6, 8,10
1.5-V LVCMOS	2, 4, 6, 8, 10, 12,16	2, 4, 6, 8, 10, 12,16
1.8-V LVTTL/LVCMOS	2, 4, 6, 8, 10, 12,16	2, 4, 6, 8, 10, 12,16
2.5-V LVTTL/LVCMOS	4, 8, 12,16	4, 8, 12,16
3.0-V LVCMOS	4, 8, 12,16	4, 8, 12,16
3.0-V LVTTL	4, 8, 12,16	4, 8, 12,16
3.3-V LVCMOS *(2)*	***2***	***2***
3.3-V LVTTL *(2)*	4, ***8***	4, ***8***
HSTL-12 Class I	8, 10,12	8, 10
HSTL-12 Class II	14	—
HSTL-15 Class I	8, 10, 12	8, 10, 12
HSTL-15 Class II	16	16
HSTL-18 Class I	8, 10, 12	8, 10, 12
HSTL-18 Class II	16	16
SSTL-18 Class I	8, 10, 12	8, 10, 12
SSTL-18 Class II	12, 16	12, 16
SSTL-2 Class I	8, 12	8, 12
SSTL-2 Class II	16	16
BLVDS	8, 12, 16	8, 12, 16

Notes to Table 6–1:

(1) The default setting in the Quartus II software is 50-Ω OCT without calibration for all non-voltage reference and **HSTL/SSTL Class I** I/O standards. The default setting is 25-Ω OCT without calibration for **HSTL/SSTL Class II** I/O standards.

(2) The default current setting in the Quartus II software is highlighted in bold italic for **3.3-V LVTTL** and **3.3-V LVCMOS** I/O standards.

For information about how to interface the Cyclone III device family with 3.3-, 3.0-, or 2.5-V systems, refer to the guidelines provided in *AN 447: Interfacing Cyclone III and Cyclone IV Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems*.

Slew Rate Control

The output buffer for each Cyclone III device family I/O pin provides optional programmable output slew-rate control. The Quartus II software allows three settings for programmable slew rate control—0, 1, and 2—where 0 is the slow slew rate and 2 is the fast slew rate. The default setting is 2. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients in the system. A slower slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Because each I/O pin has an individual slew-rate control, you can specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges. Slew rate control is available for single-ended I/O standards with current strength of 8 mA or higher.

You cannot use the programmable slew rate feature when using OCT with or without calibration.

You cannot use the programmable slew rate feature when using the **3.0-V PCI**, **3.0-V PCI-X**, **3.3-V LVTTL**, and **3.3-V LVCMOS** I/O standards. Only fast slew rate (default) setting is available.

Open-Drain Output

The Cyclone III device family provides an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that are asserted by multiple devices in your system.

Bus Hold

Each Cyclone III device family user I/O pin provides an optional bus-hold feature. The bus-hold circuitry holds the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage in which noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent overdriving signals.

If you enable the bus-hold feature, the device cannot use the programmable pull-up option. Disable the bus-hold feature when the I/O pin is configured for differential signals. Bus-hold circuitry is not available on dedicated clock pins.

Bus-hold circuitry is only active after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

For the specific sustaining current for each V_{CCIO} voltage level driven through the resistor and for the overdrive current used to identify the next driven input level, refer to the *Cyclone III Device Data Sheet* and *Cyclone III LS Device Data Sheet* chapters.

Programmable Pull-Up Resistor

Each Cyclone III device family I/O pin provides an optional programmable pull-up resistor while in user mode. If you enable this feature for an I/O pin, the pull-up resistor holds the output to the V_{CCIO} level of the output pin's bank.

If you enable the programmable pull-up, the device cannot use the bus-hold feature. Programmable pull-up resistors are not supported on the dedicated configuration, JTAG, and dedicated clock pins.

When the optional `DEV_OE` signal drives low, all I/O pins remain tri-stated even if the programmable pull-up option is enabled.

Programmable Delay

The Cyclone III device family IOE includes programmable delays to ensure zero hold times, minimize setup times, increase clock-to-output times, or delay the clock input signal.

A path in which a pin directly drives a register may require a programmable delay to ensure zero hold time, whereas a path in which a pin drives a register through combinational logic may not require the delay. Programmable delays minimize setup time. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output registers. Each dual-purpose clock input pin provides a programmable delay to the global clock networks.

Table 6–2 lists the programmable delays for the Cyclone III device family.

Table 6–2. Cyclone III Device Family Programmable Delay Chain

Programmable Delays	Quartus II Logic Option
Input pin-to-logic array delay	Input delay from pin to internal cells
Input pin-to-input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin
Dual-purpose clock input pin delay	Input delay from dual-purpose clock pin to fan-out destinations

There are two paths in the IOE for an input to reach the logic array. Each of the two paths can have a different delay. This allows you to adjust delays from the pin to the internal logic element (LE) registers that reside in two different areas of the device. You must set the two combinational input delays with the input delay from pin to internal cells logic option in the Quartus II software for each path. If the pin uses the input register, one of the delays is disregarded and the delay is set with the input delay from pin to input register logic option in the Quartus II software.

The IOE registers in each I/O block share the same source for the preset or clear features. You can program preset or clear for each individual IOE, but you cannot use both features simultaneously. You can also program the registers to power-up high or low after configuration is complete. If programmed to power-up low, an asynchronous clear can control the registers. If programmed to power-up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of the active-low input of another device upon power up. If one register in an IOE uses a preset or clear signal, all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available for the IOE registers.

For more information about the input and output pin delay settings, refer to the *Area and Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

PCI-Clamp Diode

The Cyclone III device family provides an optional PCI-clamp diode enabled input and output for each I/O pin. Dual-purpose configuration pins support the diode in user mode if the specific pins are not used as configuration pins for the selected configuration scheme. For example, if you are using the active serial (AS) configuration scheme, you cannot use the clamp diode on the `ASDO` and `nCSO` pins in user mode. Dedicated configuration pins do not support the on-chip diode.

The PCI-clamp diode is available for the following I/O standards:

- **3.3-V LVTTL**
- **3.3-V LVCMOS**
- **3.0-V LVTTL**
- **3.0-V LVCMOS**
- **2.5-V LVTTL/LVCMOS**
- **PCI**
- **PCI-X**

If the input I/O standard is **3.3-V LVTTL**, **3.3-V LVCMOS**, **3.0-V LVTTL**, **3.0-V LVCMOS**, **2.5-V LVTTL**/**LVCMOS**, **PCI**, or **PCI-X**, the PCI clamp diode is enabled by default in the Quartus II software.

For more information about the Cyclone III device family PCI-clamp diode support, refer to *AN 447: Interfacing Cyclone III and Cyclone IV Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems.*

LVDS Transmitter Programmable Pre-Emphasis

The Cyclone III device family true **LVDS** transmitter supports programmable pre-emphasis. Programmable pre-emphasis is used to compensate the frequency-dependent attenuation of the transmission line. It increases the amplitude of the high-frequency components of the output signal, which cancels out much of the high-frequency loss of the transmission line.

The Quartus II software allows two settings for programmable pre-emphasis control—0 and 1, in which 0 is pre-emphasis off and 1 is pre-emphasis on. The default setting is 1. The amount of pre-emphasis needed depends on the amplification of the high-frequency components along the transmission line. You must adjust the setting to suit your designs, as pre-emphasis decreases the amplitude of the low-frequency component of the output signal as well.

For more information about the Cyclone III device family high-speed differential interface support, refer to the *High-Speed Differential Interfaces in the Cyclone III Device Family* chapter.

OCT Support

The Cyclone III device family features OCT to provide output impedance matching and termination capabilities. OCT helps to prevent reflections and maintain signal integrity while minimizing the need for external resistors in high pin-count ball grid array (BGA) packages.

The Cyclone III device family provides output driver on-chip impedance matching and on-chip series termination for single-ended outputs and bidirectional pins. For bidirectional pins, OCT is active only for output.

When using on-chip series termination, programmable current strength is not available.

There are two ways to implement OCT in the Cyclone III device family:

- OCT with calibration
- OCT without calibration

Table 6–3 lists the I/O standards that support output impedance matching and series termination.

Table 6–3. Selectable I/O Drivers for On-Chip Series Termination with and Without Calibration Setting

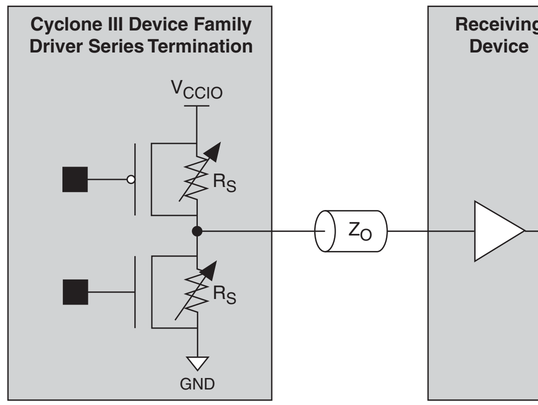
I/O Standard	On-Chip Series Termination with Calibration Setting, in ohms (Ω)		On-Chip Series Termination Without Calibration Setting, in ohms (Ω)	
	Row I/O	Column I/O	Row I/O	Column I/O
3.0-V LVTTL/LVCMOS	50, 25	50, 25	50, 25	50, 25
2.5-V LVTTL/LVCMOS	50, 25	50, 25	50, 25	50, 25
1.8-V LVTTL/LVCMOS	50, 25	50, 25	50, 25	50, 25
1.5-V LVCMOS	50, 25	50, 25	50, 25	50, 25
1.2-V LVCMOS	50	50, 25	50	50, 25
SSTL-2 Class I	50	50	50	50
SSTL-2 Class II	25	25	25	25
SSTL-18 Class I	50	50	50	50
SSTL-18 Class II	25	25	25	25
HSTL-18 Class I	50	50	50	50
HSTL-18 Class II	25	25	25	25
HSTL-15 Class I	50	50	50	50
HSTL-15 Class II	25	25	25	25
HSTL-12 Class I	50	50	50	50
HSTL-12 Class II	—	25	—	25

On-Chip Series Termination with Calibration

The Cyclone III device family supports on-chip series termination with calibration in all banks. The on-chip series termination calibration circuit compares the total impedance of the output buffer to the external 25-Ω ±1% or 50-Ω ±1% resistors connected to the RUP and RDN pins, and dynamically adjusts the output buffer impedance until they match (as shown in Figure 6–2).

The R_S shown in Figure 6–2 is the intrinsic impedance of the transistors that make up the output buffer.

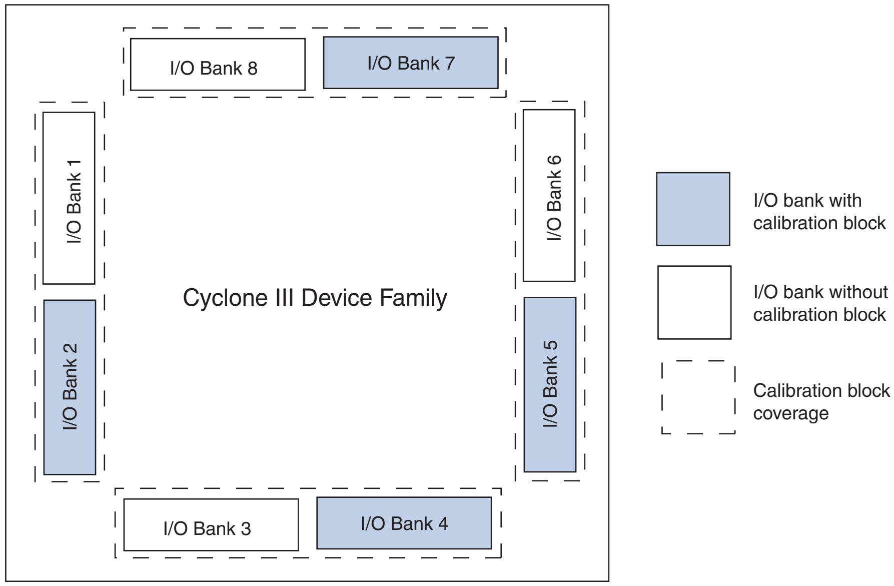
Figure 6–2. Cyclone III Device Family On-Chip Series Termination with Calibration



OCT with calibration is achieved using the OCT calibration block circuitry. There is one OCT calibration block in banks 2, 4, 5, and 7. Each calibration block supports each side of the I/O banks. Because there are two I/O banks sharing the same calibration block, both banks must have the same V_{CCIO} if both banks enable OCT calibration. If two related banks have different V_{CCIO}s, only the bank in which the calibration block resides can enable OCT calibration.

Figure 6–3 shows the top-level view of the OCT calibration blocks placement.

Figure 6–3. Cyclone III Device Family OCT Block Placement

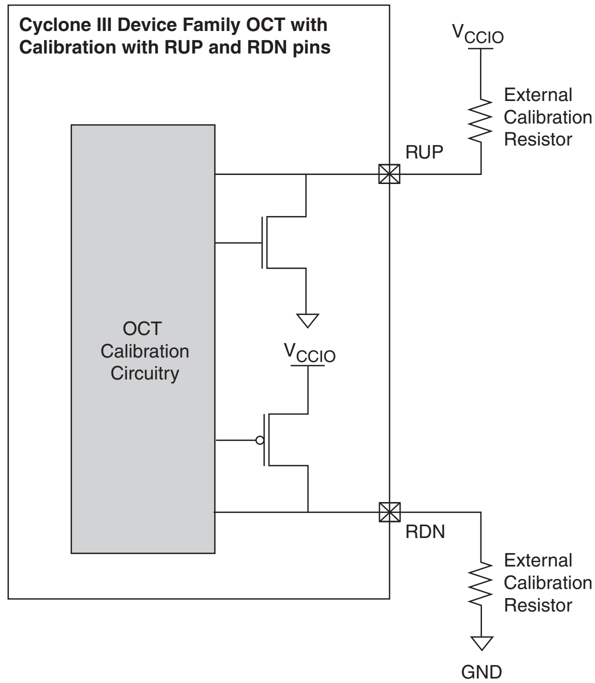


Each calibration block comes with a pair of RUP and RDN pins. When used for calibration, the RUP pin is connected to V_{CCIO} through an external 25-Ω ±1% or 50-Ω ±1% resistor for an on-chip series termination value of 25 Ω or 50 Ω, respectively. The RDN pin is connected to GND through an external 25-Ω ±1% or 50-Ω ±1% resistor for an on-chip series termination value of 25 Ω or 50 Ω, respectively. The external resistors are compared with the internal resistance using comparators. The resultant outputs of the comparators are used by the OCT calibration block to dynamically adjust buffer impedance.

During calibration, the resistance of the RUP and RDN pins varies. For an estimate of the maximum possible current through the external calibration resistors, assume a minimum resistance of 0 Ω on the RUP and RDN pins during calibration.

Figure 6–4 shows the external calibration resistors setup on the RUP and RDN pins and the associated OCT calibration circuitry.

Figure 6–4. Cyclone III Device Family On-Chip Series Termination with Calibration Setup



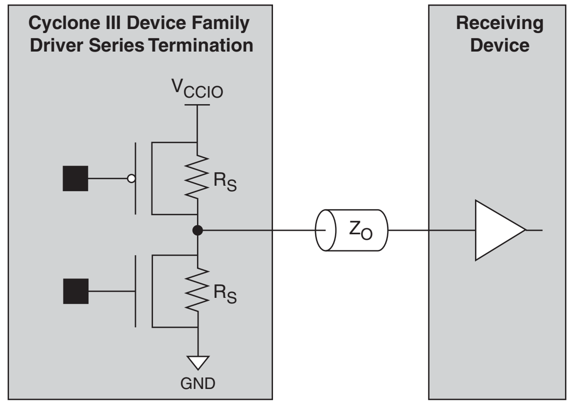
RUP and RDN pins go to a tri-state condition when calibration is completed or not running. These two pins are dual-purpose I/Os and function as regular I/Os if you do not use the calibration circuit.

On-Chip Series Termination Without Calibration

The Cyclone III device family supports driver impedance matching to the impedance of the transmission line, which is typically 25 Ω or 50 Ω. When used with the output drivers, OCT sets the output driver impedance to 25 Ω or 50 Ω. The Cyclone III device family also supports output driver series termination (R_S = 50 Ω) for **SSTL-2** and **SSTL-18**.

Figure 6–5 shows the single-ended I/O standards for OCT without calibration. The R_S shown is the intrinsic transistor impedance.

Figure 6–5. Cyclone III Device Family On-Chip Series Termination Without Calibration



All I/O banks and I/O pins support impedance matching and series termination. Dedicated configuration pins and JTAG pins do not support impedance matching or series termination.

On-chip series termination is supported on any I/O bank. V_{CCIO} and V_{REF} must be compatible for all I/O pins to enable on-chip series termination in a given I/O bank. I/O standards that support different R_S values can reside in the same I/O bank as long as their V_{CCIO} and V_{REF} are not conflicting.

Impedance matching is implemented using the capabilities of the output driver and is subject to a certain degree of variation, depending on the process, voltage, and temperature.

For more information about tolerance specification, refer to the *Cyclone III Device Data Sheet* and *Cyclone III LS Device Data Sheet* chapters.

I/O Standards

The Cyclone III device family supports multiple single-ended and differential I/O standards. Apart from 3.3-, 3.0-, 2.5-, 1.8-, and 1.5-V support, the Cyclone III device family also supports 1.2-V I/O standards.

Table 6–4 lists I/O standards supported by the Cyclone III device family and which I/O pins support them.

Table 6–4. Cyclone III Device Family Supported I/O Standards and Constraints (Part 1 of 2)

I/O Standard	Type	Standard Support	V_{CCIO} Level (in V)		Top and Bottom I/O Pins			Left and Right I/O Pins	
			Input	Output	CLK, DQS	PLL_OUT	User I/O Pins	CLK, DQS	User I/O Pins
3.3-V LVTTL, 3.3-V LVCMOS (1)	Single-ended	JESD8-B	3.3/3.0/2.5 (2)	3.3	✓	✓	✓	✓	✓
3.0-V LVTTL, 3.0-V LVCMOS (1)	Single-ended	JESD8-B	3.3/3.0/2.5 (2)	3.0	✓	✓	✓	✓	✓
2.5-V LVTTL / LVCMOS	Single-ended	JESD8-5	3.3/3.0/2.5 (2)	2.5	✓	✓	✓	✓	✓
1.8-V LVTTL / LVCMOS	Single-ended	JESD8-7	1.8/1.5 (2)	1.8	✓	✓	✓	✓	✓
1.5-V LVCMOS	Single-ended	JESD8-11	1.8/1.5 (2)	1.5	✓	✓	✓	✓	✓
1.2-V LVCMOS	Single-ended	JESD8-12A	1.2	1.2	✓	✓	✓	✓	✓
SSTL-2 Class I, SSTL-2 Class II	Voltage referenced	JESD8-9A	2.5	2.5	✓	✓	✓	✓	✓
SSTL-18 Class I, SSTL-18 Class II	Voltage referenced	JESD815	1.8	1.8	✓	✓	✓	✓	✓
HSTL-18 Class I, HSTL-18 Class II	Voltage referenced	JESD8-6	1.8	1.8	✓	✓	✓	✓	✓
HSTL-15 Class I, HSTL-15 Class II	Voltage referenced	JESD8-6	1.5	1.5	✓	✓	✓	✓	✓
HSTL-12 Class I	Voltage referenced	JESD8-16A	1.2	1.2	✓	✓	✓	✓	✓
HSTL-12 Class II (7)	Voltage referenced	JESD8-16A	1.2	1.2	✓	✓	✓	—	—
PCI and PCI-X	Single-ended	—	3.0	3.0	✓	✓	✓	✓	✓
Differential SSTL-2 Class I or Class II	Differential (3)	JESD8-9A	—	2.5	—	✓	—	—	—
			2.5	—	✓	—	—	✓	—
Differential SSTL-18 Class I or Class II	Differential (3)	JESD815	—	1.8	—	✓	—	—	—
			1.8	—	✓	—	—	✓	—
Differential HSTL-18 Class I or Class II	Differential (3)	JESD8-6	—	1.8	—	✓	—	—	—
			1.8	—	✓	—	—	✓	—
Differential HSTL-15 Class I or Class II	Differential (3)	JESD8-6	—	1.5	—	✓	—	—	—
			1.5	—	✓	—	—	✓	—
Differential HSTL-12 Class I or Class II	Differential (3)	JESD8-16A	—	1.2	—	✓	—	—	—
			1.2	—	✓	—	—	✓	—
PPDS (4)	Differential	—	—	2.5	—	✓	✓	—	✓

Table 6–4. Cyclone III Device Family Supported I/O Standards and Constraints (Part 2 of 2)

I/O Standard	Type	Standard Support	V_{CCIO} Level (in V)		Top and Bottom I/O Pins			Left and Right I/O Pins	
			Input	Output	CLK, DQS	PLL_OUT	User I/O Pins	CLK, DQS	User I/O Pins
LVDS (8)	Differential	—	2.5	2.5	✓	✓	✓	✓	✓
RSDS and **mini-LVDS** (4)	Differential	—	—	2.5	—	✓	✓	—	✓
BLVDS (6)	Differential	—	2.5	2.5	—	—	✓	—	✓
LVPECL (5)	Differential	—	2.5	—	✓	—	—	✓	—

Notes to Table 6–4:

(1) The PCI-clamp diode must be enabled for **3.3-V/3.0-V LVTTL/LVCMOS**.

(2) The Cyclone III architecture supports the MultiVolt I/O interface feature that allows Cyclone III devices to interface with I/O systems that have different supply voltages.

(3) **Differential HSTL** and **SSTL** outputs use two single-ended outputs with the second output programmed as inverted. **Differential HSTL** and **SSTL** inputs treat differential inputs as two single-ended **HSTL** and **SSTL** inputs and only decode one of them. **Differential HSTL** and **SSTL** are only supported on `CLK` pins.

(4) **PPDS**, **mini-LVDS**, and **RSDS** are only supported on output pins.

(5) **LVPECL** is only supported on clock inputs.

(6) Bus LVDS (**BLVDS**) output uses two single-ended outputs with the second output programmed as inverted. **BLVDS** input uses **LVDS** input buffer.

(7) Class I and Class II refer to output termination and do not apply to input. **1.2-V HSTL** input is supported at both column and row I/O regardless of class.

(8) True differential **LVDS**, **RSDS**, and **mini-LVDS** I/O standards are supported in left and right I/O pins while emulated differential **LVDS** (**LVDS_E_3R**), **RSDS** (**RSDS_E_3R**), and **mini-LVDS** (**LVDS_E_3R**) I/O standards are supported in both left and right, and top and bottom I/O pins.

The Cyclone III device family supports **PCI** and **PCI-X** I/O standards at 3.0-V V_{CCIO}. The 3.0-V PCI and PCI-X I/O are fully compatible for direct interfacing with 3.3-V PCI systems without requiring any additional components. The 3.0-V PCI and PCI-X outputs meet the V_{IH} and V_{IL} requirements of 3.3-V PCI and PCI-X inputs with sufficient noise margin.

For more information about the **3.3/3.0/2.5-V LVTTL** and **LVCMOS** multivolt I/O support, refer to *AN 447: Interfacing Cyclone III and Cyclone IV Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems*.

Termination Scheme for I/O Standards

This section describes recommended termination schemes for voltage-referenced and differential I/O standards.

The **3.3-V LVTTL**, **3.0-V LVTTL** and **LVCMOS**, **2.5-V LVTTL** and **LVCMOS**, **1.8-V LVTTL** and **LVCMOS**, **1.5-V LVCMOS**, **1.2-V LVCMOS**, **3.0-V PCI**, and **PCI-X** I/O standards do not specify a recommended termination scheme per the JEDEC standard.

Voltage-Referenced I/O Standard Termination

Voltage-referenced I/O standards require an input reference voltage (V_{REF}) and a termination voltage (V_{TT}). The reference voltage of the receiving device tracks the termination voltage of the transmitting device, as shown in Figure 6–6 and Figure 6–7.

Figure 6–6. Cyclone III Device Family HSTL I/O Standard Termination

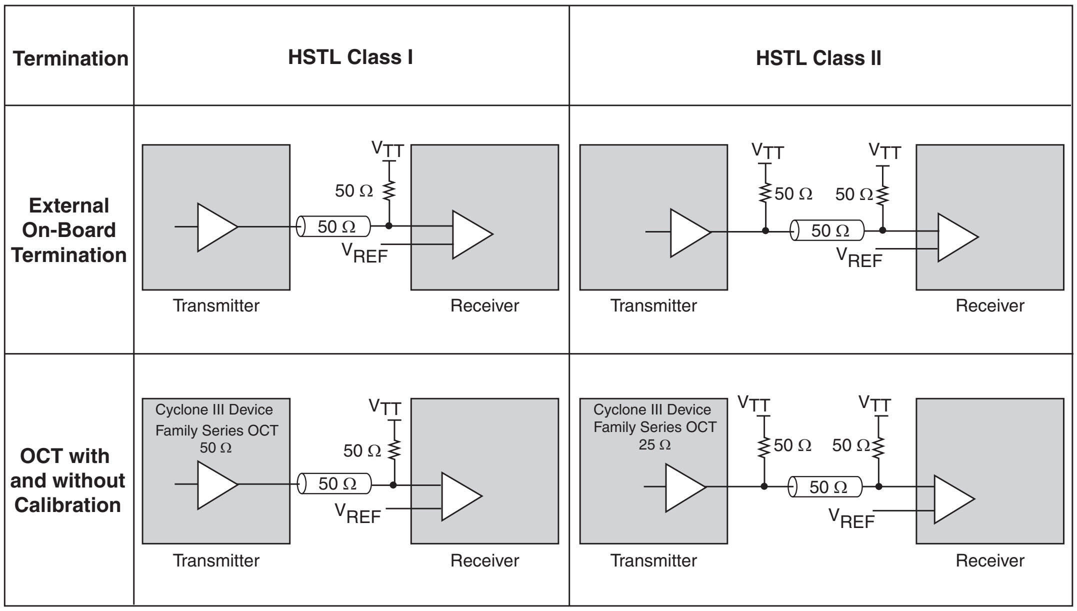
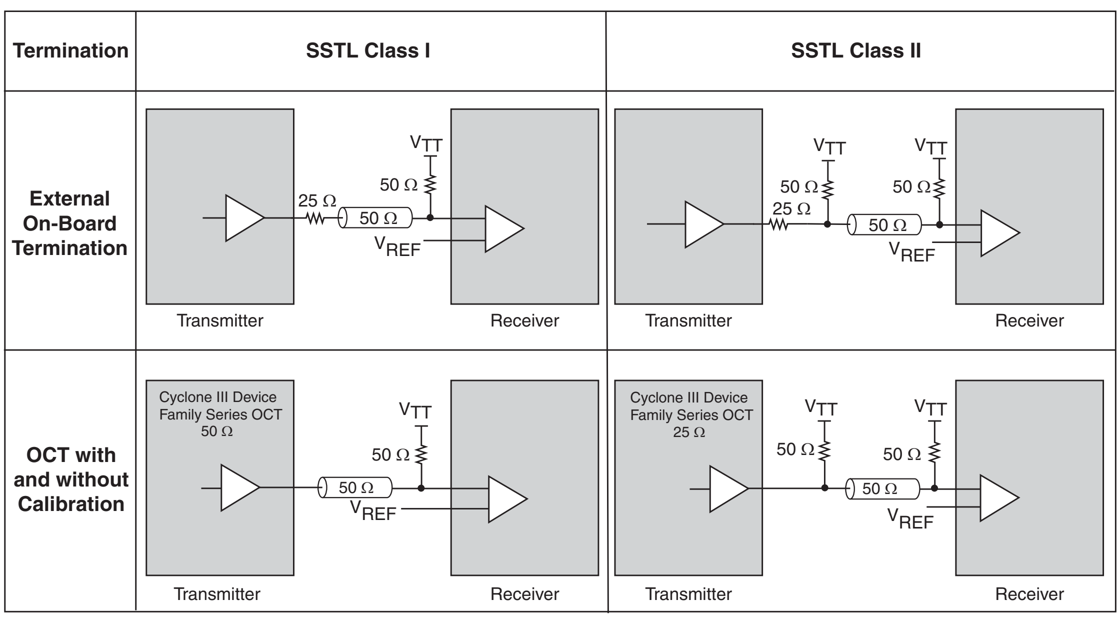


Figure 6–7. Cyclone III Device Family SSTL I/O Standard Termination



Differential I/O Standard Termination

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the bus (Figure 6–8 and Figure 6–9).

The Cyclone III device family supports **differential SSTL-2** and **SSTL-18**, **differential HSTL-18**, **HSTL-15**, and **HSTL-12**, **PPDS**, **LVDS**, **RSDS**, **mini-LVDS**, and **differential LVPECL**.

Figure 6–8. Cyclone III Device Family Differential HSTL I/O Standard Termination

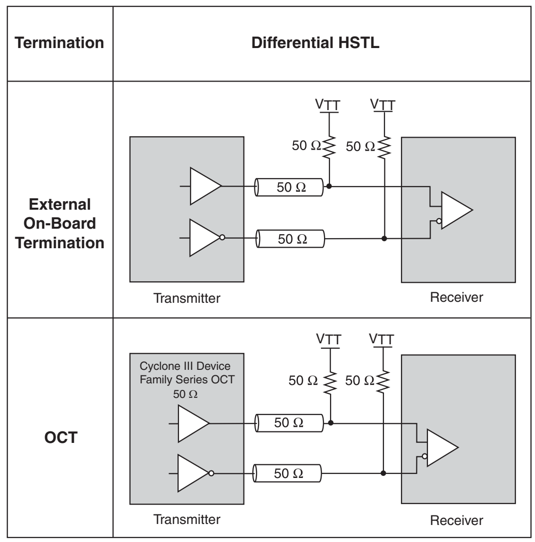
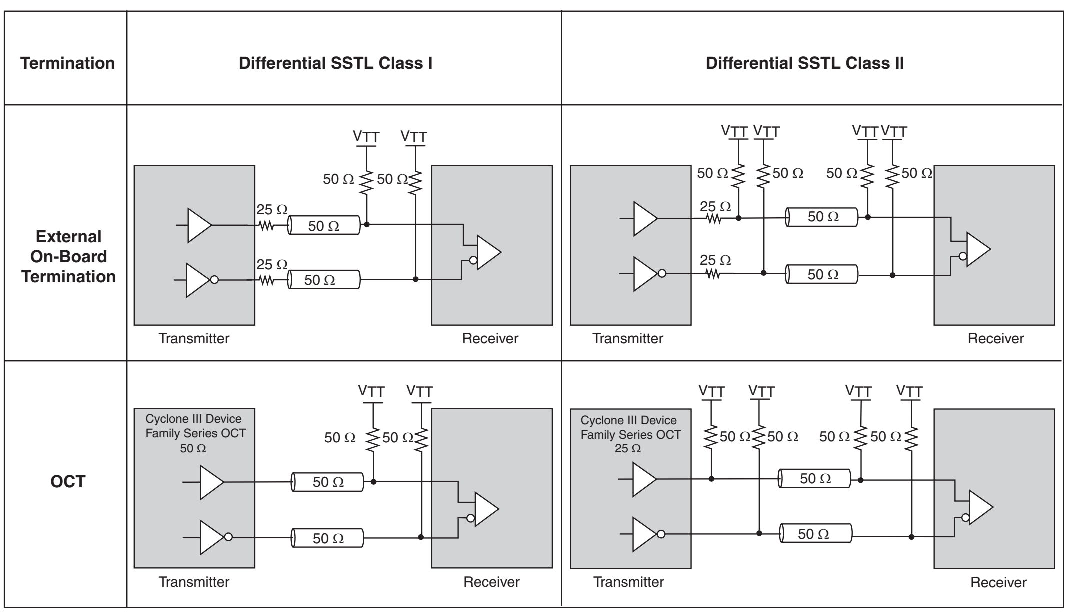


Figure 6–9. Cyclone III Device Family Differential SSTL I/O Standard Termination *(1)*



Note to Figure 6–9:

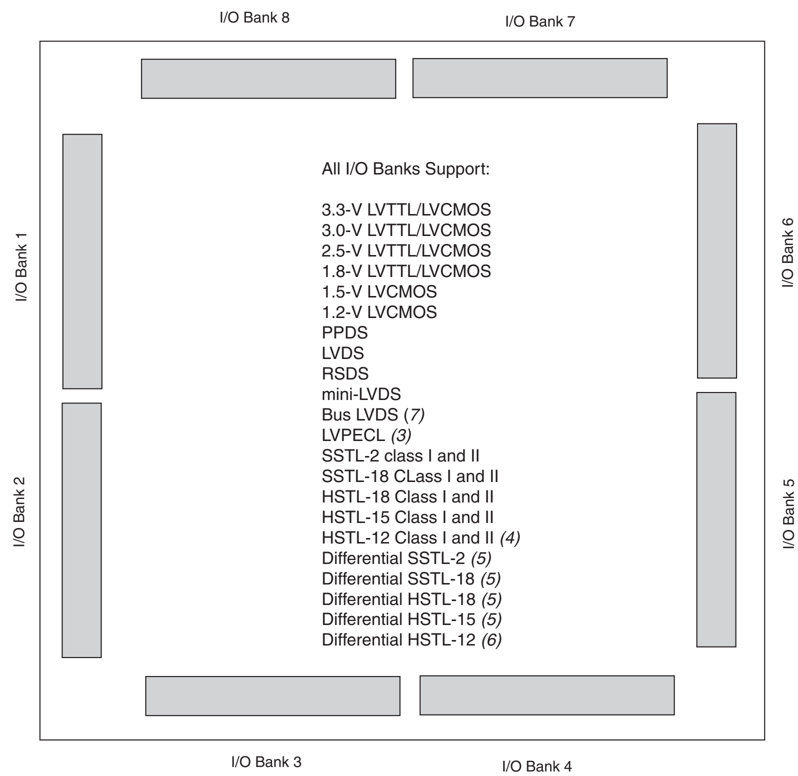
(1) Only Differential SSTL-2 I/O standard supports Class II output.

For information about the Cyclone III device family **differential PPDS**, **LVDS**, **mini LVDS**, **RSDS** I/O, and Bus LVDS (**BLVDS**) standard termination, refer to the *High-Speed Differential Interfaces in the Cyclone III Device Family* chapter.

I/O Banks

I/O pins on the Cyclone III device family are grouped together into I/O banks, and each bank has a separate power bus. Cyclone III and Cyclone III LS devices have eight I/O banks, as shown in Figure 6–10. Each device I/O pin is associated with one I/O bank. All single-ended I/O standards are supported in all banks except **HSTL-12 Class II**, which is only supported in column I/O banks. All differential I/O standards are supported in all banks. The only exception is **HSTL-12 Class II**, which is only supported in column I/O banks.

Figure 6–10. Cyclone III Device Family I/O Banks *(1)*, *(2)*



Notes to Figure 6–10:

(1) This is a top view of the silicon die. This is only a graphical representation. For exact pin locations, refer to the pin list and the Quartus II software.
(2) True differential (**PPDS**, **LVDS**, **mini-LVDS**, and **RSDS** I/O standards) outputs are supported in row I/O banks 1, 2, 5, and 6 only. External resistors are needed for the differential outputs in column I/O banks.
(3) The **LVPECL** I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.
(4) The **HSTL-12 Class II** is supported in column I/O banks 3, 4, 7, and 8 only.
(5) The **differential SSTL-18** and **SSTL-2**, **differential HSTL-18**, and **HSTL-15** I/O standards are supported only on clock input pins and phase-locked loops (PLLs) output clock pins. **Differential SSTL-18**, **differential HSTL-18**, and **HSTL-15** I/O standards do not support Class II output.
(6) The **differential HSTL-12** I/O standard is only supported on clock input pins and PLL output clock pins. **Differential HSTL-12 Class II** is supported only in column I/O banks 3, 4, 7, and 8.
(7) **BLVDS** output uses two single-ended outputs with the second output programmed as inverted. **BLVDS** input uses the **LVDS** input buffer.

Table 6–5 lists the I/O standards supported when a pin is used as a regular I/O pin in the I/O banks of the Cyclone III device family.

Table 6–5. Cyclone III Device Family I/O Standards Support

I/O Standard	I/O Banks							
	1	2	3	4	5	6	7	8
3.3-V LVTTL/LVCMOS, **3.0-V LVTTL/LVCMOS**, **2.5-V LVTTL/LVCMOS**, **1.8-V LVTTL/LVCMOS**, **1.5-V LVCMOS**, **1.2V LVCMOS**, **3.0-V PCI/PCI-X**	✓	✓	✓	✓	✓	✓	✓	✓
SSTL-18 Class I/II, **SSTL-2 Class I/II**, **HSTL-18 Class I/II**, **HSTL-15 Class I/II**, **HSTL-12 Class I**	✓	✓	✓	✓	✓	✓	✓	✓
HSTL-12 Class II	—	—	✓	✓	—	—	✓	✓
Differential SSTL-2, **Differential SSTL-18**, **Differential HSTL-18**, **Differential HSTL-15**, **Differential HSTL-12**	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*	*(1)*
PPDS *(2), (3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*
LVDS *(2)*	✓	✓	✓	✓	✓	✓	✓	✓
BLVDS	✓	✓	✓	✓	✓	✓	✓	✓
RSDS and **mini-LVDS** *(2)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*	*(3)*
Differential LVPECL	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*

Notes to Table 6–5:

(1) These differential I/O standards are supported only for clock inputs and dedicated `PLL_OUT` outputs.

(2) True differential (**PPDS**, **LVDS**, **mini-LVDS**, and **RSDS** I/O standards) outputs are supported in row I/O banks only. Differential outputs in column I/O banks require an external resistors network.

(3) This I/O standard is supported for outputs only.

(4) This I/O standard is supported for clock inputs only.

Each I/O bank of the Cyclone III device family has a VREF bus to accommodate voltage-referenced I/O standards. Each `VREF` pin is the reference source for its V_{REF} group. If you use a V_{REF} group for voltage-referenced I/O standards, connect the `VREF` pin for that group to the appropriate voltage level. If you do not use all the V_{REF} groups in the I/O bank for voltage referenced I/O standards, you can use the `VREF` pin in the unused voltage referenced groups as regular I/O pins. For example, if you have **SSTL-2 Class I** input pins in I/O bank 1 and they are all placed in the `VREFB1N0` group, `VREFB1N0` must be powered with 1.25 V, and the remaining `VREFB1N[1:3]` pins (if available) are used as I/O pins. If multiple V_{REF} groups are used in the same I/O bank, the `VREF` pins must all be powered by the same voltage level because the `VREF` pins are shorted together within the same I/O bank.

When VREF pins are used as regular I/Os, they have higher pin capacitance than regular user I/O pins. This has an impact on the timing if the pins are used as inputs and outputs.

For more information about VREF pin capacitance, refer to the pin capacitance section in the *Cyclone III Device Data Sheet* and *Cyclone III LS Device Data Sheet* chapters.

For more information about how to identify V_{REF} groups, refer to the **Cyclone III Device Family Pin-Out** files or the **Quartus II Pin Planner** tool.

Table 6–6 lists the number of VREF pins in each I/O bank for Cyclone III and Cyclone III LS devices.

Table 6–6. Number of VREF Pins Per I/O Banks for Cyclone III and Cyclone III LS Devices (Part 1 of 2)

Family	Device	Package	Pin Count	I/O Banks							
				1	2	3	4	5	6	7	8
Cyclone III	EP3C5	EQFP	144	1	1	1	1	1	1	1	1
		MBGA	164	1	1	1	1	1	1	1	1
		FBGA	256	1	1	1	1	1	1	1	1
	EP3C10	EQFP	144	1	1	1	1	1	1	1	1
		MBGA	164	1	1	1	1	1	1	1	1
		FBGA	256	1	1	1	1	1	1	1	1
	EP3C16	EQFP	144	2	2	2	2	2	2	2	2
		MBGA	164	2	2	2	2	2	2	2	2
		PQFP	240	2	2	2	2	2	2	2	2
		FBGA	256	2	2	2	2	2	2	2	2
		FBGA	484	2	2	2	2	2	2	2	2
	EP3C25	EQFP	144	1	1	1	1	1	1	1	1
		PQFP	240	1	1	1	1	1	1	1	1
		FBGA	256	1	1	1	1	1	1	1	1
		FBGA	324	1	1	1	1	1	1	1	1
	EP3C40	PQFP	240	4	4	4	4	4	4	4	4
		FBGA	324	4	4	4	4	4	4	4	4
		FBGA	484	4	4	4	4	4	4	4	4
		FBGA	780	4	4	4	4	4	4	4	4
	EP3C55	FBGA	484	2	2	2	2	2	2	2	2
		FBGA	780	2	2	2	2	2	2	2	2
	EP3C80	FBGA	484	3	3	3	3	3	3	3	3
		FBGA	780	3	3	3	3	3	3	3	3
	EP3C120	FBGA	484	3	3	3	3	3	3	3	3
		FBGA	780	3	3	3	3	3	3	3	3

Table 6–6. Number of VREF Pins Per I/O Banks for Cyclone III and Cyclone III LS Devices (Part 2 of 2)

Family	Device	Package	Pin Count	I/O Banks							
				1	2	3	4	5	6	7	8
Cyclone III LS	EP3CLS70	UBGA	278	3	3	3	3	3	3	3	3
		FBGA	278	3	3	3	3	3	3	3	3
		FBGA	413	3	3	3	3	3	3	3	3
	EP3CLS100	UBGA	278	3	3	3	3	3	3	3	3
		FBGA	278	3	3	3	3	3	3	3	3
		FBGA	413	3	3	3	3	3	3	3	3
	EP3CLS150	FBGA	210	3	3	3	3	3	3	3	3
		FBGA	413	3	3	3	3	3	3	3	3
	EP3CLS200	FBGA	210	3	3	3	3	3	3	3	3
		FBGA	413	3	3	3	3	3	3	3	3

Each I/O bank of the Cyclone III device family has its own `VCCIO` pins. Each I/O bank can support only one V_{CCIO} setting from among 1.2, 1.5, 1.8, 3.0, or 3.3 V. Any number of supported single-ended or differential standards can be simultaneously supported in a single I/O bank, as long as they use the same V_{CCIO} levels for input and output pins.

When designing **LVTTL/LVCMOS** inputs with Cyclone III and Cyclone III LS devices, refer to the following guidelines:

- All pins accept input voltage (V_I) up to a maximum limit (3.6 V), as stated in the recommended operating conditions are provided in the *Cyclone III Device Data Sheet* and *Cyclone III LS Device Data Sheet* chapters.
- Whenever the input level is higher than the bank V_{CCIO}, expect higher leakage current.
- The **LVTTL/LVCMOS** I/O standard input pins can only meet the V_{IH} and V_{IL} levels according to bank voltage level.

Voltage-referenced standards are supported in an I/O bank using any number of single-ended or differential standards, as long as they use the same V_{REF} and V_{CCIO} values. For example, if you choose to implement both **SSTL-2** and **SSTL-18** in your Cyclone III and Cyclone III LS devices, I/O pins using these standards—because they require different V_{REF} values—must be in different banks from each other. However, the same I/O bank can support **SSTL-2** and **2.5-V LVCMOS** with the V_{CCIO} set to 2.5 V and the V_{REF} set to 1.25 V.

When using Cyclone III and Cyclone III LS devices as a receiver in 3.3-, 3.0-, or 2.5-V **LVTTL/LVCMOS** systems, you are responsible for managing overshoot or undershoot to stay in the absolute maximum ratings and the recommended operating conditions, provided in the *Cyclone III Device Data Sheet* and *Cyclone III LS Device Data Sheet* chapters.

The PCI clamping diode is enabled by default in the Quartus II software for input signals with bank V_{CCIO} at 2.5, 3.0, or 3.3 V.

For more information about the Cyclone III device family I/O interface with 3.3-, 3.0-, or 2.5-V **LVTTL**/**LVCMOS** systems, refer to *AN 447: Interfacing Cyclone III and Cyclone IV Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems*.

High-Speed Differential Interfaces

The Cyclone III device family can send and receive data through **LVDS** signals. For the **LVDS** transmitter and receiver, the input and output pins of the Cyclone III device family support serialization and deserialization through internal logic.

The **BLVDS** extends the benefits of **LVDS** to multipoint applications such as in bidirectional backplanes. The loading effect and the need to terminate the bus at both ends for multipoint applications require **BLVDS** to drive out a higher current than **LVDS** to produce a comparable voltage swing. All the I/O banks of the Cyclone III device family support **BLVDS** for user I/O pins.

The reduced swing differential signaling (**RSDS**) and **mini-LVDS** standards are derivatives of the **LVDS** standard. The **RSDS** and **mini-LVDS** I/O standards are similar in electrical characteristics to **LVDS**, but have a smaller voltage swing and therefore provide increased power benefits and reduced electromagnetic interference (EMI).

The point-to-point differential signaling (**PPDS**) standard is the next generation of the **RSDS** standard introduced by National Semiconductor Corporation. The Cyclone III device family meets the National Semiconductor Corporation PPDS Interface Specification and supports the **PPDS** standard for outputs only. All the I/O banks of the Cyclone III device family support the **PPDS** standard for output pins only.

You can use I/O pins and internal logic to implement the **LVDS** I/O receiver and transmitter in the Cyclone III device family. Cyclone III and Cyclone III LS devices do not contain dedicated serialization or deserialization circuitry. Therefore, shift registers, internal PLLs, and IOEs are used to perform serial-to-parallel conversions on incoming data and parallel-to-serial conversion on outgoing data.

The **LVDS** standard does not require an input reference voltage, but it does require a 100-Ω termination resistor between the two signals at the input buffer. An external resistor network is required on the transmitter side for top and bottom I/O banks.

For more information about the Cyclone III device family high-speed differential interface support, refer to the *High-Speed Differential Interfaces in the Cyclone III Device Family* chapter.

External Memory Interfacing

The Cyclone III device family supports I/O standards required to interface with a broad range of external memory interfaces, such as DDR SDRAM, DDR2 SDRAM, and QDRII SRAM.

For more information about the Cyclone III device family external memory interface support, refer to the *External Memory Interfaces in the Cyclone III Device Family* chapter.

Pad Placement and DC Guidelines

Pad Placement

Altera recommends that you create a Quartus II design, enter your device I/O assignments, and compile your design to validate your pin placement. The Quartus II software checks your pin connections with respect to the I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this chapter.

For more information about how the Quartus II software checks I/O restrictions, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

DC Guidelines

For the Quartus II software to automatically check for illegally placed pads according to the DC guidelines, set the DC current sink or source value to **Electromigration Current** assignment on each of the output pins that are connected to the external resistive load.

The programmable current strength setting has an impact on the amount of DC current that an output pin can source or sink. Determine if the current strength setting is sufficient for the external resistive load condition on the output pin.

Document Revision History

Table 6–7 lists the revision history for this document.

Table 6–7. Document Revision History (Part 1 of 3)

Date	Version	Changes
July 2012	3.4	Updated OCT with or without calibration note in "Slew Rate Control" section,
December 2011	3.3	■ Updated Table 6–1 and Table 6–4. ■ Updated "Programmable Pull-Up Resistor" on page 6–5, "OCT Support" on page 6–7, and "I/O Standards" on page 6–11. ■ Updated hyperlinks. ■ Minor text edits.
December 2009	3.2	Minor changes to the text.
July 2009	3.1	Made minor correction to the part number.
June 2009	3.0	Updated to include Cyclone III LS information ■ Updated chapter part number. ■ Updated "Introduction" on page 6–1, "PCI-Clamp Diode" on page 6–6, "On-Chip Series Termination Without Calibration" on page 6–10, "I/O Standards" on page 6–11, "I/O Banks" on page 6–16, "High-Speed Differential Interfaces" on page 6–20, and "External Memory Interfacing" on page 6–20. ■ Updated Table 6–6 on page 6–18.

Table 6–7. Document Revision History (Part 2 of 3)

Date	Version	Changes
October 2008	2.1	■ Added *(Note 6)* to Table 6–5. ■ Updated the “I/O Banks” section. ■ Updated the “Differential Pad Placement Guidelines” section. ■ Updated the “VREF Pad Placement Guidelines” section. ■ Removed any mention of “RSDS and PPDS are registered trademarks of National Semiconductor” from chapter. ■ Updated chapter to new template.
May 2008	2.0	Changes include addition of BLVDS information. ■ Added an introduction to “I/O Element Features” section. ■ Updated “Slew Rate Control” section. ■ Updated “Programmable Delay” section. ■ Updated Table 6–1 with BLVDS information. ■ Updated Table 6–2. ■ Updated “PCI-Clamp Diode” section. ■ Updated “LVDS Transmitter Programmable Pre-Emphasis” section. ■ Updated “On-Chip Termination with Calibration” section and added new Figure 6–9. ■ Updated Table 6–3 title. ■ Updated Table 6–4 unit. ■ Updated “I/O Standards” section and Table 6–5 with BLVDS information and added *(Note 5)*. ■ Updated “Differential I/O Standard Termination” section with BLVDS information. ■ Updated “I/O Banks” section. ■ Updated *(Note 2)* and added *(Note 7)* and BLVDS information to Figure 6–15. ■ Updated *(Note 2)* and added BLVDS information to Table 6–6. ■ Added MBGA package information to Table 6–7. ■ Deleted Table 6-8. ■ Updated “High-Speed Differential Interfaces” section with BLVDS information. ■ Updated “Differential Pad Placement Guidelines” section and added new Figure 6–16. ■ Updated “VREF Pad Placement Guidelines” section and added new Figure 6–17. ■ Updated Table 6–11. ■ Added new “DCLK Pad Placement Guidelines” section. ■ Updated “DC Guidelines” section.

Table 6–7. Document Revision History (Part 3 of 3)

Date	Version	Changes
July 2007	1.1	■ Updated feetpara note in “Programmable Current Strength” section. ■ Updated feetpara note in “Slew Rate Control” section. ■ Updated feetpara note in “Open-Drain Output” section. ■ Updated feetpara note in “Bus Hold” section. ■ Updated feetpara note in “Programmable Pull-Up Resistor” section. ■ Updated feetpara note in “PCI-Clamp Diode” section. ■ Updated Figure 6–13. ■ Updated Figure 6–14 and added Note (1). ■ Updated “I/O Banks” section. ■ Updated Note (5) to Figure 6–15. ■ Updated “DDR/DDR2 and QDRII Pads” section and corrected ‘cms’ to ‘cmd’. ■ Updated Note 3 in Table 6-8. ■ Added chapter TOC and “Referenced Documents” section.
March 2007	1.0	Initial release.