Digital System Design Capsule 2024 Spring PROJECT 1

Uneven Seven-Sided Dice Roller | Task 2: Full adder

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This report delves deep into the interesting functionality of a Fuller Adder, a critical component pivotal in digital arithmetic operations. Within the scope of our project, the Fuller Adder assumes a central role, offering robustness and versatility essential for computational tasks, particularly in the context of our uneven seven-sided dice roller.

The Fuller Adder stands as a cornerstone in digital electronics, embodying the essence of binary addition with enhanced capabilities beyond its predecessor, the Half Adder. Unlike the Half Adder, which handles two inputs, the Fuller Adder adeptly processes three binary inputs – A, B, and a carry-in (Cin), enabling seamless integration of carry bits from preceding stages. Its architecture is reminiscent of a cascading chain of logic gates, orchestrated to perform the addition operation efficiently.

At the heart of the Fuller Adder lies a sophisticated interplay of logic gates, primarily XOR (Exclusive OR), AND, and OR gates. These gates, intricately interconnected, facilitate the computation of sum (S) and carry-out (Cout) outputs based on the input combinations. The XOR gate calculates the sum output, ensuring that it reflects the addition modulo 2 of the input bits. Meanwhile, the AND gate determines the carry-out, signalling whether there's a carry-over to the next higher bit position.

However, what distinguishes the Fuller Adder is its ability to accommodate the carry-in bit, a feature indispensable for cascading multiple adders in larger arithmetic circuits. This carry-in input augments the circuit's functionality, enabling it to handle carry propagation seamlessly, thereby ensuring accurate and efficient arithmetic computation.

Furthermore, the Fuller Adder's robustness extends to its implementation using MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) technology, where PMOS (P-channel MOSFET) and NMOS (N-channel MOSFET) transistors are strategically integrated. This integration ensures optimal performance and reliability, crucial for its application in digital systems.

→ Circuit diagrams:

Circuit design for OR gate: using the Circuit design for NOR gate we made a OR gate by adding an inverter as seen in the diagram.

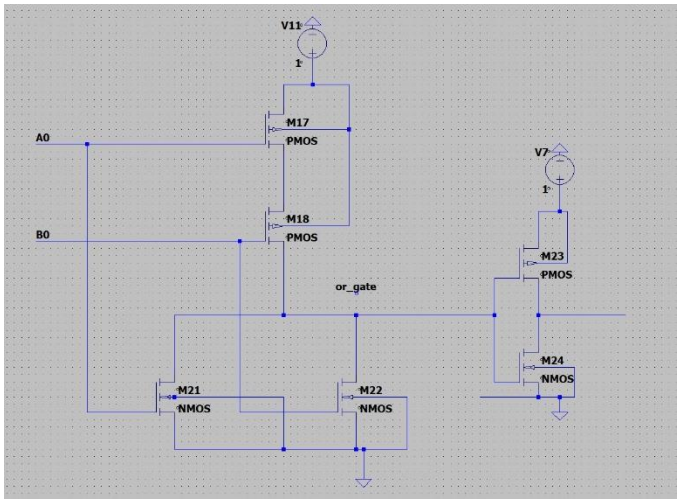


Figure 1.0.

Circuit design for XOR gate:

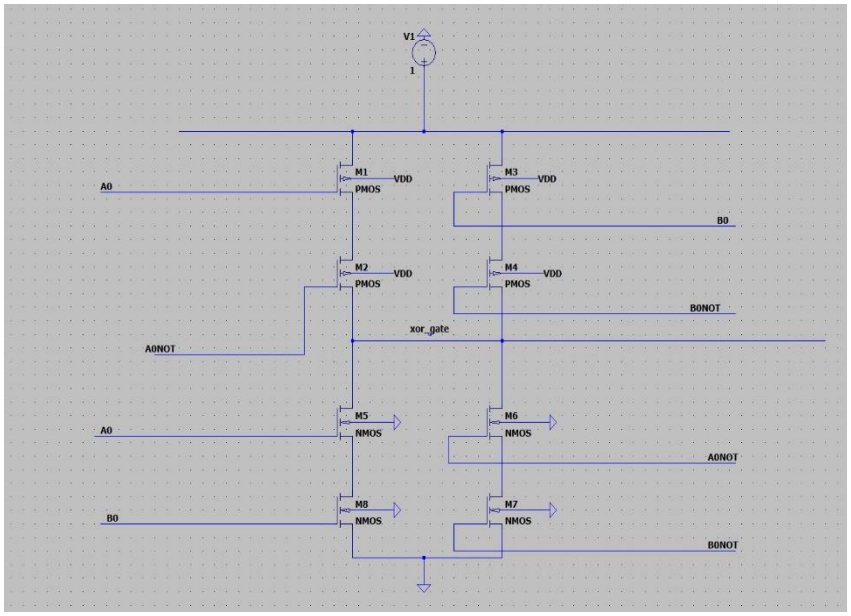


Figure 1.2.

Circuit design for AND gate: using the Circuit design for NAND gate we made a AND gate by adding an inverter as seen in the diagram.

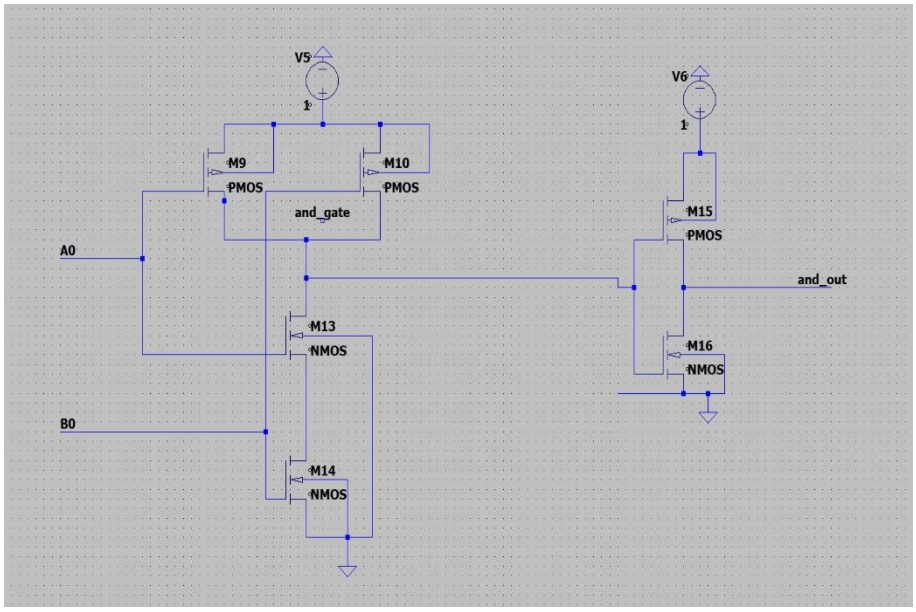


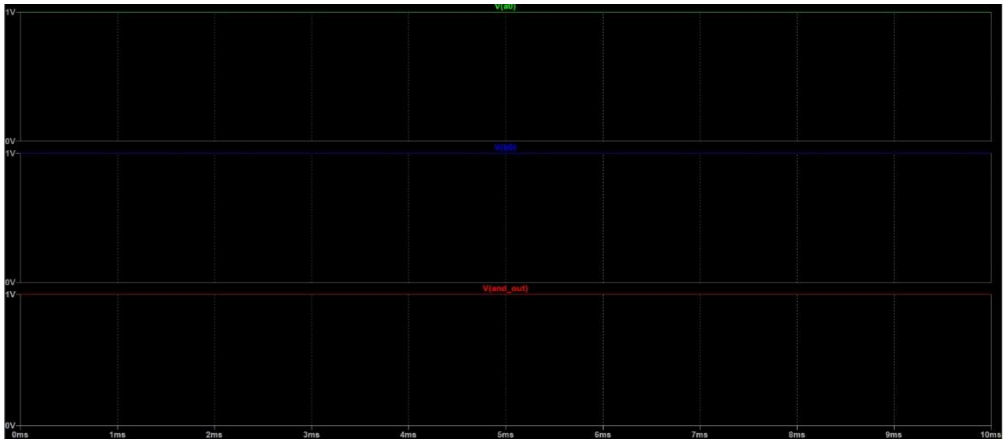
Figure 1.3.

→ Simulation results

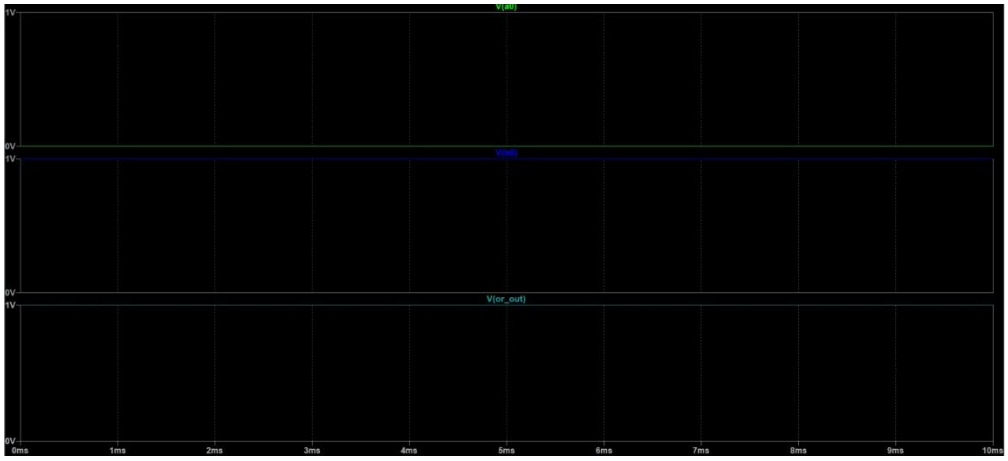
The truth table for the system:

A1	A0	B1	B0	S1	S2	CARRY
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	1	0	1	0	1
1	1	1	1	1	1	0

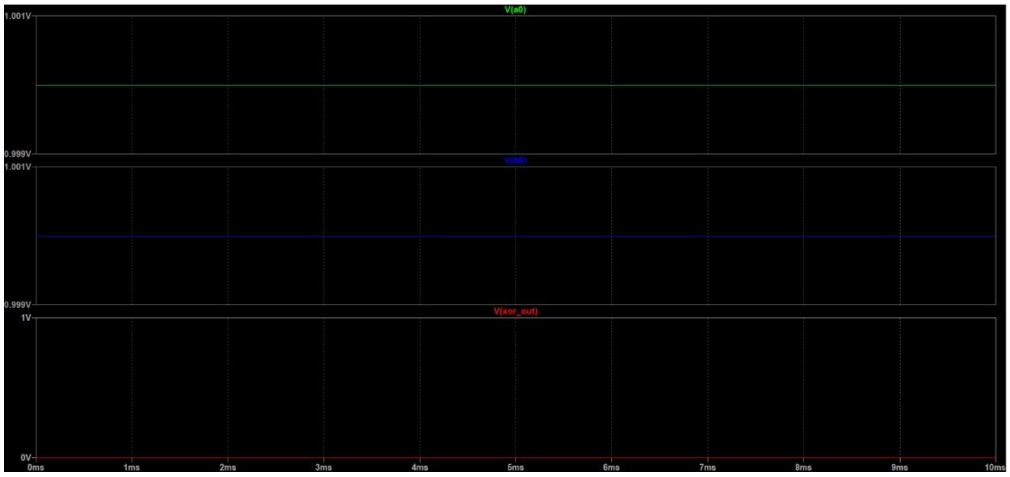
Simulation result for AND gate:



Simulation result for OR gate:

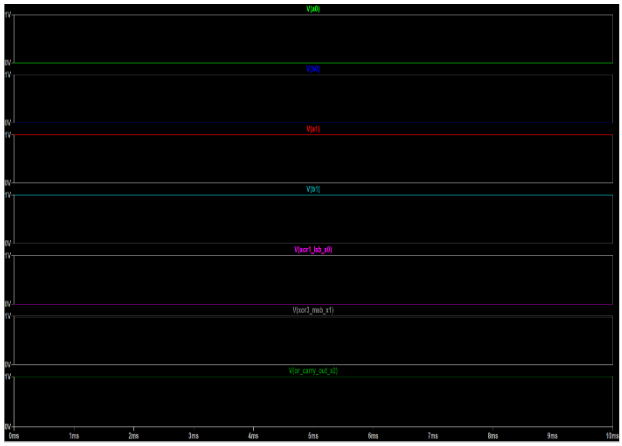


Simulation result for XOR gate:

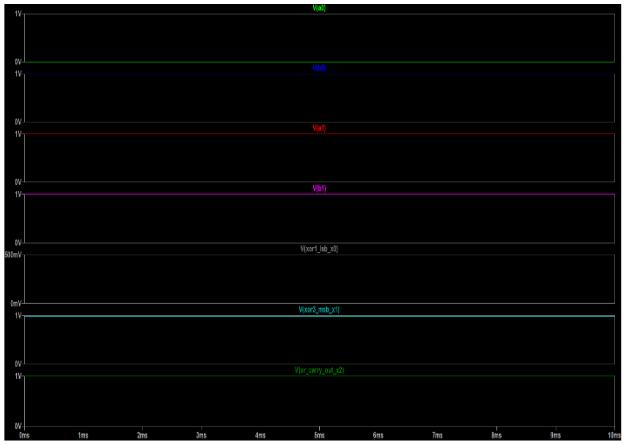


Simulation for 2-bit full adder:

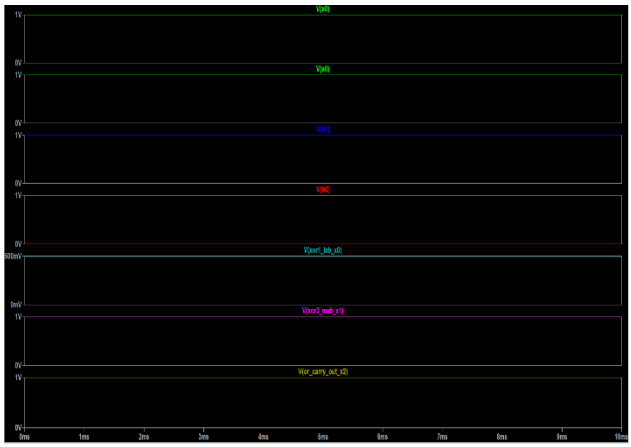
1010



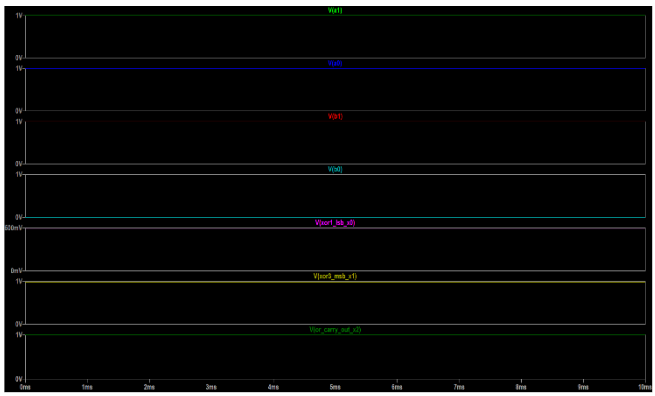
1011


V(a0)
V(b0)
V(a1)
V(b1)
V(xor1_lsb_x0)
V(xor3_msb_x1)
V(or_carry_out_x2)

1110


V(a0)
V(b0)
V(a1)
V(b1)
V(xor1_lsb_x0)
V(xor3_msb_x1)
V(or_carry_out_x2)

1111


V(a1)
V(a0)
V(b1)
V(b0)
V(xor1_lsb_x0)
V(xor3_msb_x1)
V(or_carry_out_x2)