DSD CAPSULE PROJECT REPORT

ABDULLAH RIHAWI
Electrical and Electronics Engineering
Abdullah Gul University
Turkey, Kayseri
abdullah.rihawi@agu.edu.tr

HUSEIN MOHAMED FAARAH
Electrical and Electronics Engineering
Abdullah Gul University
Turkey, Kayseri
husein.faarah@agu.edu.tr

***Abstract*:**

This report explains the Uneven-Seven-Sided Dice Roller that Abdullah and Husein made for the DSD Capsule of the Electrical and Electronics Engineering Department. In this project, we implemented our electronics and digital design knowledge to prepare this design. In the report, we are going to present our development for this project by showcasing each step and its functionality for the Uneven-Seven-Sided Dice Roller.

INTRODUCTION

The dice roller is used in games usually having 6 sides numbered from 1 to 6. However, in certain games or educational activities, a dice with an uneven number of sides can be more suitable. Unlike the traditional dice, the seven-sided dice roller has seven possible outputs which have differing probabilities of occurring. In this project, we design a 7-sided dice roller and scrutinize its functionality using the basics of electronics and digital design.

Description of the Entire system

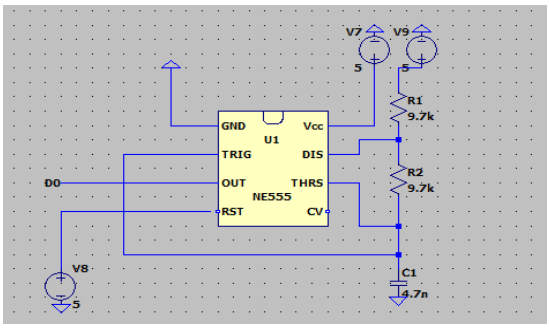
In this section, we are going to mention and scrutinize the different parts and circuits of this system. The system is designed with sequential circuits. Starting from generating initial data until acquiring the random 3-bit outputs. These binary outputs will be converted into decimals to get the randomness between 1 and 7.

The circuits used in the system.

- 1-bit Data Generator (Timer).
- Clock1
- Intermediate Register (R1)
- 2-bit full adder
- Clock4
- Output Register (R0)

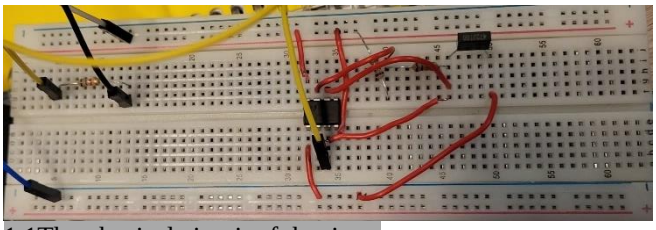
1-bit Data Generator (Timer):

For this circuit, in the first demonstration where we had to explain the 1-bit data generator we made a 7th-order ring oscillator that had a square wave frequency of ≈ 5500Hz. While finishing the project, we decided to use a timer instead of the ring oscillator because it is more accurate and stable.

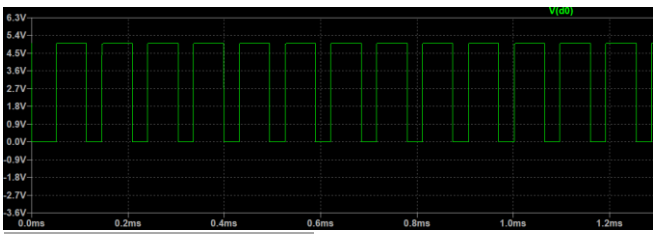


1.0. Simulation of the timer circuit

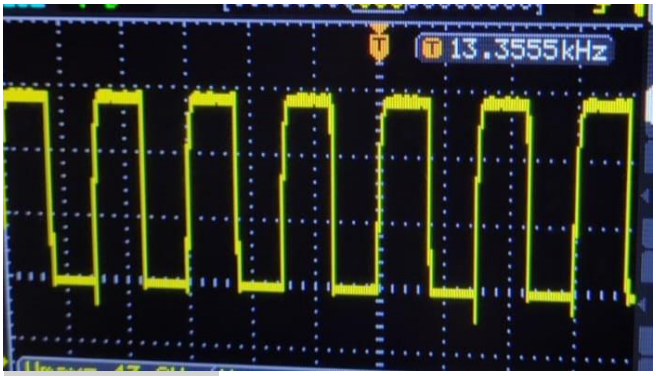
The oscillation frequency of the NE555 timer is set by the resistors (R1 and R2) and capacitors (C1), which are ≈ 10kHz. The output (OUT) pin becomes high when the voltage across C1 charges through R1. The capacitor discharges through R2 when the voltage hits a specific threshold, usually two-thirds of the supply voltage (Vcc), which lowers the output. The resistor and capacitor values dictate the frequency of the continuous pulse train that is produced at the output pin because of repeating this cycle.



1.1The physical circuit of the timer



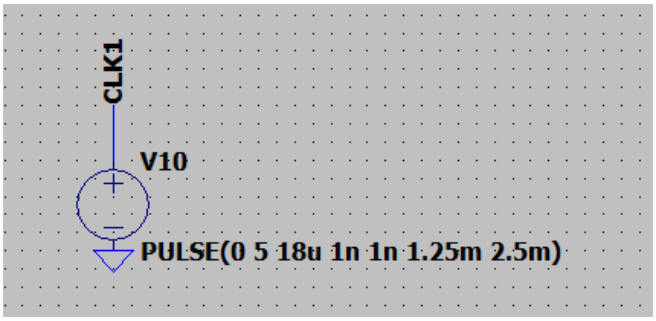
1.2. The output of the Timer.



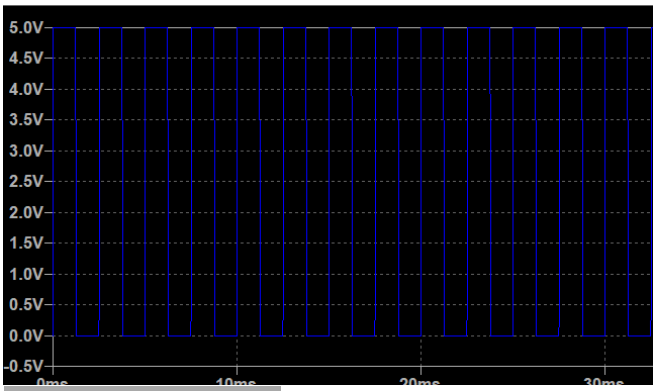
D0 generator output

Clock 1:

A 400 Hz clock signal (CLKI) that is dependable and steady is needed for the uneven seven-sided dice roller circuit. The functioning of several components is synchronized by this clock signal, guaranteeing accurate timing and unpredictability in the output that is produced.
The design factors and implementation alternatives for creating CLKI are covered in detail in this study. The CLK1 is going to be produced by a microcontroller, which in our case is an Arduino Uno



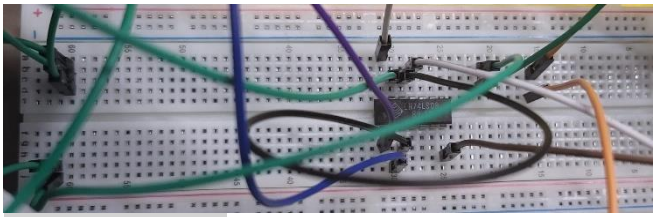
1.3.The simulation of Clock 1.



1.4. The output of clock 1

Intermediate Register and CLK4:

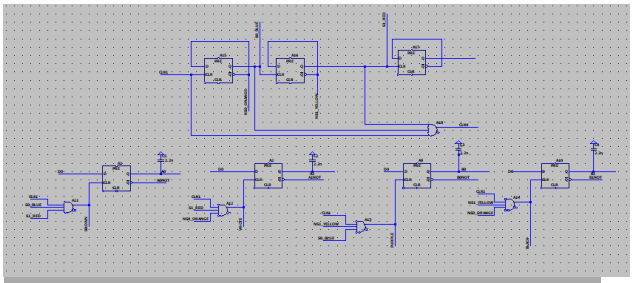
Data Capture: With the triggering edge of the clocking signal (CLKI), the register stores the present value of the data line (D0) from the generator (D). The result is that the random piece selected at that given point is held for processing at a later stage.


1.5. Clock-4-Circuit.

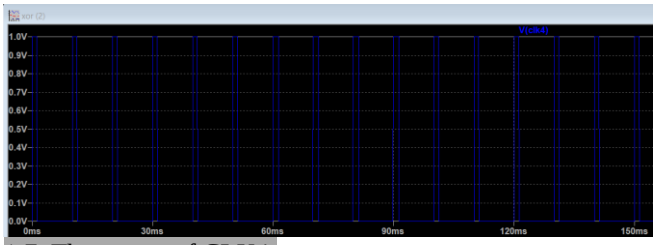
Temporary Storage: Register R which stores the captured data bit (D0) is utilized until it is used to perform the full adder operation. This clock's temporary storage allows the synchronization with the CLKI signal, which is the driver, and then triggers an addition.

Synchronization Point: The inner shift register is a synchronizing block between the asynchronous data generation and the synchronous full adder operation. The data generator having its frequency is composed of the register that works in the condition where the captured bit is integrated into the full adder operation on the specified clock cycles determined by the frequency of CLKI.

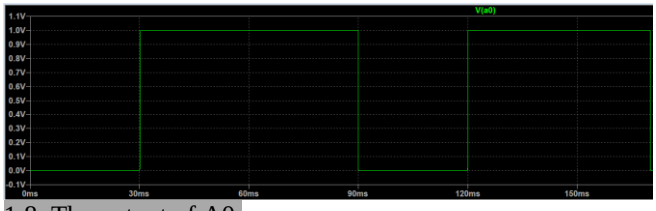
As for CLK4, it was produced from CLK1. CLK1, the output of the first flip-flop, and the output of the second flip-flop will go through an AND gate in order to yield CLK4.


1.6. The Simulation of Intermediate Register and CLK4

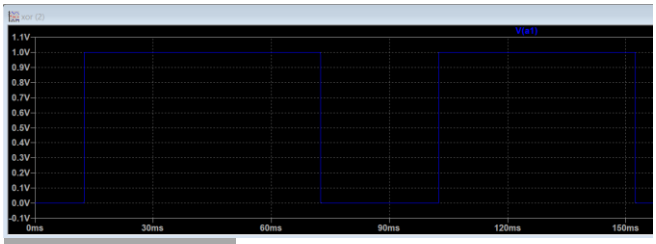
The circuit above is made from a clock and a shift register. The clock generates the slaves that control the functionality of the shift register. The outputs we have are A0, A1, B0, and B1.



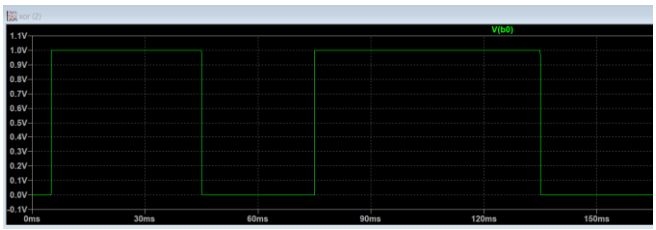
1.7. The output of CLK4.



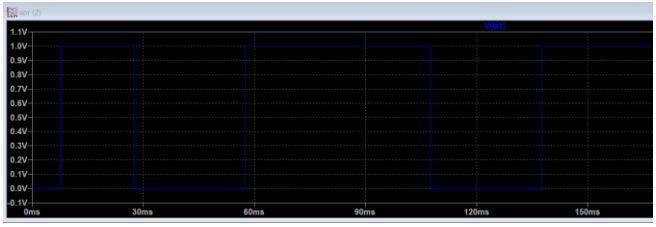
1.8. The output of A0.



1.9. The output of A1



2.0. The output of B0



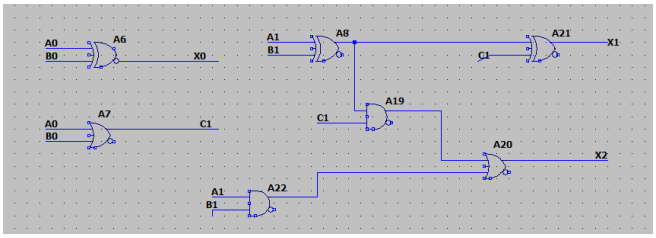
2.1. The output of B

2-bit full adder :

operation of a 2-bit full adder works as a foundation for computing the random numbers created by the data generator. The random number generator generates random numbers from the range of 1 to 7, that represent the six faces of six-sided dice. These numbers must be set using a random number generator so that one can ultimately get the dice roll outcome. Adding Random Numbers: The 2-bit full adder circuit generated headers are received for adding your newly generated random numbers with any existing value stored in the intermediate register. Here the random number plus that of the last face value is employed to determine the current face value. Handling Overflow: The dice cannot be greater than 7 because it has 7 sides in all, so adding may create a number greater than 7. The 2-bit full adder circuit is designed with inputs to sort overflow conditions and make sure that finally, the output is within the allowable range of 1 to 7, the manifestations of which correspond to the faces of the die. Output Determination: The final result of the two-bit addition after the process of handling overflow if possible is stored in the temporary register for the next duty cycle.

Here, the value on the medium number register is equivalent to selecting the face of the 7-sided dice after the addition process, and it is displayed next on the output register for user viewing.

In short, a 2-bit full adder is responsible for the addition of the so-called random values produced by the data generator as well as the sum being the truth-table representation of a 7-sided dice with certain limitations in the range of values (number should be from 1 to 7) and handling a carry-out, which appear during the sum of values.



2.2. simulation of the Full-adder.

The Output Register:

The output register is the block that will put on view the result of the culminating operation - the face of the 7-sided dice after being split down into parts (for example, bit A, which is the first one, bit B the second one, etc.), which is computed by the 2-bit full adder.

Storage of Final Result:

Output register is a kind of sequential circuit that stores the last value, which is the result of regicating the numbers produced by the Data generator.

The completion of the addition procedure by a 2-bit full adder and the handling of possible carryout clocks is followed. The output sum will be stored in the output register.

Display Functionality:

The output segment of the display device configures the data that will be digitally rendered to represent the face of the 7-sided dice.

The data stored in the output register is executed to a format, that is elsified appropriately to display; either in decimal or binary form, it is mainly determined by the design-specific requirements.

Latch and Clocking Mechanism:

The output latch uses register circuits (e.g., D flip-flops) where the output value is stored and kept until it is refreshed with some new value.

A clocked system is implemented to wait for a precise time-lapse to enter the output register with the right data, to have the data representation accurate.

User Interaction:

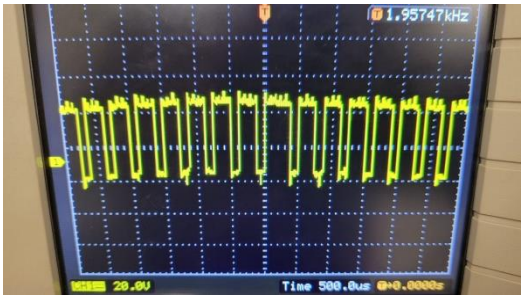
The showcasing by the output register makes it possible to see what the result of a roll of the dice should look like in digital mode, which means it could be used for gaming or educational purposes.

A lucid digital representation of the dice face is a perfectly accurate reflection of the outcome received from the computation of randomly generated numbers and a summation of those.

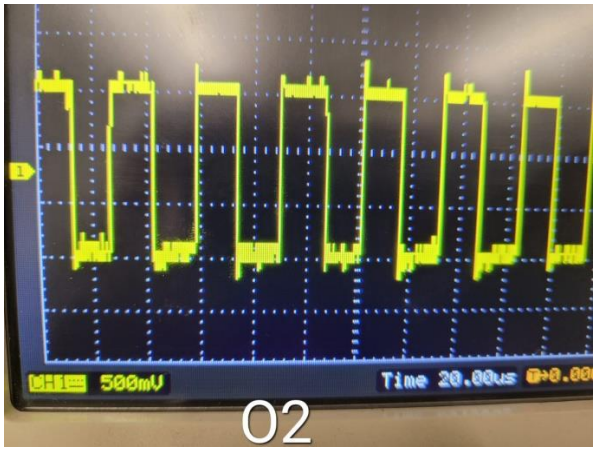
The final outputs of the system:

O0:

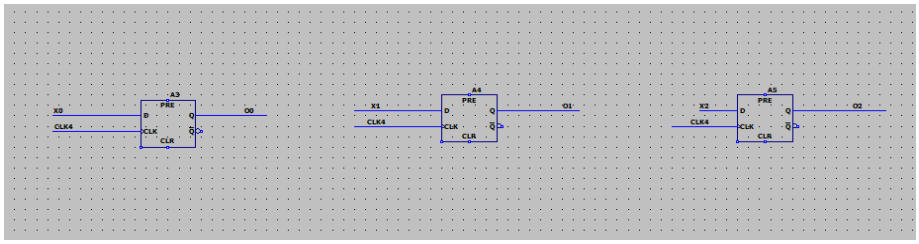
O1:



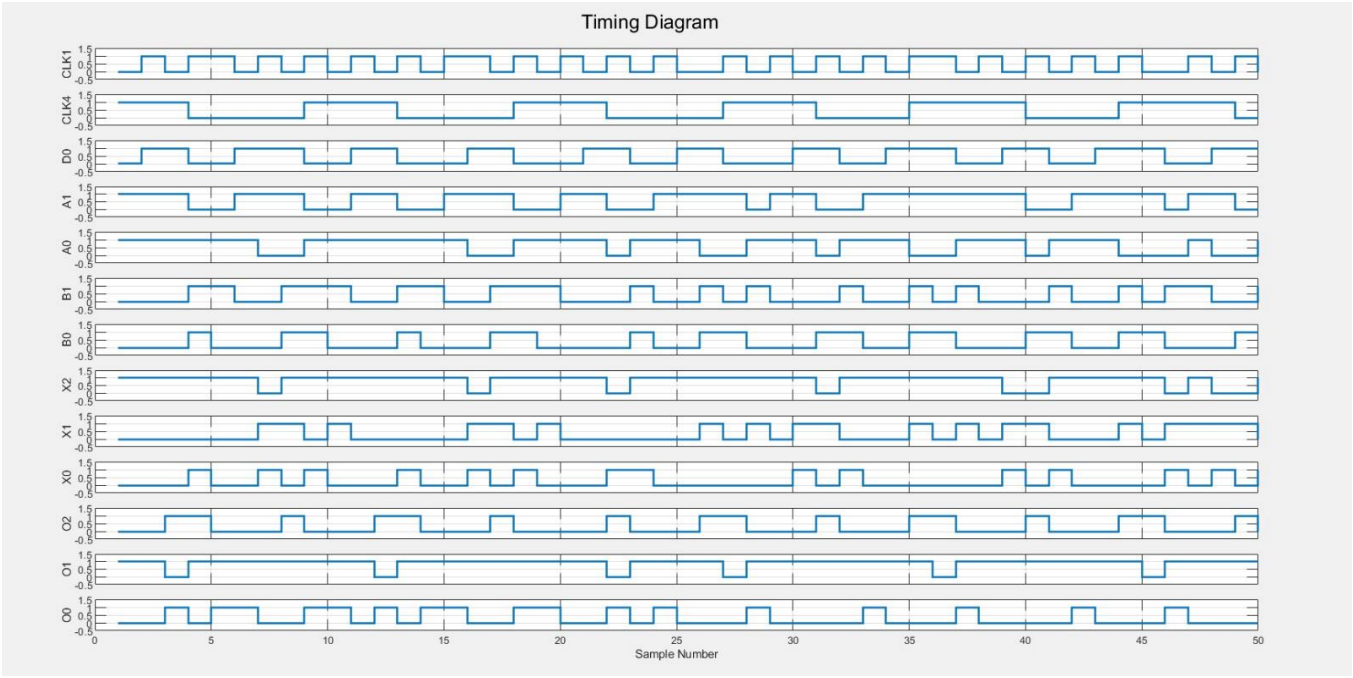
O2:



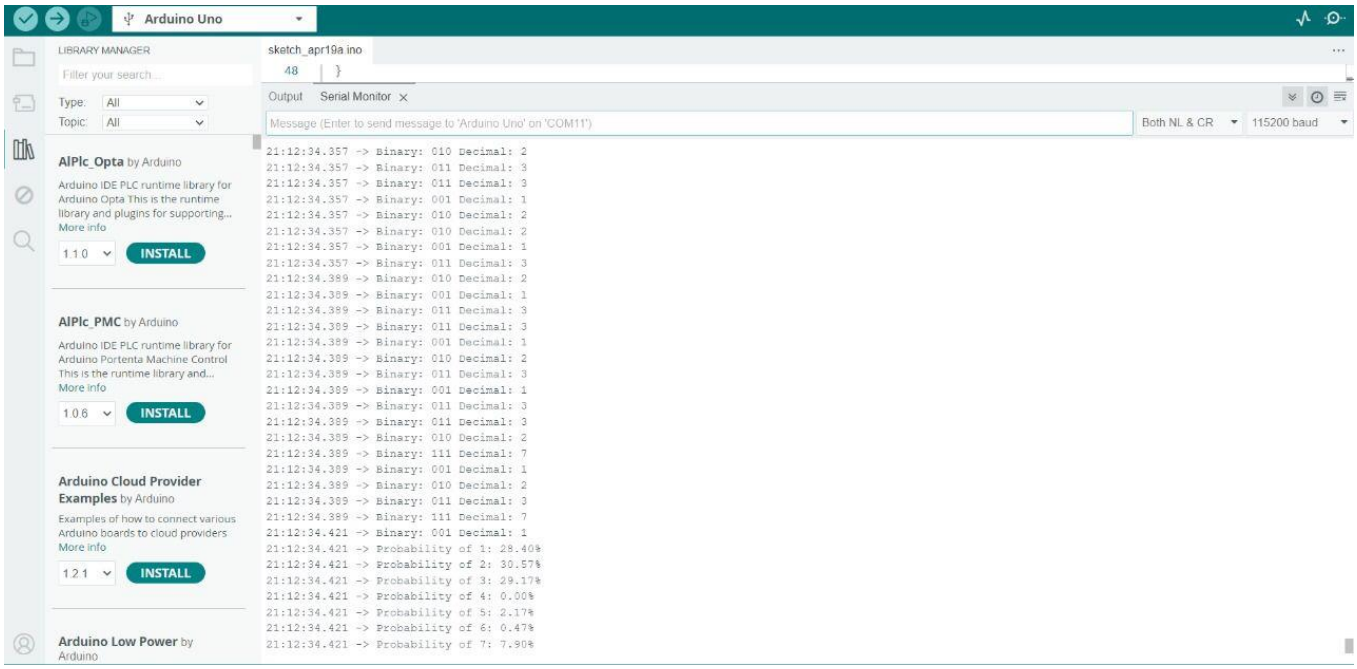
The Output Register:



Timing Diagram:



The probability of the outputs:



Conclusion:

In this project, we successfully designed and implemented an electronic circuit for an uneven 7-sided dice using CMOS transistors. The circuit consists of a data generator, a 2-bit full adder, an intermediate register, and an output register. The data generator generates random numbers within the range of 1 to 7, representing the faces of the dice. The 2-bit full adder adds these random numbers with any existing value in the intermediate register, handling overflow conditions to ensure the final output remains within the valid range. The intermediate register stores the intermediate sum, while the output register displays the result, representing the face of the 7-sided dice after the addition process. This project demonstrates the feasibility of creating a digital implementation of uneven dice and contributes to the field of digital electronics and random number generation.

References:

[1] Digital Design by M. Morris Mano

[2] CMOS Digital Integrated Circuits by Sung-Mo Kang and Yusuf Leblebici.