Digital System Design Capsule 2024 Spring PROJECT 1:

Uneven Seven-Sided Dice Roller | Task 1: Data (D0) generator

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The following report will explain the procedure of which we were asked to simulate a pulse generator for data (D0) that we are going to use in the following tasks of this project. We decided to make a ring oscillator circuit that generates square waves in the frequency of ≈ 5500Hz.

The ring oscillator circuit is a good building block in many digital applications, where it offers versatility and reliability which are needed in our process of making the uneven seven-sided dice roller project. In this circuit the resistors and capacitors play crucial roles in determining the frequency of oscillation and stability of the ring oscillator. The inverter chain of the oscillator is composed of PMOS and NMOS MOSFETs, which serves as the active elements. As the name itself depicts, a ring oscillator is an odd-numbered transistoric chain that begins with an inverter whose output goes into the input of the other one in the sequence.

The chain of PMOS and NMOS transistors alternate in this configuration, providing a continuous signal propagation as a result of which the oscillations is being sustained. Charging and releasing of the capacitors through the MOSFETs generate a constant switching of the states inside the ring. This back-to-back connection gives rise to the oscillation of the output signal whose frequency is dictated by the inverters' propagation delays and time-constants set by the resistors and capacitors.

- Simulation Results:

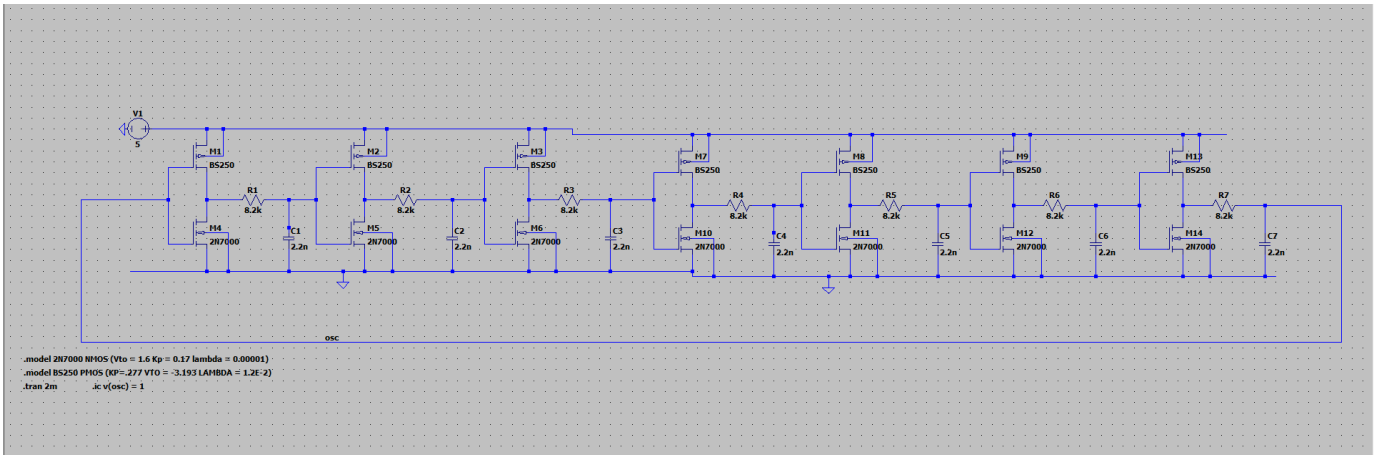

Figure 1.0.

In figure 1.0, the circuit dynamic is explained. The circuit is designed to be a 7 order CMOS with an RC connection. The value of resistance is 8.2k and the value of capacitance is 2,2nF. The NMOS model is assumed to be 2N7000 and the PMOS model is BS250 as they are available at stores. The DC voltage supply is 5V.

- Hand Calculation:

To calculate the frequency of the ring oscillator, we are using the following formula:

$$f = \frac{1}{2nT}$$

Where n is the number of orders in the circuit and T is the period.

Firstly, we must find the period using the following sub-formula:

$$T = \frac{T_{PHL} + T_{PLH}}{2}$$

In the context of a ring oscillator, T_{PHL} (propagation delay from high to low) and T_{PLH} (propagation delay from low to high) represent the propagation delays of the inverter stages in the oscillator. These propagation delays correspond to the time it takes for the output of an inverter to transition from a high state to low state (T_{PHL}) and from a low state to a high state (T_{PLH}) respectively. In simple terms, the period (T) of an oscillator, be it a ring oscillator or any other, is about twice the time it takes the wave (a signal) to move across one inverter stage because first it must complete the high-to-low and low-to-high transition before being in a stable state again. Hence, by having the sum of the inverted signals transition times, it will determine the delays for both transitions. This information is being used to calculate the average time taken for the signal to propagate through one inverter stage. This number is then multiplied by the number of stages, so the result will be the total period of the oscillator.

Since we are using 2N7000 and BS250 MOSFETs, we must consider their drain-source on resistance and input capacitance. For 2N7000: drain-source on resistance = 5ohm, and the input capacitance = 60pF. For BS250 the drain-source resistance = 14ohm and the input capacitance = 45pF.

- $T_{PHL} = 0.7\left(R_{interior\ for\ NMOS} + R_{exterior}\right) \times \left(C_{interior\ for\ NMOS} + C_{exterior}\right)$
  - $T_{PHL} = 0.7\ (5 + 8200) \times (60 \times 10^{-6} + 2.2 \times 10^{-9}) = 1.3 \times 10^{-5}$

- $T_{PLH} = 0.7\left(R_{interior\ for\ PMOS} + R_{exterior}\right) \times \left(C_{interior for\ PMOS} + C_{exterior}\right)$
  - $T_{PLH} = 0.7\ (14 + 8200) \times (45 \times 10^{-12} + 2.2 \times 10^{-9}) = 1.3 \times 10^{-5}$

$$T = \frac{T_{PHL} + T_{PLH}}{2} = \frac{1.3 \times 10^{-5} + 1.3 \times 10^{-5}}{2} = 1.3 \times 10^{-5}$$

$$f = \frac{1}{2nT} = \frac{1}{2 \times 7 \times 1.3 \times 10^{-5}} = 5495.5Hz$$

As a result, the theoretical value of the frequency is 5495.5Hz, and when we compare it with the simulation result, we will see the following:

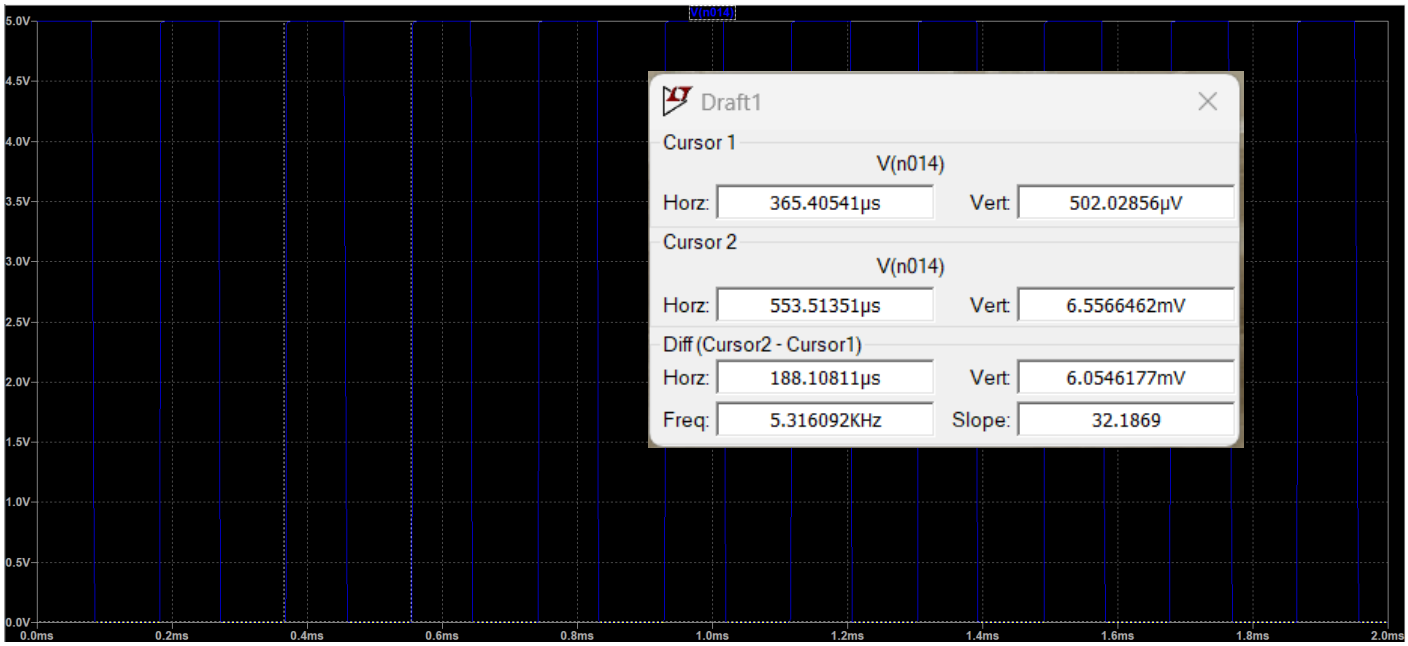

Figure 1.1.

We can clearly see that the two result are close to each other, where the simulation result is 5316Hz.

In the end, the composition and utilization of a ring oscillator circuit with resistors, capacitors, PMOS/NMOS MOSFETs provide the ability to provide the best possible clock generation delay or signal modulation functionalities. By taking care to select values for the components that are just right and optimally tuned to the oscillator, one can design the oscillator to be an ideal match to the specific needs of the application, which guarantees the best performance and efficiency.