MIDDLE EAST
TECHNICAL UNIVERSITY

ELECTRICAL-ELECTRONICS ENGINEERING
DEPARTMENT

EE463 HW2- DEVICE PARAMETERS

PREPARED BY
HÜSEYİN OĞUZ-2516623
AHMAD PARWAİZ QORAM- 1907336

Homework 2

Device Parameters

Introduction

We will review the major power diode and MOSFET parameters, their respective loss mechanisms, and the compromises that are made in device selection with respect to different voltage, current, and material ratings. The derived analysis, based on specific component examples, emphasizes how these traits impact efficiency and performance quantitatively. These physical understandings are then used in the development of designs for buck and boost converters, both analytically and through simulation, by emphasizing conduction modes, ripple, and the effects of non-idealities on converter behavior.

Experimental Results

Q1-

a)

The main characteristics of the power diode are its average forward current, I_{ave}, representing the maximum continuous current the diode can conduct safely under given thermal conditions, thereby reflecting the ability of the diode to handle steady-state operation; peak repetitive reverse voltage, V_{RRM}, as the highest reverse voltage the diode can withstand repeatedly without breaking down, showing the capability to endure reverse stress in normal switching applications; non-repetitive surge current, I_{Fsm}, which defines the largest short-term current the diode can survive during events such as inrush or fault conditions, demonstrating the robustness of the diode against temporary overloads; reverse recovery time, t_{rr}, describing how quickly the diode switches from conducting to blocking, which affects switching losses and efficiency directly in high-frequency circuits. Finally, the forward voltage drop, V_f, is the voltage across the diode in the case of conduction, and it plays an important role in determining conduction losses and overall system efficiency.

b)

The major sources of losses in diodes are conduction and switching, both dependent on electrical and thermal behavior. Conduction losses occur whenever the diode is carrying current, caused by the forward voltage drop V_f; larger forward current directly increases power dissipation and heat. Switching losses happen during turn-off, when the diode briefly conducts in the reverse direction-this is determined by the reverse recovery charge Q_{rr} and the reverse recovery time t_{rr}, and it becomes especially important at high switching frequencies. Temperature also plays a key role, since V_f, Q_{rr}, and leakage currents change with junction temperature, while repeated high surge currents may worsen thermal buildup. In other words, forward voltage, conduction current, reverse recovery behavior, switching frequency, and operating temperature are the major influencing factors on the diode losses.

c)

Part Number	Type / Material	V_{RRM} (V)	I_{ave}(A)	Typical V_F (V)(at I_{ave})	Reverse Recovery Behavior
STPST10H100	Silicon low-voltage Schottky	100	10	~0.7 V @ 10 A	Essentially zero reverse-recovery

					charge (Schottky)
GHXS100B065S-D3	SiC Schottky diode module	650	100	1.61	Zero/near-zero reverse recovery (SiC SBD)

In this respect, the comparison between the 10A Silicon Trench Schottky (STPST10H100) and the 100A Silicon Carbide (SiC) Schottky (GHXS100B065S-D3) defines the trade-off between conduction efficiency and blocking capability that is typically performed during power semiconductor device selection. The low-voltage Silicon device (100V nominal rating) offers very low conduction losses, thanks to the very low forward voltage drop (V_F ≈0.7V$); it is therefore very efficient for lower-power applications. In contrast, the 100A SiC diode is designed to block much larger voltages of 650V; being based on a wide-bandgap material, this inherently gives a larger V_F (≈1.61V$); however, the primary advantage of SiC technology is that it ensures "zero reverse recovery" behavior at these higher voltages-so whereas a conventional Silicon diode at 650V would be subjected to severe switching losses, the SiC Schottky meets the same switching speed as the low-voltage counterpart, thus enabling high-frequency operation of high-power converters despite the increased static conduction loss.

d)

Part Number	Type / Material	V_{RRM} (V)	I_{ave}(A)	Typical V_F (V) (at I_{ave})	Reverse Recovery Behavior
RFN10RSM2S	Ultra-fast recovery (Si) (ROHM)	200 V	10	0.88 (Typical at 25 ℃).	trr= 15ns
VS-VSKC91/10	Silicon Carbide Schottky Diode (Z-Rec® Rectifier)	1000 V (1 kV)	100	Typical forward/peak on-state voltages listed 1.5 V at 25 ℃	Zero reverse-recovery (SiC Schottky) → high-frequency, low loss

The two diodes you listed show complementary trade-offs: The RFN10RSM2S is a 200 V, 10 A ultra-fast silicon device with a typical forward drop of about 0.88 V at 25 °C and a measurable reverse-recovery time (~15 ns), so it minimizes conduction loss at low-to-moderate currents and is compact and cost-effective for low-voltage SMPS/free-wheeling roles but still incurs switching losses and EMI from its finite trr. By contrast, the VS-VSKC91/10 is a 1 kV SiC Schottky rated for much higher average currents (listed as 100 A in your row) with a forward/peak on-state figure around 1.5 V at 25 °C and essentially zero reverse recovery; that means at high voltage and high switching frequency it delivers far lower switching losses and allows higher switching speeds and junction temperatures, improving overall efficiency and thermal headroom for PFC/inverter/high-voltage stages—at the cost of higher forward drop at the specific current point you showed, higher unit price, and different thermal/packaging and surge considerations. In short: choose the RFN10RSM2S where low cost, low voltage and modest switching speed matter; choose the VS-VSKC91/10 where high voltage, high current and minimal reverse-recovery losses at high frequency justify the extra cost and cooling/packaging requirements.

e)

Part Number	Type / Material	V_{RRM} (V)	I_{ave}(A)	Typical V_F (at I_{ave})	Reverse Recovery Behavior
RFN10RSM2S	Ultra-fast recovery (Si) (ROHM)	200 V	10	0.88 V (Typical at 25 °C).	trr=15 ns
STPST10H100	Silicon low-voltage Schottky	100	10	~0.7 V @ 10 A	Essentially zero reverse-recovery charge (Schottky)

Compared to the 200 V RFN10RSM2S (Si, 10 A, Vf ≈ 0.88 V, trr ≈ 15 ns) and the low-voltage STPST10H100 Schottky (100 V, 10 A, Vf ≈ 0.7 V, essentially zero reverse recovery), a 1 kV/100 A SiC Schottky such as the VS-VSKC91/10 (typical forward/peak ~1.5 V at its rated current, zero reverse recovery) shows the main tradeoffs engineers encounter as voltage and current ratings rise: higher voltage capability usually requires a thicker or more heavily doped junction (larger die or different material), which tends to increase forward drop and leakage at a given current and raises thermal resistance unless the package is scaled up; higher continuous current rating requires larger junction area and better heat sinking, which reduces temperature rise for the same current but increases package size, cost and often stray inductance. Material choices change behavior: Si devices (fast/ultrafast) have finite reverse-recovery charge (trr) that causes switching losses and EMI at high dV/dt, whereas Schottky and SiC Schottky have essentially no recovery loss and therefore much lower switching loss and better efficiency at high frequency, but SiC parts typically cost more and can exhibit higher reverse leakage at high temperature. Over-designing current rating (picking a 100 A diode for a 10 A application) gives clear benefits—much lower thermal stress, higher surge margin, longer lifetime and better reliability under transient abuse—but has downsides: larger cost and footprint, possibly higher junction capacitance and parasitic inductance (which can worsen switching behavior), and in some high-voltage technologies a larger device can have higher absolute leakage; moreover choosing a much higher voltage-rated part than needed can increase forward drop and reduce efficiency. In short, pick the lowest VRRM that comfortably exceeds your transient margins and a current rating that gives modest headroom; use SiC Schottky where switching losses and high-frequency efficiency matter, and reserve heavy over-rating for designs that need exceptional surge margin or simplified thermal management.

Q2-

a)

The main characteristics of a power MOSFET are the drain-to-source voltage, Vds, which is the maximum voltage that a MOSFET can block when it is in the off-state and therefore reflects its high-voltage stress capability; the continuous drain current, Id, which is the maximum current the device can conduct continuously under specified thermal conditions and thus shows its steady-state load-carrying capability; on-state resistance, Rds(on), which is the resistance between drain and source when the MOSFET is fully ON and thus directly affects the conduction losses and efficiency; the gate charge, Qg, which is the amount of charge required to fully switch the MOSFET on and therefore impacts switching speed and driving requirements; and threshold voltage, Vth, which is the minimum gate voltage required to turn the MOSFET on and hence affects the design of the gate drive and precise control over switching behavior.

b)

The main contributors to MOSFET losses are conduction and switching losses, both of which depend very much on the electrical characteristics of the device and operating conditions. Conduction losses occur when the MOSFET is on and have a proportional relation to the on-state resistance RDS(on) and the square of the drain current (Ids^2*RDS(on)), with higher current or higher RDS(on) increasing power dissipation directly. Switching losses occur during turn-on and turn-off when voltage and current are overlapped, and these depend on such factors as total gate charge Qg, gate-to-source threshold voltage Vth, and switching speed. The higher the frequency, the higher the losses. Temperature also affects both types of losses because RDS(on) increases with junction temperature, while gate charge can vary slightly with temperature. To sum

up, the main factors that determine MOSFET losses are RDS(on), drain current, gate charge, switching frequency, and operating temperature.

c)

Part Number	Type / Material	V_{DS} (V)	I_D(A)	$R_{DS(on)}$(mΩ)	Total Gate Charge Qg (nC)
IRF3205	Silicon MOSFET	55	110	8	146 nC
C2M0160120D	SiC MOSFET	1200	18	160	40 nC

If we examine the voltage rating, current capability, and device technology between the IRF3205 silicon MOSFET and the C2M0160120D SiC MOSFET, a number of key parameters are affected. For example, IRF3205 is a low-voltage silicon MOSFET rated to 55 V and 110 A with correspondingly low RDS(on) of 8 mΩ and relatively high gate charge of 146 nC, reflecting the trade-off of high current at low voltage. This can be compared with the C2M0160120D as a high-voltage SiC MOSFET rated to 1200 V but only 18 A, with much higher RDS(on) at 160 mΩ and lower gate charge of 40 nC. It reflects the typical trend in power devices whereby, with increasing voltage rating, on-resistance goes up significantly, thereby limiting current capability, while gate charge can go down in widebandgap devices like SiC, enabling faster switching and higher efficiency at high voltages. The selection of a device with a current rating far above application requirements reduces conduction losses but may increase the gate drive needs along with cost and parasitic effects. Likewise, a greatly underutilized voltage rating could result in an unnecessarily larger die size and thermal capacity.

d)

Part Number	Type / Material	V_{DS} (V)	I_D(A)	$R_{DS(on)}$(mΩ)	Total Gate Charge Qg (nC)
IRFP250N	Silicon MOSFET	200	30	75	123
C3M0065100K	SiC MOSFET	1000	35	65	35

A comparison of the IRFP250N silicon MOSFET and the C3M0065100K SiC MOSFET highlights how both device technology and ratings of voltage/current impact key parameters. The IRFP250N is a 200 V, 30 A silicon MOSFET featuring an RDS(on) of 75 mΩ and a total gate charge of 123 nC, optimized for moderate voltage and current with relatively low conduction losses and manageable gate drive requirements. By contrast, the C3M0065100K is a wide-bandgap SiC MOSFET rated for 1000 V and 35 A featuring a much lower RDS(on) of 65 mΩ and a much smaller gate charge of 35 nC. Because of the superior properties of SiC, its conduction resistance is only a little lower than that of the IRFP250N even though its voltage rating is much higher, and its small gate charge allows much faster switching. This comparison illustrates that SiC allows designers to achieve both high voltage and high current within one device while maintaining low switching and conduction losses. Normally, however, SiC devices are more expensive, and attention should be given to gate drive circuitry in order to exploit their high-speed capability fully.

e)

Part Number	Type / Material	V_{DS} (V)	I_D(A)	$R_{DS(on)}$(mΩ)	Total Gate Charge Qg (nC)
C2M0160120D	SiC MOSFET	1200	18	160	40
C3M0065100K	SiC MOSFET	1000	35	65	35

A comparison of the C2M0160120D and the C3M0065100K SiC MOSFETs sheds further light on how voltage and current ratings interact with key device parameters. The former is rated at 1200 V and 18 A, features a high RDS (on) of 160 mΩ and a moderate total gate charge of 40 nC-the result of a required trade-off of

achieving very high voltage capability: the thicker drift region required for supporting 1200 V translates into higher on-resistance and reduced ability to conduct higher currents efficiently. The latter device features a slightly lower voltage rating of 1000 V but achieves a much higher current rating of 35 A, with a lower RDS (on) of 65 mΩ and a reduced gate charge of 35 nC. This illustrates that the increase in current capability (by increasing active area) when the voltage is reduced can substantially improve conduction efficiency. In general, RDS (on) increases substantially as the voltage rating rises unless wide-bandgap technology such as SiC is employed. An overdesigned MOSFET-for example, selecting a device featuring a much higher current rating than what is needed-can reduce conduction losses as well as improve thermal margins, thanks to the generally lower RDS (on). However, it usually increases cost and parasitic capacitances, possibly leading to increased switching losses and complicating the design of the gate drive. The main conclusion is that balancing voltage, current, and device technology is crucial for the optimization of efficiency, cost, and systems performance.

Q3)

a) We need minimum load current $I_{load,min}$ to guarantee CCM.

Inductor current ripple:

$$\Delta I_L = \frac{V_{in} - V_{out}}{L} D\, T_s$$

where $D=V_{out}/V_{in}$ is the duty cycle and $T_s=1/f_s$ is the switching period.

Minimum inductor current should stay above 0 for CCM:

$$I_{L,min} = I_{load} - \frac{\Delta I_L}{2} > 0 \quad \Rightarrow \quad I_{load} > \frac{\Delta I_L}{2}$$

The inductor current ripple:

$$\Delta I_L = \frac{V_{in} - V_{out}}{L} \cdot D \cdot T_s$$

$D=V_{out}/V_{in}$, so:

$$\Delta I_L = \frac{V_{in} - V_{out}}{L} \cdot \frac{V_{out}}{V_{in}} \cdot \frac{1}{f_s}$$

$$\Delta I_L = \frac{(V_{in} - V_{out})V_{out}}{LV_{in}f_s}$$

Minimum load current is:

$$I_{load,min} = \frac{\Delta I_L}{2} = \frac{(V_{in} - V_{out})V_{out}}{2LV_{in}f_s}$$

Since the higher V_{in}, the lower the duty cycle and the inductor ripple, CCM is most at risk when input voltage is maximum. When we put V_{in}=200V, and the other given values, we get:

$$I_{load,min} = \frac{9600}{4000} = 2.4\,\text{A}$$

b)

When the switch is on, $V_L = V_{in} - V_{out}$, so inductor current rises:

$$\Delta I_{L,\text{rise}} = \frac{(V_{in} - V_{out})}{L} D\, T_s.$$

When the switch is off, the inductor current falls by the same amount:

$$\Delta I_L = \frac{(V_{in} - V_{out})}{L} D\, T_s$$

where $D = V_{out}/Vin$ and $T_s = 1/f_s$

$$\Delta I_L = \frac{(V_{in} - V_{out})\, V_{out}}{L\, V_{in}\, f_s}$$

The capacitor current is the AC part of the inductor current ($i_c(t) = i_L(t) - I_{out}$).

$$Q = \tfrac{1}{2} \times \text{base} \times \text{height} = \tfrac{1}{2} \left(\frac{T_s}{2}\right) \left(\frac{\Delta I_L}{2}\right) = \frac{\Delta I_L\, T_s}{8}$$

This charge produces the peak change in capacitor voltage, so the output peak to peak ripple is

$$\Delta V_{o(pp)} = \frac{Q}{C} = \frac{\Delta I_L\, T_s}{8C}$$

Substitue T_s and ΔI_L:

$$\Delta V_{o(pp)} = \frac{(V_{in} - V_{out})\, V_{out}}{8\, L\, C\, V_{in}\, f_s^2}$$

Inductor ripple increases with input voltage, so the worst case is at $V_{in,max} = 200$ V.

$$\Delta I_L\Big|_{200} = \frac{(200 - 120) \cdot 120}{100 \times 10^{-6} \cdot 200 \cdot 100 \times 10^3} = 4.80 \text{ A}$$

$$\Delta V_{o(pp)} = \frac{4.80}{8 \cdot 100 \times 10^3 \cdot 10 \times 10^{-6}} = 0.60 \text{ V (pp)}$$

c)

I choose R value from the formula R=(V^2)/P. I choose R as R=(120^2)/500=28.8 Ω

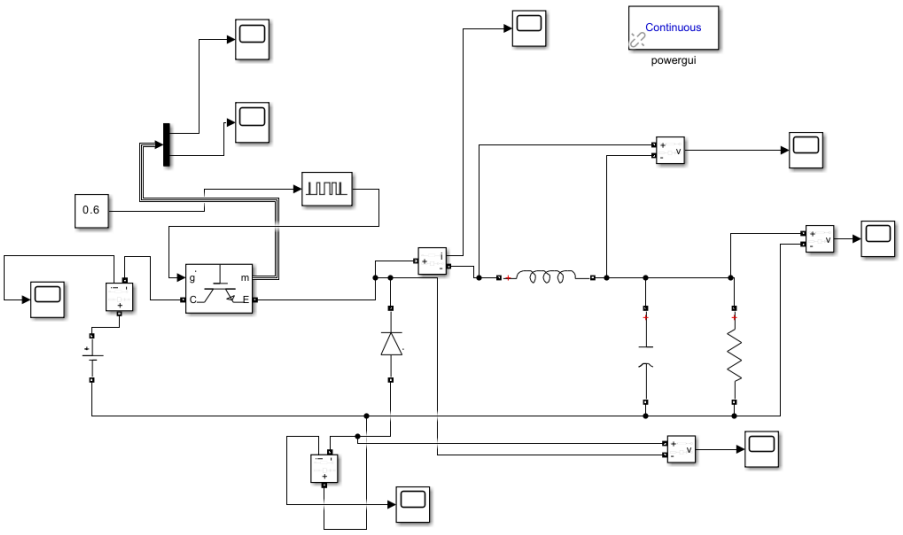

Figure 3.1- Buck converter

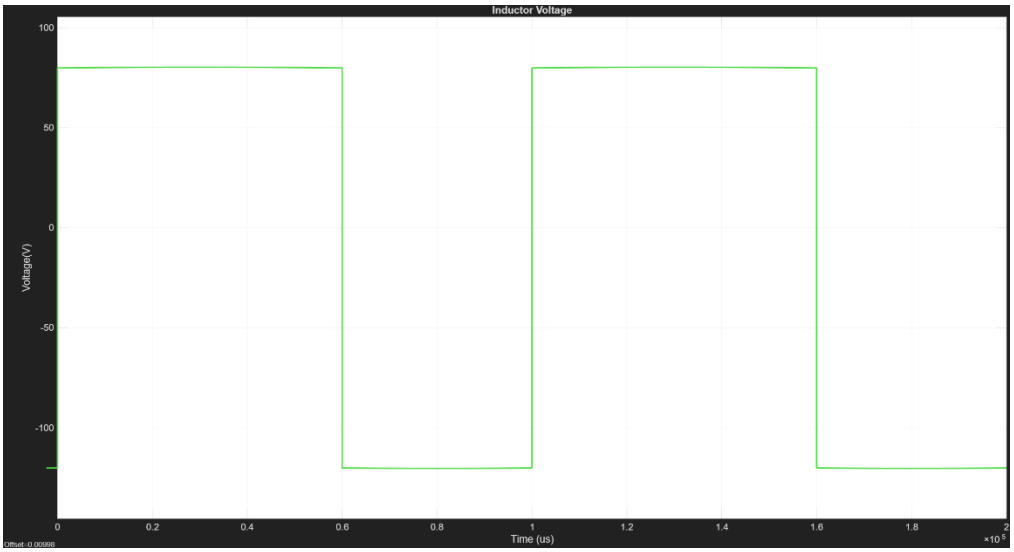

Figure 3.2- Inductor voltage

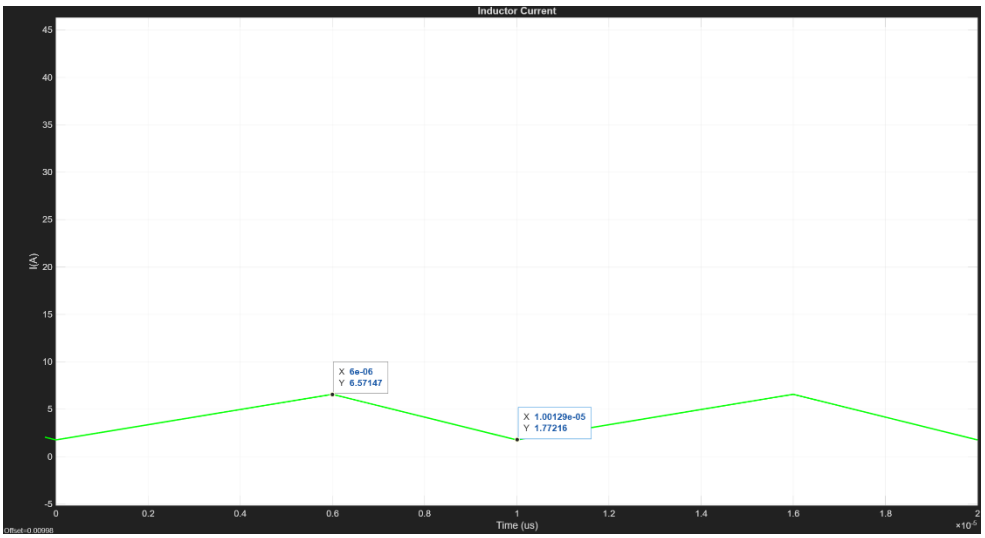

Figure 3.3- Inductor current

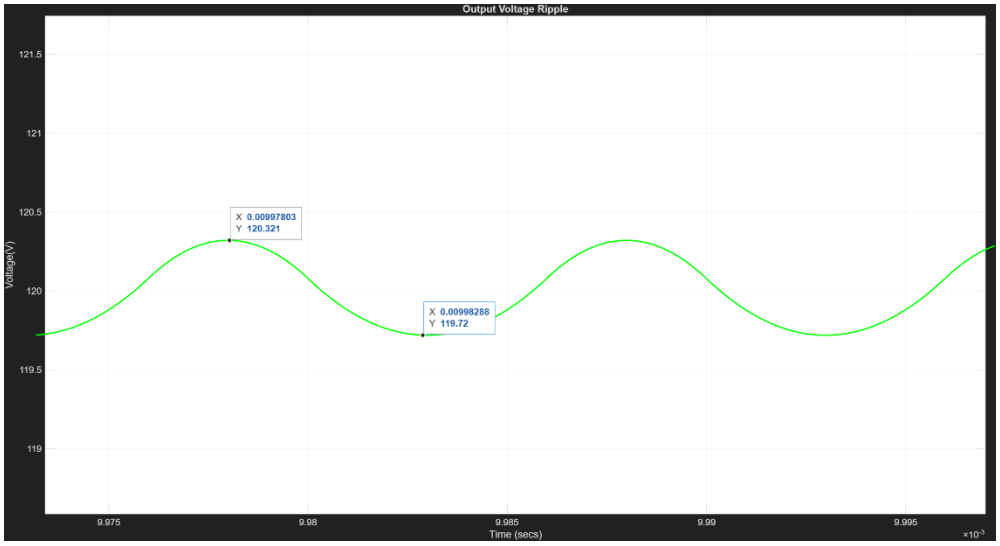

Figure 3.4- Output voltage ripple

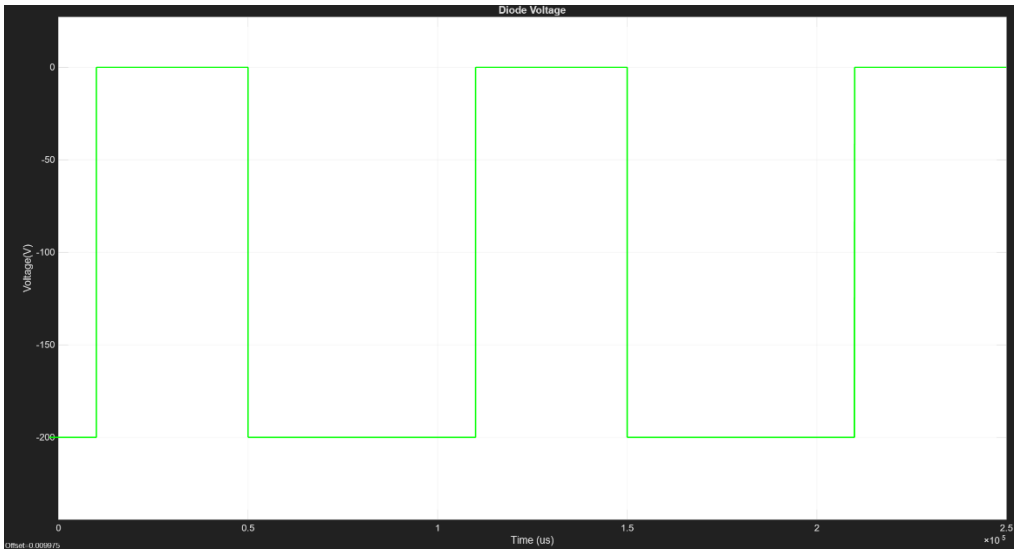

Figure 3.5- Diode voltage

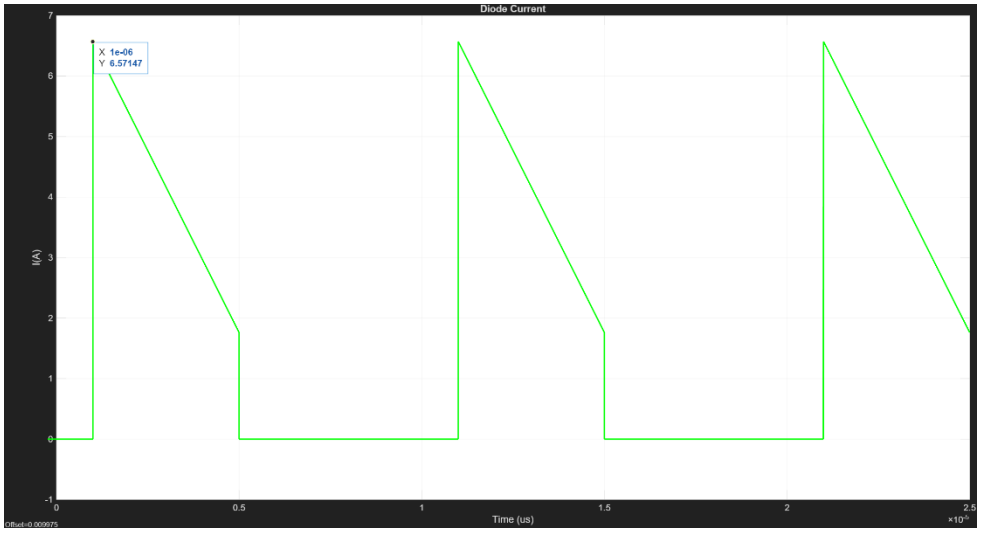

Figure 4.6- Diode current

Figure 3.7- Switch voltage

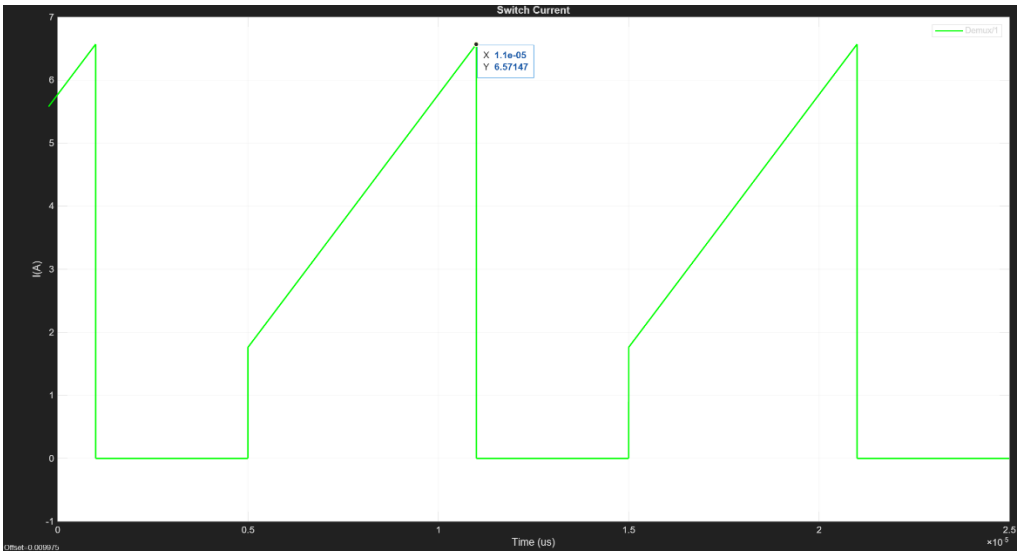

Figure 3.8- Switch current

The Buck converter simulation successfully reaches the steady state for the case of Vin=200V, Vout=120V, and Pout=500W, corresponding to a duty cycle of D=0.6 and an average current of 4.17A. The inductor voltage confirms the principle of steady state, where the volt-seconds are balanced, with segments of value 80V and 120V; the Inductor Current is in CCM, oscillating between 1.77A and 6.57A with the correct average value. The filtering action of the converter is excellent: the output voltage ripple is very low, with only a 0.601V peak-to-peak variation around the desired 120V DC level. The switching elements behave complementarily: the switch voltage blocks 200V and the switch current carries the rising inductor current during D*T_s, while the diode voltage blocks 200V and the diode current carries the falling inductor current during (1-D) *T_s. These results confirm that such a step-down topology operates in stable and efficient mode.

d)

Inrush current is the maximum instantaneous input current that an electrical device draws during its initial power-up phase, largely caused by the rapid charging of output capacitors. These act as a short circuit to instantaneous voltage changes (i = C*dv/dt) before reaching a steady state.

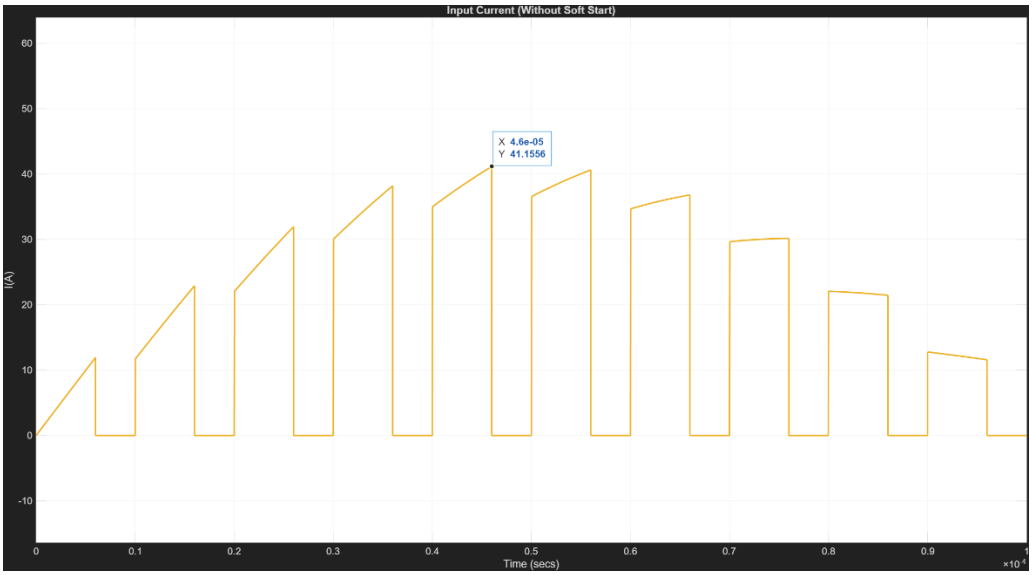

Figure 3.9- Input current without soft start

From the simulation results in the hard-switching scenario of part-c, there is a severe inrush current spike of about 42A. This is because the large error initially between the reference and output voltage will force the duty cycle to saturate near 100% and apply the full input voltage across the inductor. In order to avoid this detrimental surge, it was proposed and implemented to use a Soft Start: a PID controller (P= 0.001, I=10, D=0) driven by a ramp reference signal instead of a step input, which will limit the error magnitude and increase the duty cycle gradually.

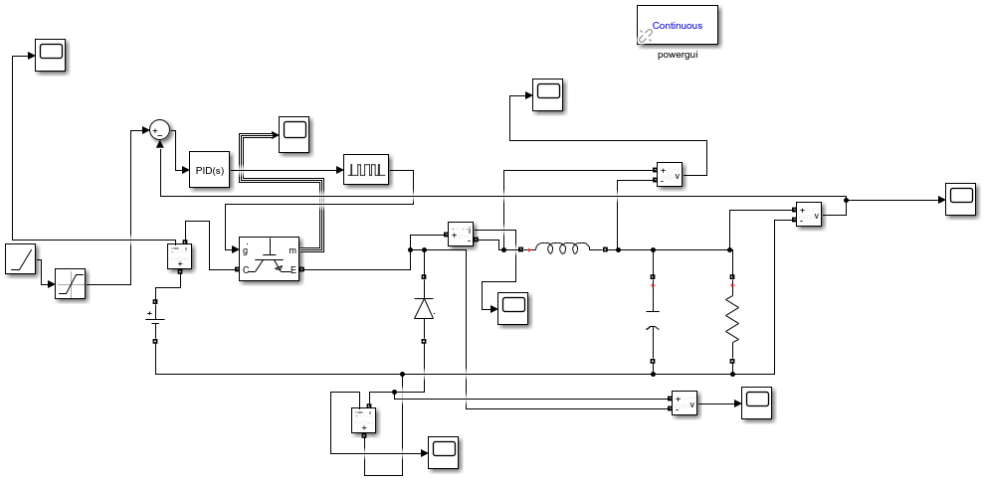

Figure 3.10- The circuit for the soft start

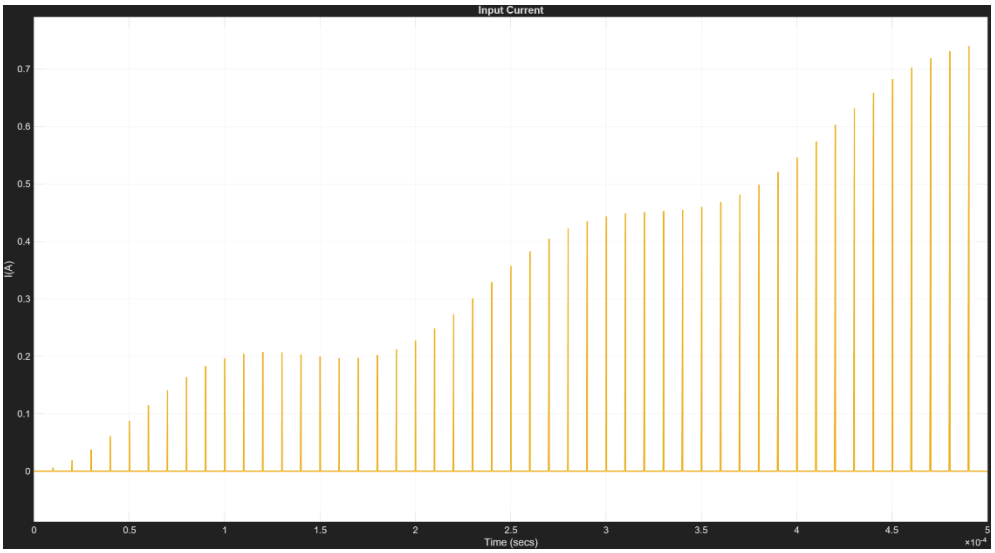

Figure 3.11- Input current with soft start

By comparing the two simulation results, it can be seen that the proposed solution significantly enhances the system performance. While in the uncontrolled case, there is a dangerous spike of 42A, the implementation of soft-start yields a smooth, monotonic rise of the input current, which approaches the steady-state value of around 6.5A slowly and eliminates the electrical stress on the input source and components.

Q4)

a)

$$\Delta I_{L,\text{rise}} = \frac{V_{in}\, D\, T_s}{L}$$

$$I_{L,\text{avg}} = I_{in} = \frac{P_{out}}{V_{in}}$$

To be in the CCM, inductor current should never reach zero:

$$I_{L,\text{avg}} > \frac{\Delta I_L}{2}$$

Substitute ΔI_L and I_{in}:

$$\frac{P_{out}}{V_{in}} > \frac{1}{2} \cdot \frac{V_{in}\, D\, T_s}{L} \quad \Longrightarrow \quad L > \frac{V_{in}^2\, D\, T_s}{2\, P_{out}}$$

$D = 1 - \frac{V_{in}}{V_{out}}$ for a boost converter, so:

$$L > \frac{V_{in}^2 \left(1 - \frac{V_{in}}{V_{out}}\right) T_s}{2 P_{out}}$$

To find the worst case V_{in}, we need to differentiate the equation:

$$f(V_{in}) = V_{in}^2\left(1 - \frac{V_{in}}{V_{out}}\right) = V_{in}^2 - \frac{V_{in}^3}{V_{out}}$$

$$f'(V_{in}) = 2V_{in} - \frac{3V_{in}^2}{V_{out}} = V_{in}\left(2 - \frac{3V_{in}}{V_{out}}\right) = 0$$

V_{in}=0 or V_{in}= (2/3)*V_{out} . Vout=72 V is given, so, Vin=48 V.

$$L_{\min} = \frac{V_{in}^2\, D\, T_s}{2P_{out}} = \frac{48^2 \cdot \frac{1}{3} \cdot 10^{-5}}{2 \cdot 150} = 2.56 \times 10^{-5}\ \text{H} = 25.6\ \mu\text{H}$$

b)

I choose R value from the formula R=(V^2)/P. I choose R as R=(72^2)/150= 34.56 Ω

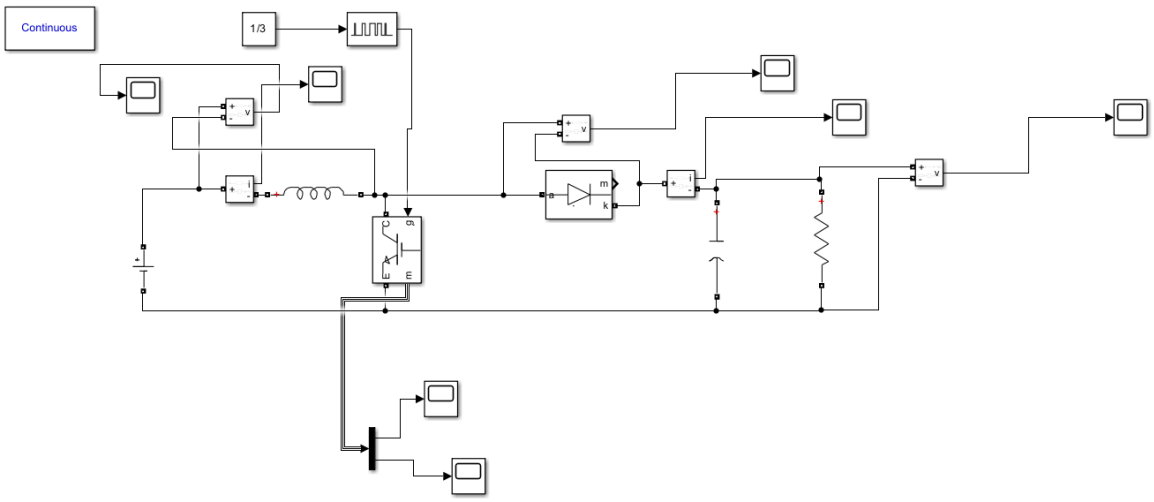

Figure 4.1- Boost converter

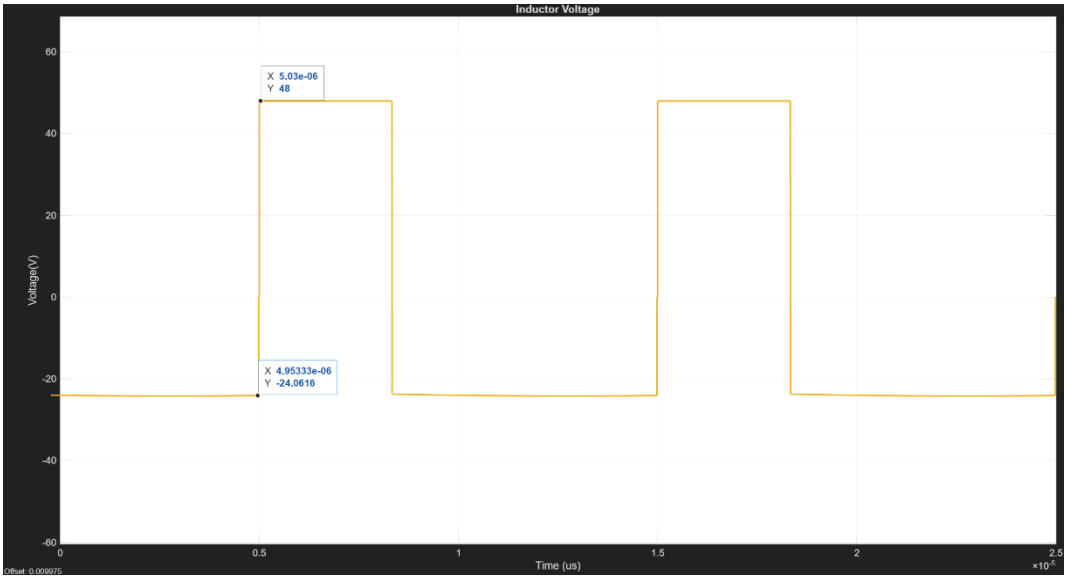

Figure 4.2- Inductor voltage

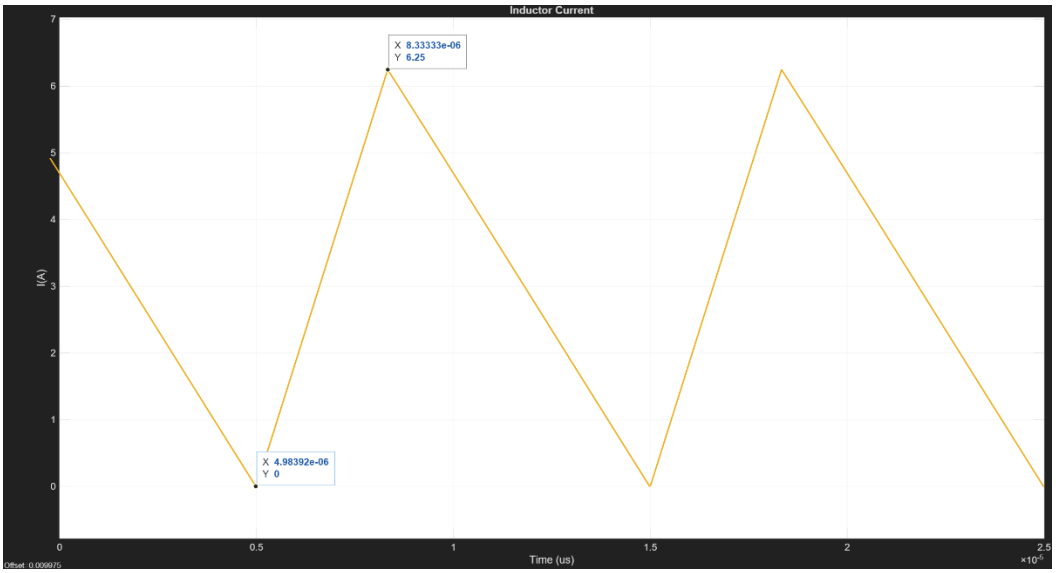

Figure 4.3- Inductor current

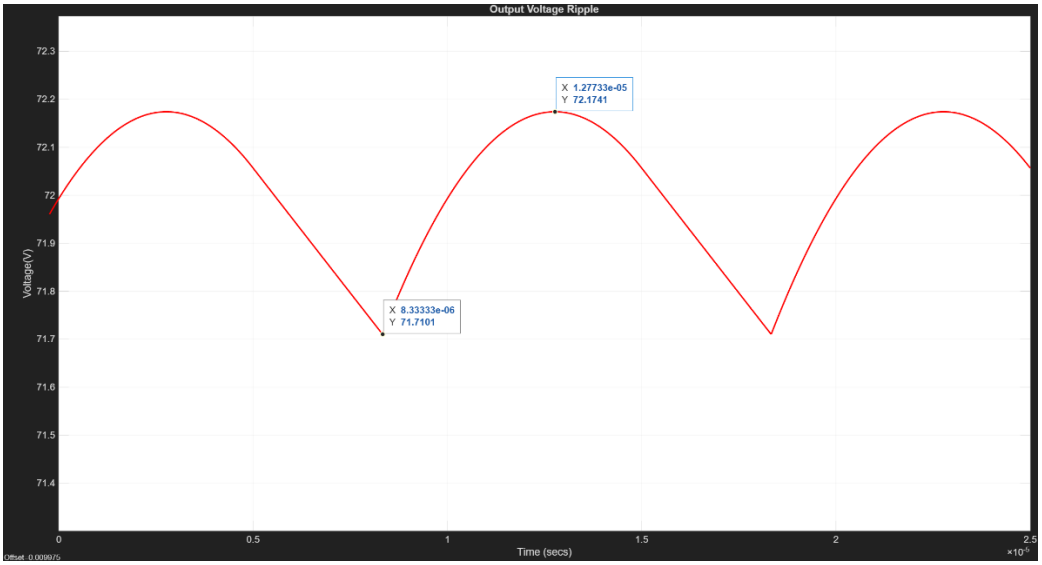

Figure 4.4- Output voltage ripple

Figure 4.5- Diode voltage

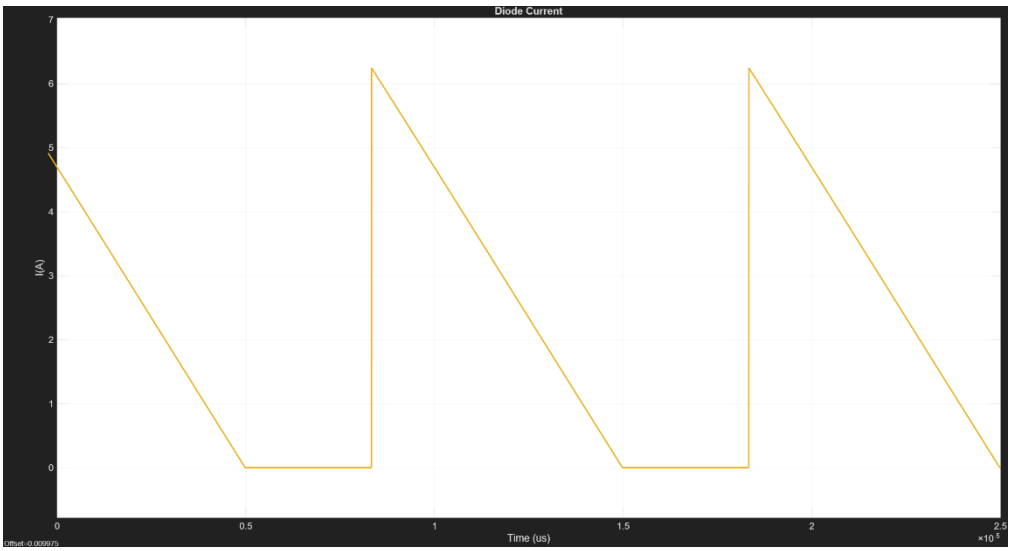

Figure 4.6- Diode current

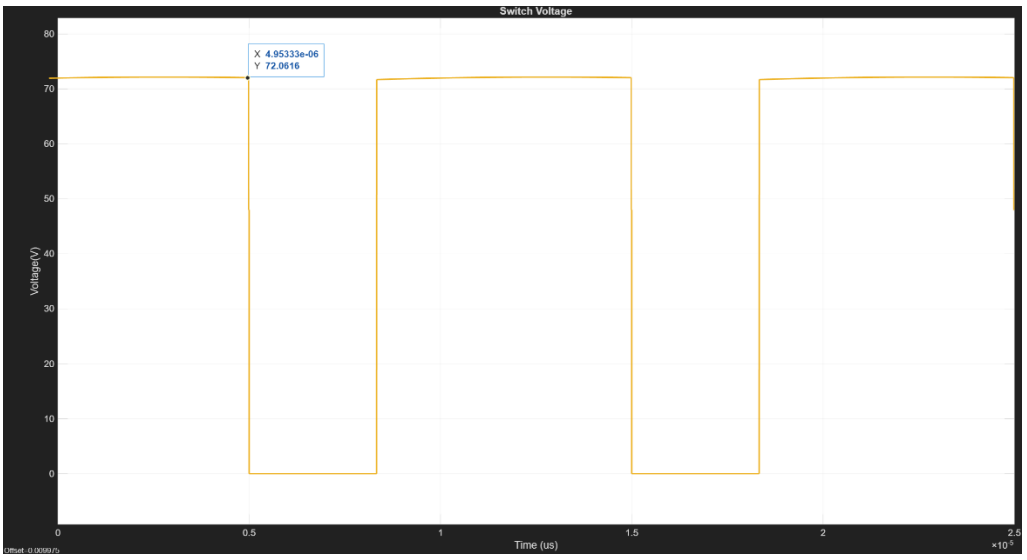

Figure 4.7- Switch voltage

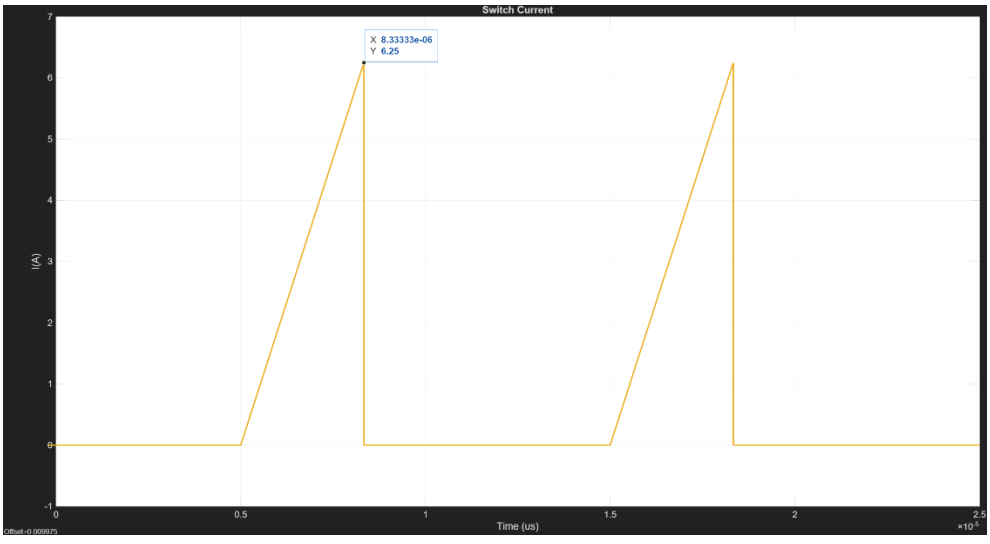

Figure 4.8- Switch current

Results from this steady-state simulation confirm that the boost converter operates correctly: the output voltage settles at about 72 V, boosting the 48 V input evidenced by the inductor voltage swinging between 48 V and -24 V. The inductor current waveform successfully verifies the design requirements through oscillations between a peak of approximately 6.25 A and a minimum of exactly 0 A, hence confirming explicitly that the converter operates in BCM. In the off-state, the switch voltage stresses appropriately to the 72 V output voltage level, while during the on-state, it carries inductor current; similarly, the diode conducts current to the load when the switch is off. Furthermore, the output voltage ripple is observed to be approximately 0.464 V peak-to-peak with a characteristic triangular shape that shows periodic charging and discharging of the output capacitor in steady state.

c)

$$V_{L(on)} = V_{in} - I_L \cdot r$$

$$V_{L(off)} = V_{in} - I_L \cdot r - V_{out}$$

Volt-Second balance applied:

$$\langle V_L \rangle = D \cdot V_{L(on)} + (1-D) \cdot V_{L(off)} = 0$$

$$D(V_{in} - I_L r) + (1-D)(V_{in} - I_L r - V_{out}) = 0$$

$$V_{in} - I_L r - (1-D)V_{out} = 0$$

$$V_{in} = (1-D)V_{out} + I_L r \quad \text{— (Eq. 1)}$$

Relating inductor current with output voltage:

$$I_{diode(avg)} = I_{out}$$

$$I_{diode(avg)} = (1-D) \cdot I_L$$

$$I_L = \frac{I_{out}}{1-D} = \frac{V_{out}}{R_{load}(1-D)} \quad \text{— (Eq. 2)}$$

Substitute Eq.2 to Eq.1:

$$V_{in} = (1-D)V_{out} + \left[\frac{V_{out}}{R_{load}(1-D)}\right] \cdot r$$

$$\frac{V_{in}}{V_{out}} = (1-D) + \frac{r}{R_{load}(1-D)}$$

Gain= V_{out}/V_{in}

$$\frac{V_{out}}{V_{in}} = \frac{1-D}{(1-D)^2 + \frac{r}{R_{load}}}$$

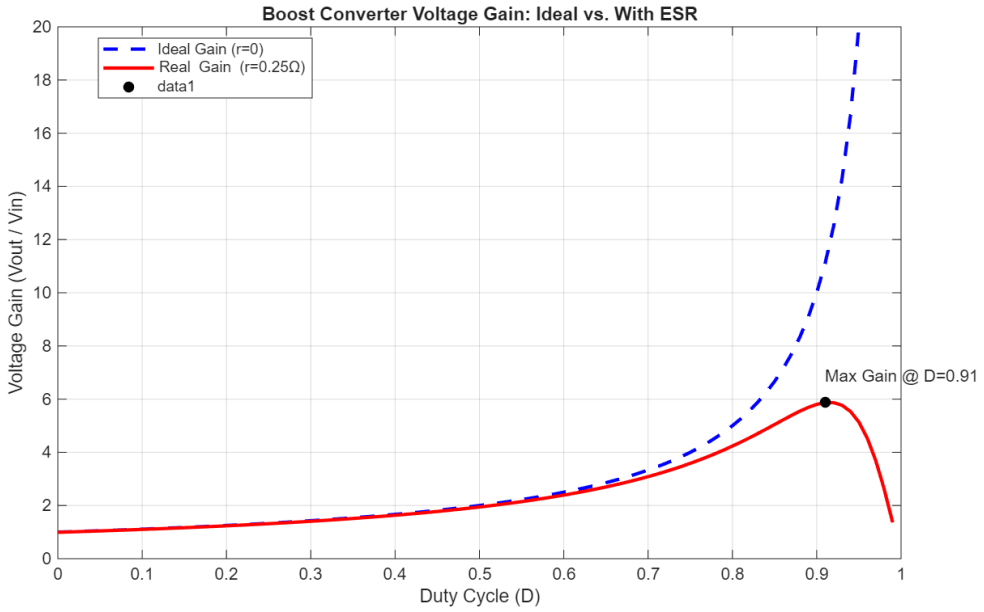

Figure 4.-Voltage gain with and without ESR of the inductor as a function of D

The analysis of the voltage gain as a function of the duty cycle reports an evident deviation between the ideal theoretical model and the practical system including inductor ESR (r_L = 250 $m\Omega$). In the low duty cycle area (D < 0.5), the inductor current is relatively low, hence the resistive drop (I_L*r_L) is negligible, and the real gain curve follows well the ideal asymptotic response. When the duty cycle approaches unity, the required inductor current grows exponentially. This brings resistive losses ($I_{rms}^{2*}r_L$) to dominate the system dynamics and also introduces energy dissipation in the inductor. Hence, the output voltage cannot increase indefinitely. Therefore, differently from the ideal model, where the gain goes to infinity, the practical gain reaches only a maximum peak of around 6 at a critical duty cycle of D≈0.91, beyond which the voltage gain drastically drops due to excessive parasitic losses.

d)

$$P_{out} = I_{out}^2 \cdot R_{load}$$

$$P_{loss} = I_{rms}^2 \cdot r \approx I_L^2 \cdot r \quad \text{(Assuming small ripple)}$$

$$I_{out} = I_{diode\_avg} = (1 - D) \cdot I_L$$

$$I_L = \frac{I_{out}}{1 - D}$$

Efficiency is:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}}$$

$$\eta = \frac{I_{out}^2 R_{load}}{I_{out}^2 R_{load} + I_L^2 r}$$

$$\eta = \frac{I_{out}^2 R_{load}}{I_{out}^2 R_{load} + \left(\frac{I_{out}}{1-D}\right)^2 r}$$

$$\eta = \frac{R_{load}(1 - D)^2}{R_{load}(1 - D)^2 + r}$$

$$\eta = \frac{(1-D)^2}{(1-D)^2 + \frac{r}{R_{load}}}$$

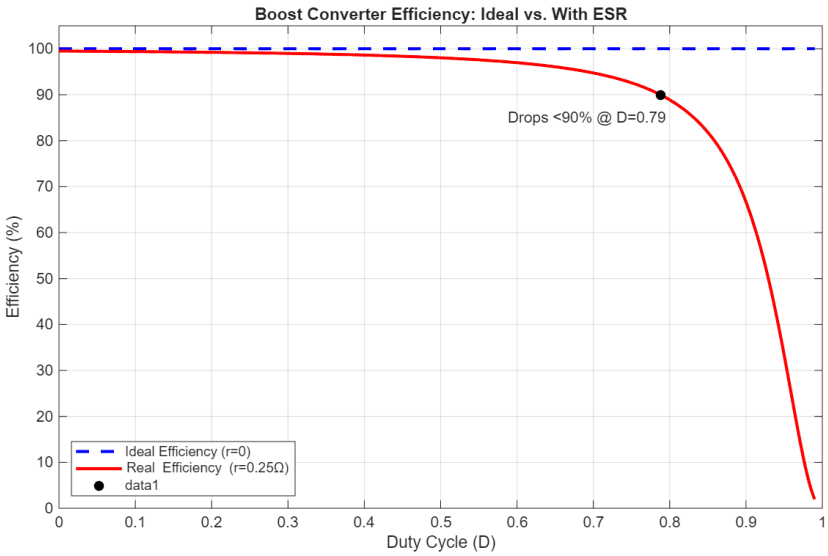

Figure 4.- Efficiency with and without ESR as a function of D

The comparative analysis of the boost converter efficiency contrasts sharply between the theoretical ideal model and the practical implementation including inductor ESR (r_L = 250 mΩ). While the ideal model predicts a constant 100% efficiency across the full duty cycle range (0<D < 1), the incorporation of parasitic resistance unmasks a nonlinear degradation in performance. For low values of the duty cycle (D < 0.5), the efficiency curve stays close to the ideal limit since the inductor current is small, hence the I^2*R losses will be minimal. In contrast, for duty cycles approaching unity, the required inductor current increases asymptotically (I_L proportional to 1/(1-D)), and with this, the resistive power losses grow quadratically. As a result, at large values of the duty cycle, the real efficiency deviates notably from the ideal line, falling below useful levels (D<50%) near the point of maximum gain, showing that parasitic elements impose a hard limit on the feasible operating range of the converter.

I added the codes for the part c and d to appendix.

Conclusion

This overall analysis, from basic characteristics of the diode and MOSFET to their use in buck and boost converter designs, will demonstrate how device parameters fundamentally influence converter performance, efficiency, and operating limits. With obvious differences between silicon, Schottky, and SiC technologies, increasing voltage and current ratings is invariably linked with trade-offs in forward losses, switching behavior, thermal performance, and cost, where proper device selection becomes indispensable for reliable operation. Simulated buck and boost converters confirm the theoretical predictions: conditions for CCM and BCM, expected ripple behaviors, and also the impact of parasitic elements such as inductor ESR on voltage gain and efficiency. Finally, the soft-start implementation eliminates harmful inrush currents effectively, emphasizing the importance of control strategies besides component selection. In general, this work emphasizes that high-performance power conversion can only be achieved with proper balancing of semiconductor physics, converter topology, and practical non-idealities.

APPENDIX

Part c)

```
% Parameters
r = 0.250;       % Inductor ESR in Ohms (250 mOhm)
R_load = 34.56;     % Load Resistance in Ohms (Assumed)
D = 0:0.01:0.99; % Duty Cycle vector (0 to 95%)

% 1. Ideal Gain Calculation (r = 0)
% Formula: 1 / (1-D)
Gain_Ideal = 1 ./ (1 - D);

% 2. Non-Ideal Gain Calculation (with ESR)
% Formula Derived above
ratio = r / R_load;
Gain_Real = (1 - D) ./ ( (1 - D).^2 + ratio );

% Plotting
figure;
plot(D, Gain_Ideal, 'b--', 'LineWidth', 2); hold on;
plot(D, Gain_Real, 'r-', 'LineWidth', 2);
grid on;

% Formatting
title('Boost Converter Voltage Gain: Ideal vs. With ESR');
xlabel('Duty Cycle (D)');
ylabel('Voltage Gain (Vout / Vin)');
legend('Ideal Gain (r=0)', ['Real Gain (r=' num2str(r) '\Omega)']);
xlim([0 1]);
ylim([0 20]); % Limiting Y-axis to see the divergence clearly

% Mark the maximum point of the real curve
[max_gain, max_idx] = max(Gain_Real);
plot(D(max_idx), max_gain, 'ko', 'MarkerFaceColor', 'k');
text(D(max_idx), max_gain+1, sprintf('Max Gain @ D=%.2f', D(max_idx)));
```

Part d)

```
% Parameters
r = 0.250;       % Inductor ESR in Ohms
R_load = 50;     % Load Resistance in Ohms
D = 0:0.001:0.99; % Duty Cycle vector

% 1. Ideal Efficiency Calculation (r = 0)
% Efficiency is always 100% (or 1)
Eff_Ideal = ones(size(D));

% 2. Real Efficiency Calculation (with ESR)
% Derived Formula: 1 / ( 1 + r / (R_load * (1-D)^2) )
ratio = r / R_load;
Eff_Real = 1 ./ ( 1 + ratio ./ ((1 - D).^2) );

% Plotting
figure;
plot(D, Eff_Ideal * 100, 'b--', 'LineWidth', 2); hold on; % Ideal (Blue Dashed)
plot(D, Eff_Real * 100, 'r-', 'LineWidth', 2);           % Real (Red Solid)
grid on;

% Formatting
title('Boost Converter Efficiency: Ideal vs. With ESR');
xlabel('Duty Cycle (D)');
ylabel('Efficiency (%)');
```

```
legend('Ideal Efficiency (r=0)', ['Real Efficiency (r=' num2str(r) '\Omega)'], 'Location',
'SouthWest');
xlim([0 1]);
ylim([0 105]);

% Mark the drop-off point (e.g., where Efficiency drops below 90%)
idx_90 = find(Eff_Real < 0.90, 1);
if ~isempty(idx_90)
    plot(D(idx_90), Eff_Real(idx_90)*100, 'ko', 'MarkerFaceColor', 'k');
    text(D(idx_90)-0.2, Eff_Real(idx_90)*100-5, sprintf('Drops <90%% @ D=%.2f',
D(idx_90)));
end
```