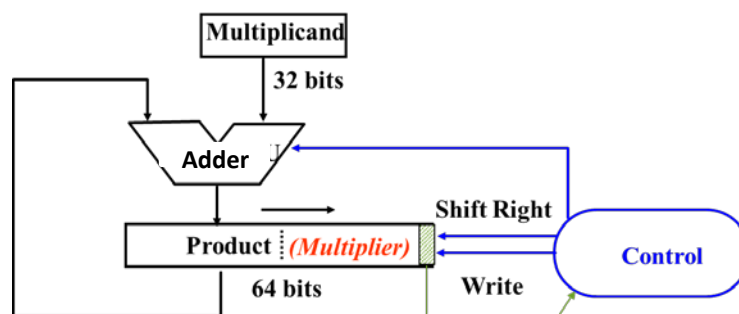# CSE 331/503

Computer Organization

Homework 3 – ALU with Multiplication Design

Due Date 19/12/2020 Sunday 23:59

In this assignment you will design an ALU that is capable of unsigned multiplication using **Quartus** and **Verilog HDL**.

1. mult32.v Module

Your design will have three modules: adder.v, control.v and datapath.v. You will combine them in a mult32.v file to have the 32 bit multiplier.

Your Control Unit (control.v) will implement the below ASM. Design that first drawing your state diagram and finding the Boolean expressions for Next state variables and control signal outputs:
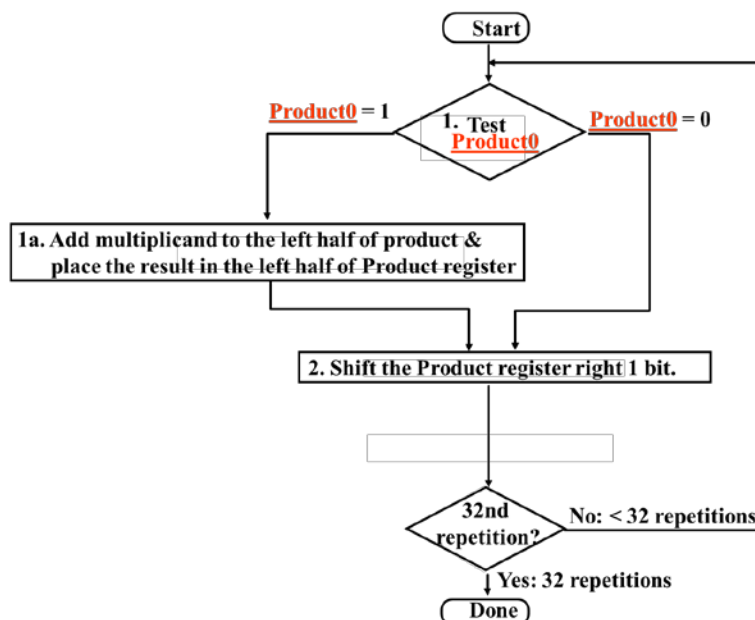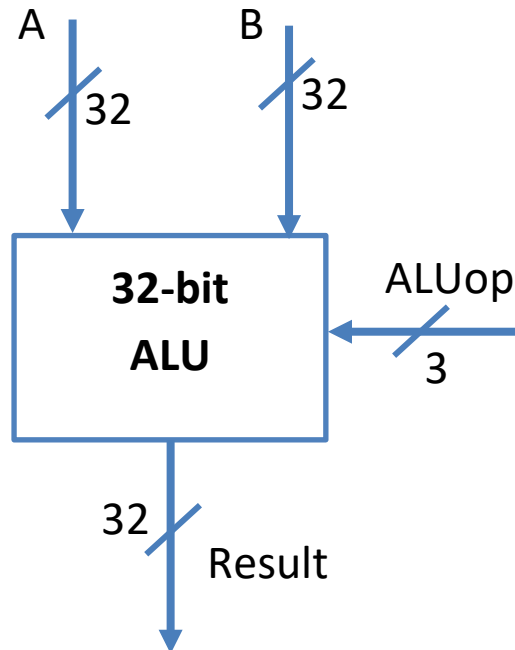
2. `alu32.v` Module

Your ALU will be able to perform addition, subtraction, multiplication, AND, OR, XOR, NOR and Set Less Than operations.

Therefore the **alu32.v** will use **mult32.v** module inside.

ALUop	Operation
000	ADD
001	XOR
010	SUB
011	MULT
100	SLT
101	NOR
110	AND
111	OR

- Write a report showing and explaining all Verilog files, including your schematics.
- **You can only use structural Verilog. Behavioral Verilog is not permitted.**
- **No other operations are permitted. And you cannot change ALUop decisions.**
- Perform simulations and check for accuracy. Not working designs will not get above 30pts. If the mistake is small it is your responsibility to find and correct it.
- Cheating results in -100 even from outer resources if not mentioned in the report.
- **Attend the PS on December 9, 2021!**