National University of Sciences and Technology (NUST)
School of Electrical Engineering and Computer Science

ESE

[EE321: Computer Architecture and Organization]

[22 Aug 2020] [Time Allowed: 150 Minutes]

[BSCS-8A]

Name _____ **Registration #**_____

Signature: _____ **Section:**_____

Instructions

- Closed book, closed notes.
- Clearly write the steps of your solution.
- Invigilators will NOT answer any query, therefore solve whatever you understand.
- Talking to anyone during the exam is strictly prohibited.
- **Using any unfair means** during the exam will result in immediate cancellation of your exam.
- Write in a neat and clean manner.
- Scan all pages of the solved exam and email as a **Single PDF** file.
- Good Luck!

Q1: MCQs --- Q2: Short Answers --- Q3,Q4: Problem Solving

Marks						Total
	Q1 CLO-1	**Q2** CLO-1	**Q3** CLO-2	**Q4** CLO-2		**100**
	20	**30**	**20**	**30**		

Instructor _____
Dr. Khawar Khurshid

Peer Reviewed By____
Dr. Ahmad Salman

PART 1: Objectives

1. The fastest addressing mode is

   (a) Register
   (b) Direct
   (c) Immediate
   (d) Displacement
   (e) None of the above

2. Direct Memory Access (DMA) controller performs the memory operations

   (a) Using the CPU resources
   (b) Independently with its own hardware
   (c) Through operating system
   (d) All of the above

3. Calculating the parity sequence is a

   (a) Arithmetic operation
   (b) Logical operation
   (c) Conversion operation
   (d) None of the above
   (e) All of the above

4. In case of a 'for loop' which branch-handling method is generally better

   (a) Stalling
   (b) Predict always taken
   (c) Predict never taken
   (d) Delayed branch

5. Which of the following sequence of types of instructions cause problems in a pipeline?

   (a) Write after write
   (b) Read after write
   (c) Write after read
   (d) All of the above
   (e) None of the above

6. For a 16-bit binary number how many check bits are required for the Hamming code?

   _____

7. Which of the following are used to select the source or destination of the data?
    a. Data Bus Lines
    b. Control Bus Lines
    c. Address Bus Lines
    d. Both (b) and (c)

8. Top Level view of a Computer System Structure includes:
    a. CPU
    b. Main Memory
    c. I/O
    d. All of the above

9. In case of a Set Associative Cache, a block of memory may reside in:
    a. any cache line of a particular set
    b. in a predetermined line in any of the available set
    c. in any line of any set
    d. only (a) and (b) are correct

10. Which of the following is valid for Disks and Tape Drives?
    (a) From structural point of view, categorized as Machine Readable I/O Devices.
    (b) From architectural point of view, communication devices
    (c) From functional point of view, they form part of Memory Hierarchy
    (d) (a) and (c)

PART 2: Short Questions

1. Explain the difference between the Write Back policy and the Write Through policy. (3)

2. Describe Spatial locality and Temporal Locality with examples. (3)

3. How can the Structural Hazard be avoided in pipelined architecture? (4)

4. Assume an instruction set that uses a fixed 16-bit instruction length. Operand specifiers are 6 bits in length. What is the maximum number of instruction possible for the following? (4)

- Zero operand - One operand - Two Operand

5. For an 8-bit word 00111001, the check bits stored are 0111. Suppose when the word is read from the memory, the check bits are calculated to be 0010. What is the data word that was read from the memory? (5)

6. Draw the diagram for the following address calculation: (5)

EA = (R1 + (M))

7. A non-pipelined processor has a clock rate of 4.0 GHz and average cycles per instruction (CPI) equal to 3. Another processor has a six-stage pipeline with a clock rate of 2.0 GHz. Assuming there are no branches or exceptions, (6)

(a) Calculate and show which processor can execute a 1000 instruction program faster?
(b) What is the speed up factor?

PART 3: Problem Solving

Question 3:

(a) The following MIPS program is to be run on a MIPS pipeline processor of the form IF-ID-EX-MEM-WB. Please identify **all data dependencies** beside each instruction, in the form: <type of dependency> on <register> from <line-no> to <line-no>, e.g. WAW on R10 from Line 20 to Line 18.

Line 1: lw R2, 60(R1)

Line 2: lw R1, 40(R2)

Line 3: add R1, R1, R2

Line 4: sw R1, 20(R2)

(b) Work out and draw the optimal pipeline using forwarding (whenever the data is available) to any other stage, then compute the average cycles per instruction (CPI) for this pipeline.

Question 4:

Samsung has implemented a system design, and it has a known execution in **600 seconds**.

(a) Apple proposes a single cycle solution, and plans to use a compiler that will generate 300 Billion instructions per execution. How fast does Apple need to make its clock cycle in order to make the program run faster than Samsung's?

(b) Google proposes a pipelined data path, with a clock period of 1.2 ns. Its compiler will generate 400 Billion instructions. Of these 400 Billion instructions, 25% are loads, and 20% are branches. 40% of all loads cause a 2-cycle load-use stall. Also. the penalty for a mis-predicted branch is 5 cycles. The processor does not suffer from any other stalls. How accurate does Google's branch predictor need to be in order to make the program run faster than Samsung's?

Note: You need to figure out the information of total number of instructions for program execution, each instruction requires 1 clock cycle (plus any stalls mentioned above), and the time required for one clock cycle.