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BJT As Small Signal Low Frequency Amplifier

7.1 Introduction

We have seen that V-I characteristics of an active device such as BJT are non-linear. The analysis of a non-linear device is complex. Thus to simplify the analysis of the BJT, its operation is restricted to the linear V-I characteristics around the Q-point i.e. in the active region. This approximation is possible only with small input signals. With small input signals the transistor can be replaced with small signal linear model. This model is also called **small signal equivalent circuit**.

We know that the reactance of the capacitance is inversely proportional to the frequency, $Z_C = 1/2\pi f C$. Thus for low frequencies the reactances of junction capacitances of the transistor are very high. Since these junction reactances appear in parallel with junctions, their effect is ignored at low frequencies and transistor analysis is further simplified. Therefore, in this chapter we examine the BJT as **small signal low frequency amplifier**.

7.2 Transistor as an Amplifier

An amplifier is used to increase the signal level; i.e. the amplifier is used to get a larger signal output from a small signal input. We will assume a sinusoidal signal at the input of the amplifier. At the output, signal must remain sinusoidal in waveform, with frequency same as that of the input.

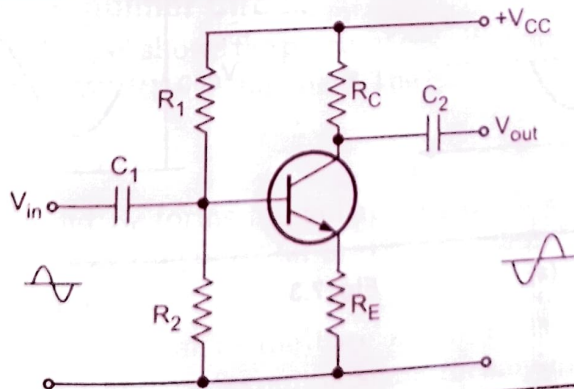


Fig. 7.1 Common emitter amplifier

To make the transistor work as an amplifier, it is to be biased to operate in the active region, i.e. base-emitter junction is to be forward biased, while base-collector junction to be reversed biased.

Let us consider the common emitter amplifier circuit using self bias or voltage divider bias as shown in the Fig. 7.1

In the absence of input signal, only dc voltage are present in the circuit. This is known as zero-signal or no-signal condition or quiescent condition for the amplifier. The dc collector-emitter voltage, V_{CE} , the dc collector current I_C and dc base current I_B is the quiescent operating point for the amplifier. On this dc quiescent operating point, we superimpose ac signal by application of ac sinusoidal voltage at the input. Due to this base current varies sinusoidally, as shown in Fig. 7.2.

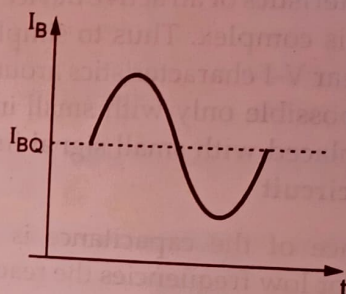


Fig. 7.2 I_{BQ} is quiescent DC base current

Since the transistor is biased to operate in the active region, the output is linearly proportional to the input. The output current i.e. the collector current is β times larger than the input base current in common emitter configuration. Hence the collector current will also vary sinusoidally about its quiescent value, I_{CQ} . The output voltage will also vary sinusoidally as shown in the Fig. 7.3 (a) and 7.3 (b).

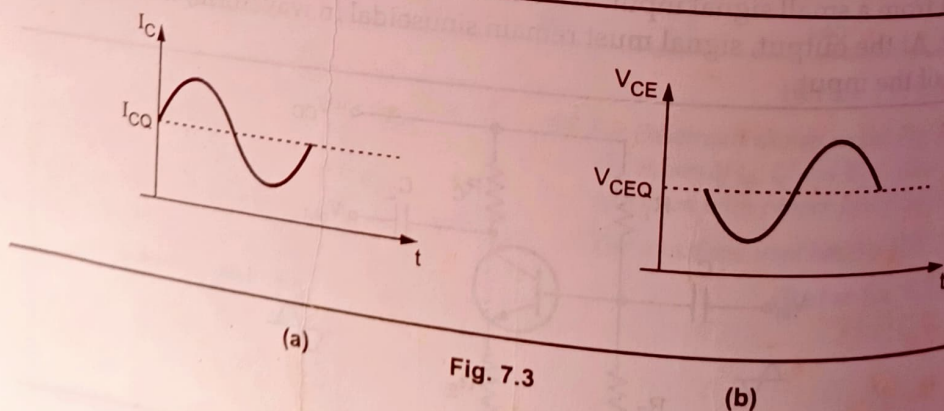


Fig. 7.3

Fig. 7.3 (c) Graph

Then variations due to change in I_B are shown in Fig. 7.3. The collector current, and the output voltage, are 180° out-of-phase with I_B .

When one cycle means the frequency of the input signal. Thus in the amplifier, the magnitude of the output is β times the magnitude of the input.

7.2.1 Common Emitter Amplifier

Fig. 7.4 (See Fig. 7.1) shows a common emitter amplifier. It consists of the following components:

1. Biasing Circuit

The resistances R_1 and R_2 are used for biasing the amplifier. It sets the operating point.

2. Input Capacitor

This capacitor is used to couple the input signal to the amplifier. It is present in the input circuit to provide the required biasing conditions.

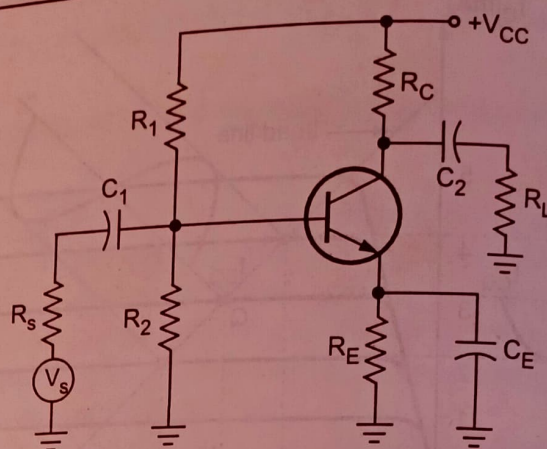


Fig. 7.4 Practical common emitter amplifier circuit

3. Emitter Bypass Capacitor C_E

An emitter bypass capacitor C_E is connected in parallel with the emitter resistance, R_E to provide a low reactance path to the amplified ac signal. If it is not inserted, the amplified ac signal passing through R_E will cause a voltage drop across it. This will reduce the output voltage, reducing the gain of the amplifier.

4. Output Coupling Capacitor C_2

The coupling capacitor C_2 couples the output of the amplifier to the load or to the next stage of the amplifier. It blocks dc and passes only ac part of the amplified signal.

7.2.1.1 Need for C_1 , C_2 and C_E

We know that, the impedance of capacitor is given as

$$X_C = \frac{1}{2\pi fC}$$

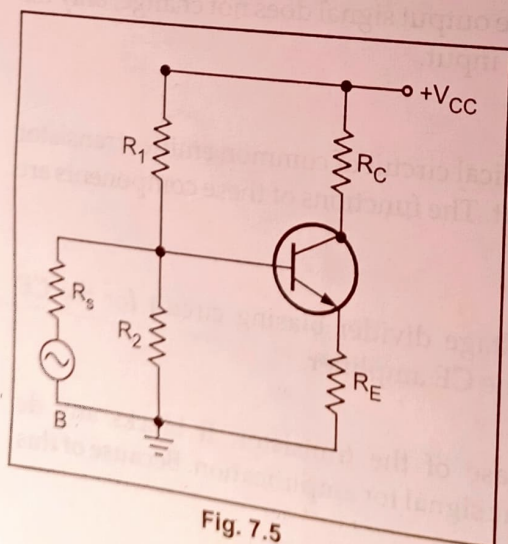


Fig. 7.5

Thus, at signal frequencies all the capacitors have extremely small impedance and it can be treated as an ac short circuit. For bias/dc conditions of the transistor all the capacitors act as a dc open circuit. With this knowledge we will see the importance of C_1 , C_2 and C_E .

Consider that the signal source is connected directly to the base of the transistor as shown in Fig. 7.5.

Looking at the Fig. 7.5 we can immediately notice that source resistance R_s is in parallel with R_2 . This will reduce the bias voltage at the transistor base and, consequently alter the

collector current I_C and V_{CE} will be. capacitors are used to maintain a dc, maintain the advantage of the signal is routed.

The emitter resistor R_E provides a low swing.

For the proper operation, the dc voltage level must be grounded through the emitter with respect to

7.2.1.2 Phase

The phase shift is considered. The positive half-cycle of the input voltage, a positive voltage is applied to the junction. This causes the collector current to increase, hence the collector voltage $V_C = V_{CC} - I_C R_C$ decreases. Since $V_C = V_{CC}$ is constant. Thus, we get negative

In the negative half-cycle, the input voltage is negative, the base-emitter junction is reverse biased, the drop across R_C is zero, and the output voltage is zero. The shift of 180° between the input and output is observed.

7.2.2 Common

The Fig. 7.6 shows the common emitter amplifier. The load resistor R_L is connected to the collector.

When a signal is applied to the base, the signal goes to the emitter and emitter current $I_E = I_B + I_C$ is developed.

collector current, which is not desired. Similarly, by connecting R_L directly, the dc levels of V_C and V_{CE} will change. To avoid this and maintain the stability of bias condition coupling capacitors are connected. As mentioned earlier, coupling capacitors act as open circuits to dc, maintain stable biasing conditions even after connection of R_s and R_L . Another advantage of connecting C_1 is that any dc component in the signal is opposed and only ac signal is routed to the transistor amplifier.

The emitter resistance R_E is one of the component which provides bias stabilization. But it also reduces the voltage swing at the output. The emitter bypass capacitor C_E provides a low reactance path to the amplified a.c. signal increasing the output voltage swing.

For the proper operation of the circuit, polarities of the capacitors must be connected correctly. The curve bar which indicates negative terminal must always be connected at a dc voltage level lower than (or equal to) the dc level of the positive terminal (straight bar). For example, C_1 in Fig. 7.4 has its negative terminal at dc ground level, because it is grounded through the signal source resistance R_s . The positive terminal of C_1 is at $+V_B$ with respect to ground.

7.2.1.2 Phase Reversal

The phase relationship between the input and output voltages can be determined by considering the effect of a positive half cycle and negative half cycle separately. Consider the positive half cycle of input signal in which terminal A is positive w.r.t. B. Due to this, two voltages, ac and dc will be adding each other, increasing forward bias on base emitter junction. This increases base current. The collector current is β times the base current, hence the collector current will also increase. This increases the voltage drop across R_C . Since $V_C = V_{CC} - I_C R_C$, the increase in I_C results in a drop in collector voltage V_C , as V_{CC} is constant. Thus, as V_i increases in a positive direction, V_o goes in a negative direction and we get negative half cycle of output voltage for positive half cycle at the input.

In the negative half cycle of input, in which terminal A becomes negative w.r.t. terminal B, the ac and dc voltages will oppose each other, reducing forward bias on base-emitter p-n junction. This reduces base current. Accordingly collector current and drop across R_C both reduce, increasing the output voltage. Thus, we get positive half cycle at the output for negative half cycle at the input. Therefore, we can say that there is a phase shift of 180° between input and output voltages for a common emitter amplifier.

7.2.2 Common Collector Amplifier Circuit

The Fig. 7.6 shows common collector circuit. The dc biasing is provided by R_1 , R_2 and R_E . The load resistance is capacitor coupled to the emitter terminal of the transistor.

When a signal is applied via to the base of the transistor, V_B is increased and decreased as the signal goes positive and negative, respectively. Looking at Fig. 7.6 we can write that $V_E = V_B - V_{BE}$. Considering V_{BE} fairly constant, we say that variation in the V_B appears at $V_E = V_B - V_{BE}$. emitter voltage V_E will vary same as base voltage V_B . Since the emitter is

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output terminal, it can be noted that the output voltage from a common collector circuit is the same as its input voltage. In other words, we can say that in common collector circuit emitter terminal follows the signal voltage applied to the base. Hence the common collector circuit is also known as an **emitter follower**.

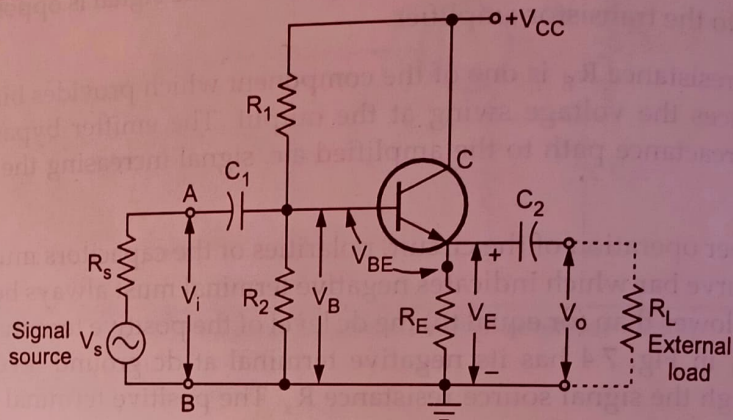


Fig. 7.6 Common collector circuit

7.2.3 Common Base Amplifier Circuit

Fig. 7.7 shows common base circuit. The signal source is coupled to the emitter of the transistor via C_1 . The load resistance R_L is coupled to the collector of the transistor via C_2 .

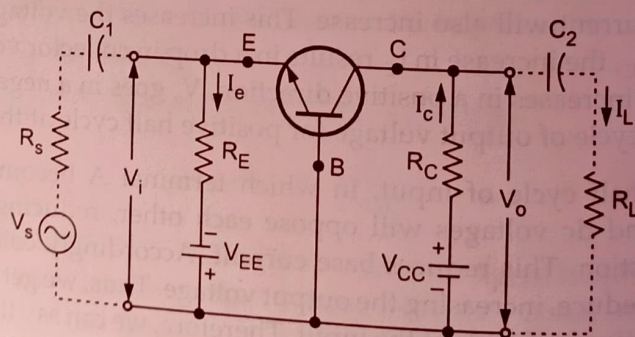


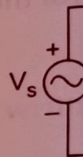
Fig. 7.7 Common base circuit

The positive going pulse of input source increases the emitter voltage. As base voltage is constant, the forward bias of emitter base junction reduces. This reduces I_b , reducing I_c and hence the drop across R_C . Since $V_o = V_{CC} - I_c R_C$, the reduction in I_c results in an increase in V_o . Therefore, we can say that positive going input produces positive going output and similarly negative going input produces negative going output and there is no phase shift between input and output in a common base amplifier.

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7.3 General Characteristics

The amplifier is connected to the input and output terminals, as shown in Fig. 7.8.



The signal to be amplified is applied to the input terminal. The output signal is taken from the output terminal. The signal source is assumed to be at some fixed or variable frequency.

The signal is a low level signal. The output signal is a high level signal. The amplifier is a relay in which the input signal is enlarged version of the input signal. The input and output signal are in phase. The amplifier is a relay in which the input signal is enlarged version of the input signal. The input and output signal are in phase. The amplifier is a relay in which the input signal is enlarged version of the input signal. The input and output signal are in phase.

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Referring to Fig. 7.8,

V_s :

R_s :

V_i :

I_1 :

V_2 :

I_2 :