10

FET SMALL SIGNAL ANALYSIS

10.1 Introduction

Field effect transistor amplifiers provide an excellent voltage gain with the added advantage of a high input impedance. There are three basic FET circuit configurations : Common source, common drain, and common gate. These are similar to the bipolar transistor common emitter, common collector and common base circuits, respectively. The only difference is that BJT controls a large output (collector) current by means of a relative small input (base current), whereas, FET controls an output (drain) current by means of small input (gate) voltage. It is important to note that in both the cases the output current is the controlled variable.

In this chapter we are going to study low frequency equivalent circuit and analysis of common source and common drain amplifiers. Later part of this chapter is devoted to high frequency equivalent circuit of FET.

10.2 JFET as an Amplifier

Field-effect transistor amplifier circuits use the voltage-controlled nature of the JFET. In the pinch-off region, I_D depends (approximately) only on V_{GS}.

Let us discuss the use of the JFET as an amplifier by considering the common-source circuit, shown in the Fig. 10.1.

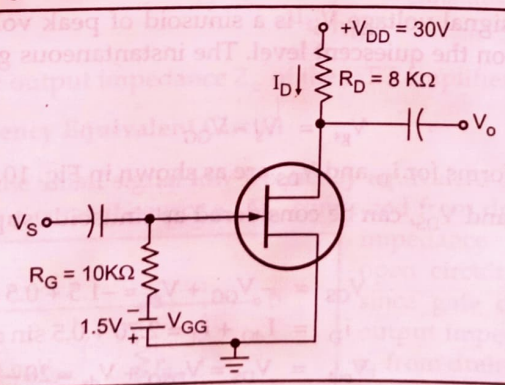

Fig. 10.1 Common source circuit

The voltage V_{GG} provides the necessary reverse-bias between gate and source of the JFET. The signal to be amplified is V_s. The volt-ampere characteristics of the JFET is as shown in Fig. 10.2.

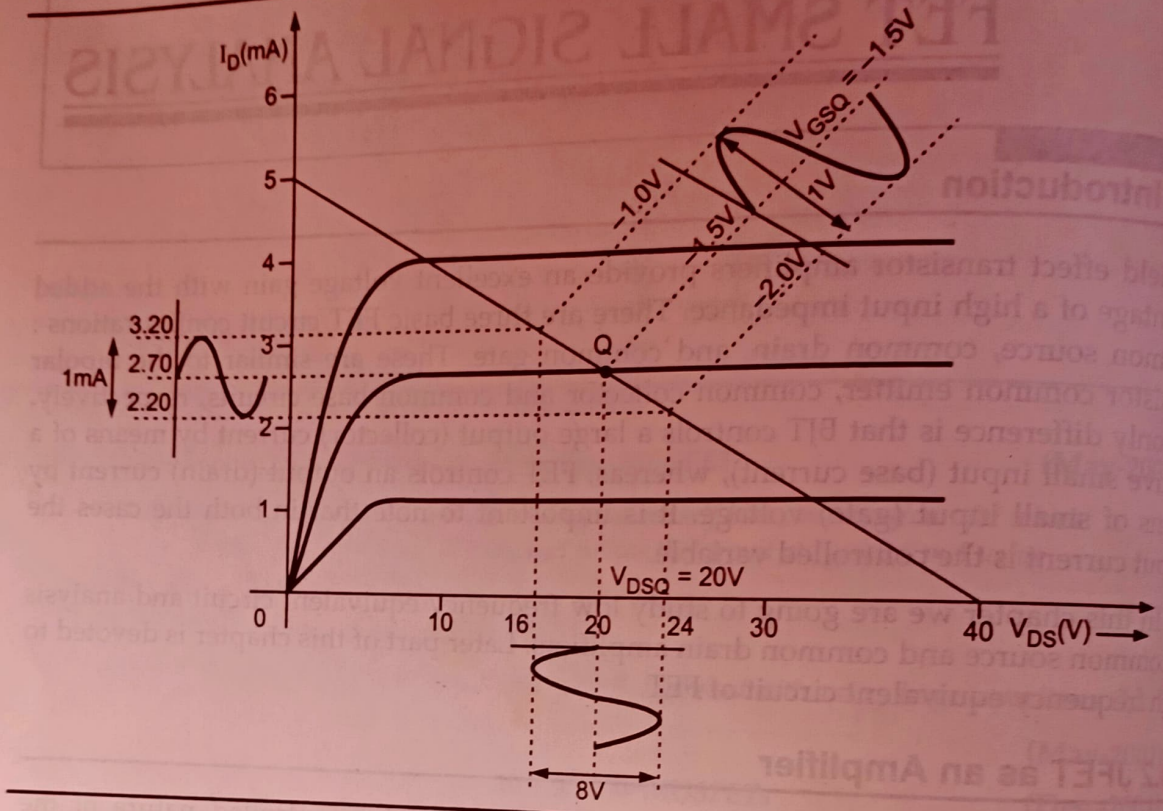

Fig. 10.2 Volt-ampere characteristics of JFET

On the output characteristics, a load line corresponding to $V_{DD} = 40$ V and $R_D = 8\ k\Omega$ is constructed. The transistor is biased at point Q and results in $V_{DSQ} = 20$ V and $I_{dSQ} = 2.70$ mA.

Assuming that the signal voltage V_s is a sinusoid of peak voltage $V_m = 0.5$ V, this signal is superimposed on the quiescent level. The instantaneous gate-to source voltage is

$$V_{gs} = V_s - V_{GG}$$

The resulting waveforms for i_D and V_{DS} are as shown in Fig. 10.2.

Both quantities, i_D and V_{DS}, can be considered as sinusoids superimposed on the dc values.

Then

$$V_{GS} = -V_{GG} + V_{gs} = -1.5 + 0.5 \sin \omega t$$

$$i_D = I_{dQ} + i_d = 2.70 + 0.5 \sin \omega t \quad \text{mA}$$

$$V_{out} = V_{DS} = V_{DSQ} + V_{ds} = 20 - 4 \sin \omega t$$

We observe that the output signal is greater than the input signal, thus indicating amplification.

The magnitude of the voltage gain $|A_v|$ is the ratio of the output ac signal amplitude [4.0 V] to the input ac signal amplitude [0.5 V]. Then, in this example,

$$|A_v| = \frac{4.0}{05} = 8$$

Note that the quiescent operating point Q is selected to be approximately the midpoint of the load line. This gives undistorted output, i.e. output waveform is sinusoidal when the input signal is sinusoidal. If the operating point is selected either close to the ohmic region or near the pinch-off voltage, i.e. at the one of the ends of the load line, the output sinusoid would be clipped during either the positive or negative half-cycles of the input signal. In case of common-source circuit of JFET, there is a phase shift of 180° between the input and output sinusoidal voltages.

10.3 JFET Low Frequency Small Signal Model

The JFET parameters are the major components of low frequency small signal model for JFET. Hence before examining the low frequency small signal model we recall the JFET parameters that we have studied earlier in chapter 8.

We know, that drain to source current of JFET is controlled by gate to source voltage. The change in the drain current due to change in gate to source voltage can be determined using the transconductance factor g_m. It is given as

$$\Delta I_d = g_m \Delta V_{GS} \quad \ldots (10.1)$$

We know that, in BJT the relation between an output and input quantity is given by amplification factor β, whereas in JFET this relation is given by transconductance factor g_m.

The another important parameter of JFET is drain resistance r_d. It is given by

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}} = \text{constant} \quad \ldots . (10.2)$$

It determines the output impedance Z_o of the JFET amplifier.

JFET Low Frequency Equivalent Circuit

Fig. 10.3 shows the small signal low frequency equivalent circuit. The relation of I_d by V_{gs} is included as a current source $g_m V_{gs}$ connected from drain to source. The input impedance is represented by the open circuit at its input terminals, since gate current I_G is zero. The output impedance is represented by r_d from drain to source.

Note that lower case subscripts represent ac levels.

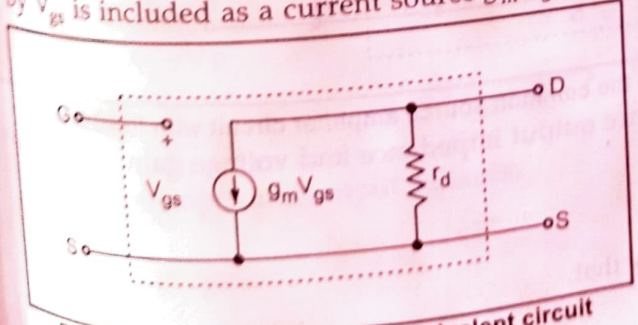

Fig. 10.3 JFET low frequency equivalent circuit

10.4 Common Source Circuit

In common source amplifier circuit input is applied between gate and source and output is taken from drain and source. In the following sections we see the low frequency equivalent circuits for common source configuration with different biasing techniques.

10.4.1 JFET with Fixed Bias

Fig. 10.4 shows common source amplifier with fixed bias. The coupling capacitor C_1 and C_2 which are used to isolate the dc biasing from the applied ac signal, act, as a short circuits for the ac analysis.

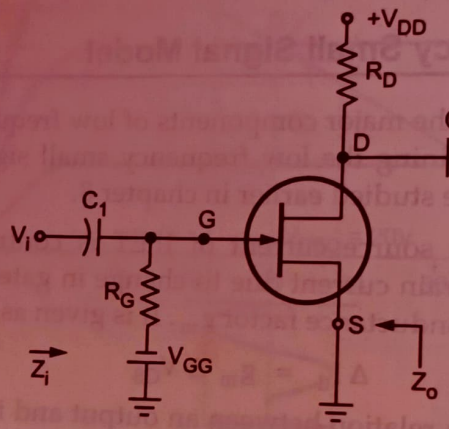

Fig. 10.4 Common source JFET amplifier with fixed bias

Fig. 10.5 shows the low frequency equivalent model for the common source amplifier circuit with fixed bias. It is drawn by replacing :

- All capacitors and dc supply voltages with short circuits. and,
- JFET with its low frequency equivalent circuit.

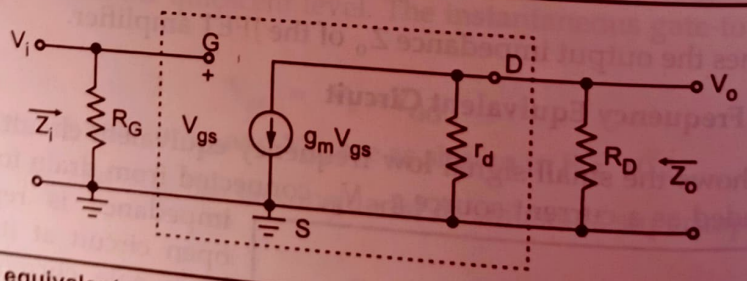

Fig. 10.5 ac equivalent model for the common source amplifier circuit with fixed bias

Now, we see the input impedance output impedance and voltage gain of the above model.

Input impedance Z_i :

Looking into Fig. 10.5 we can say that,

$$Z_i = R_G \qquad \ldots (10.3)$$

Output Impedance Z_o :

The output impedance Z_o is the impedance measured looking from the output side with input voltage (V_i) equal to 0. As $V_i = 0$

$V_{gs} = 0$ and hence $g_m V_{gs} = 0$.

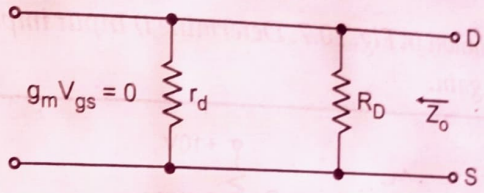

Fig. 10.6

The $g_m V_{gs} = 0$ allows current source to be replaced by an open circuit, as shown in the Fig. 10.6. Therefore the output impedance is

$$Z_o = R_D \,||\, r_d \qquad \ldots (10.4)$$

If the resistance r_d is sufficiently large compared to R_D then we say that the output impedance is approximately equal to R_D.

$$Z_o \approx R_D \qquad \because r_d >> R_D \qquad \ldots (10.5)$$

Voltage Gain A_v :

$$\text{The voltage gain } A_v = \frac{V_o}{V_i}$$

Looking at Fig. 10.5 we can write

$$V_o = -g_m V_{gs} \,(r_d \,||\, R_D) \qquad \ldots (10.6)$$

As we know $V_i = V_{gs}$ we can write

$$V_o = -g_m V_i \,(r_d \,||\, R_D) \qquad \ldots (10.7)$$

$$\therefore \quad A_v = \frac{V_o}{V_i} \qquad \ldots (10.8)$$

$$= -g_m \,(r_d \,||\, R_D)$$

and if $r_d >> R_D$ $\qquad \ldots (10.9)$

$$A_v \approx -g_m R_D$$

The negative sign in the equation for A_v clearly indicates there is a phase shift of 180° between input and output voltages.

Table 10.1 summarizes performance of common source amplifier with fixed bias.

Parameter	Exact	With $r_d \gg R_D$
Z_i	R_G	R_G
Z_o	$R_D \| r_d$	R_D
A_v	$-g_m (R_D \| r_d)$	$-g_m R_D$

Table 10.1

Ex. 10.1 : *For the circuit shown in Fig. 10.7. Determine i) Input impedance ii) Output impedance and iii) Voltage gain.*

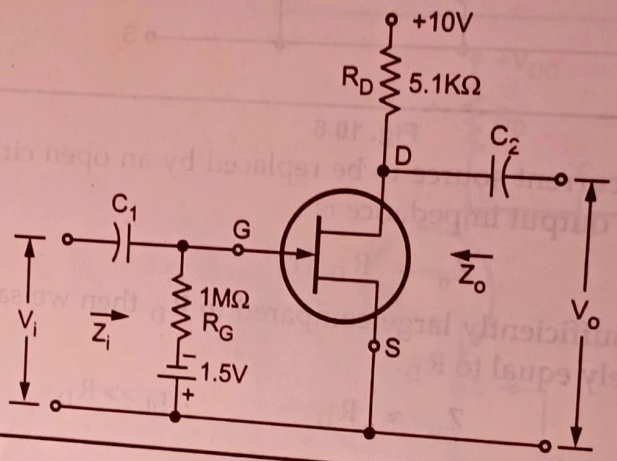

Fig. 10.7

Sol. : i) From equation 10.3 we have

$$Z_i = R_G$$
$$= 1M\Omega$$

ii) From equation 10.4 we have

$$Z_o = r_d \| R_D$$
$$= 50\,K \| 5.1\,K$$
$$= 4628\,\Omega$$

iii) Voltage Gain A_v : From equation 10.8 we have

$$A_v = -g_m (r_d \| R_D)$$
$$= -2\,mS\,(50\,K \| 5.1\,K)$$
$$= -2\,mS\,(4628)$$
$$= -9.256$$