

$$V_{GS} - |V_{DSS}| \geq V_{GS}$$

4.12 FET TREE

The input Z of JFET is much higher compared to a junction transistor. But for MOSFETs, the input Z is much higher compared to JFETs. So these are very widely used in ICs and are fast replacing JFETs.

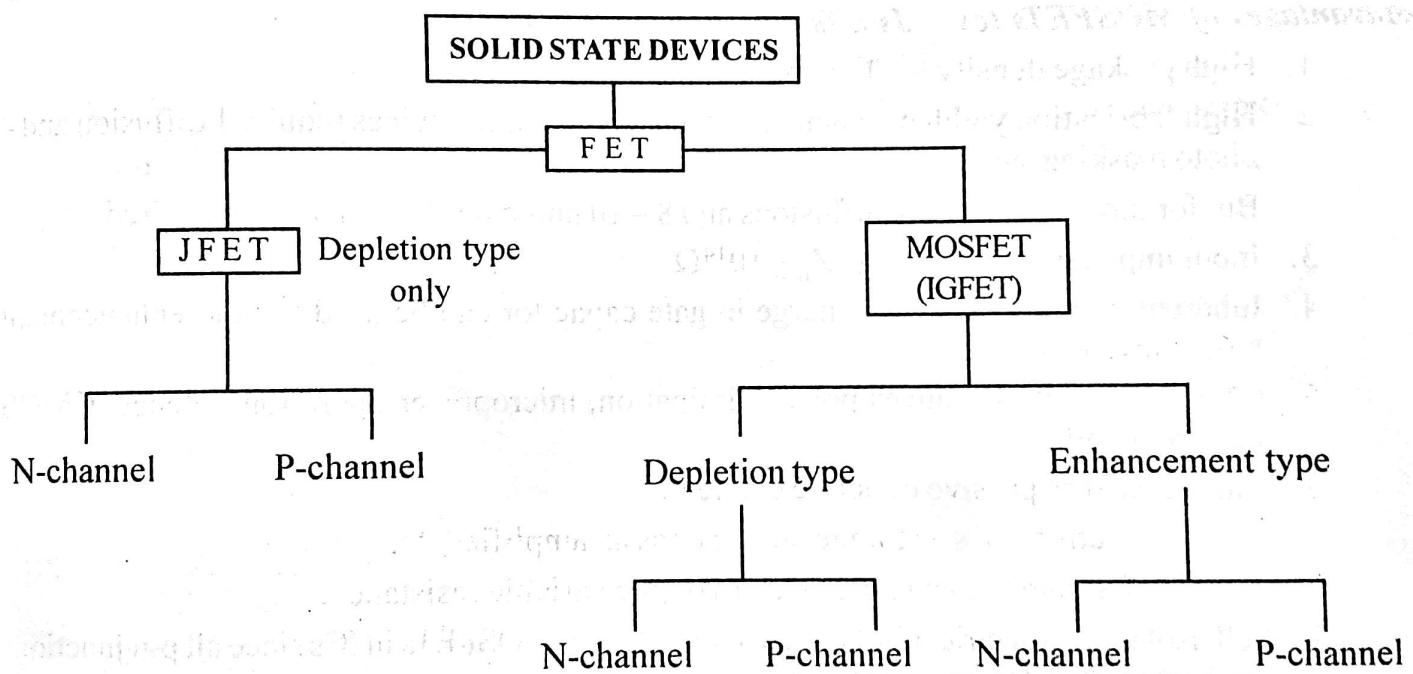
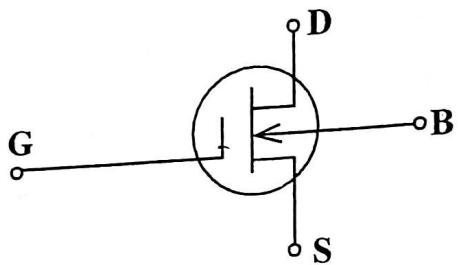


Fig 4.45 FET Tree.

There are two types of MOSFETs, enhancement mode and depletion mode. These devices, derive their name from Metal Oxide Semiconductor Field Effect Transistor (MOSFET) or MOS transistor (See Fig. 4.46). These are also known as IGFET (Insulated Gate Field Effect Transistor). The gate is a metal and is insulated from the semiconductor (source and drain are semiconductor type) by a thin oxide layer.

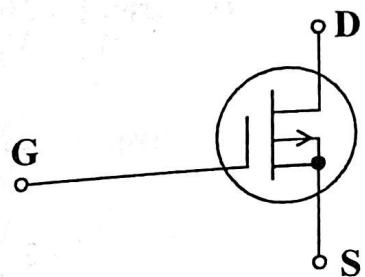
In FETs the gate source junction is a p-n junction. (If the source is n-type, gate will be p-type). But in MOSFETs, there is no p-n junction between gate and channel, but rather a capacitor consisting of metal gate contact, a dielectric of SiO_2 and the semiconductor channel. [two conductors separated by dielectric]. It is this construction which accounts for the very large input resistance of 10^{10} to $10^{15} \Omega$ and is the major difference from the JFET.

The symbols for MOSFETs are,



n-channel MOSFET, depletion type

Fig 4.46



p-channel MOSFET, depletion type

Fig 4.47

Some manufacturers internally connect the bulk to the source. But in some circuits, these two are to be separated (See Fig. 4.46). The symbol, if they are connected together is, given in Fig. 4.47.

for p - channel, the arrow will point outwards.

Bulk is the substrate material taken.

Advantages of MOSFETs (over JFETs and other devices)

1. High package density $\approx 10^5$ components per square cm.
2. High fabrication yield. p - channel Enhancement mode devices require 1 diffusion and 4 photo masking steps.
But for bipolar devices, 4 diffusions and 8 – 10 photo masking steps are required.
3. Input impedance is very high $Z_n \approx 10^{14}\Omega$.
4. Inherent memory storage : charge in gate capacitor can be used to hold enhancement mode devices ON.
5. CMOS or NMOS reduces power dissipation, micropower operation. Hence, CMOS ICs are popular.
6. Can be used as passive or active element.
 - Active : As a storage device or as an amplifier etc.
 - Passive : As a resistance or voltage variable resistance.
7. Self Isolation : Electrical isolation occurs between MOSFETs in ICs since all p-n junctions are operated under zero or reverse bias.

Disadvantage

1. Slow speed switching.
2. Slower than bipolar devices.
3. Stray and gate capacitance limits speed.

4.12.1 ENHANCEMENT TYPE MOSFET

n-channel is induced, between source and drain. So it is called as n-channel MOSFET.

For the MOSFET shown in Fig. 4.48, source and drain are n-type. Gate is Al (metal) in between oxide layer is there. The source and drain are separated by 1 mil. Suppose the substrate is grounded, and a positive voltage is applied at the gate. Because of this an electric field will be directed perpendicularly through the oxide. This field will induce negative charges on the

semiconductor side. The negative charge of electrons which are the minority carriers in the p - type substrate form an inversion layer. As the positive voltage on the gate increases, the induced negative charge in the semiconductor increases. The region below the SiO_2 oxide layer has n-type carriers. So the conductivity of the channel between source and drain increases and so current flows from source to drain through the induced channel. Thus, the drain current is enhanced by the positive gate voltage and such a device is called an *enhancement type MOS*.

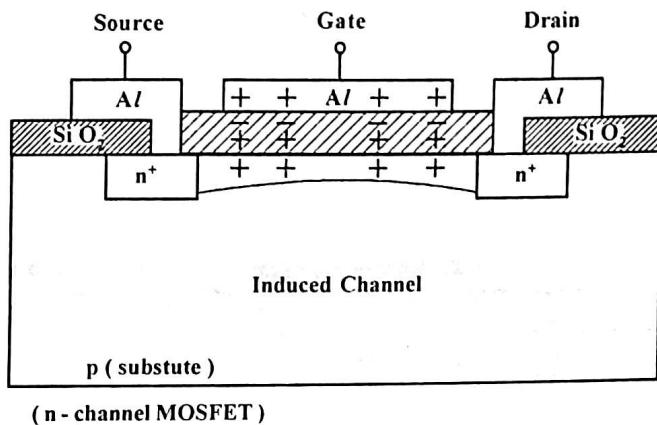
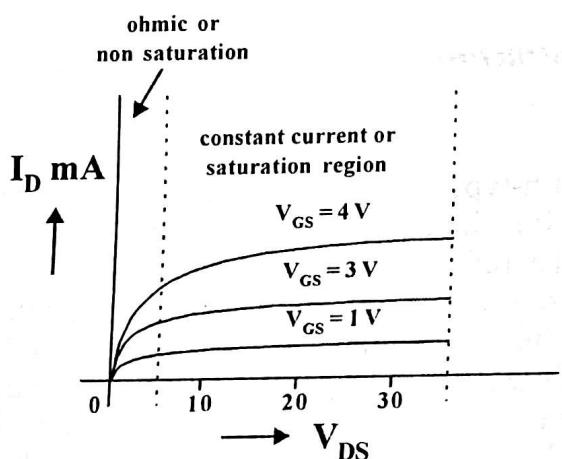
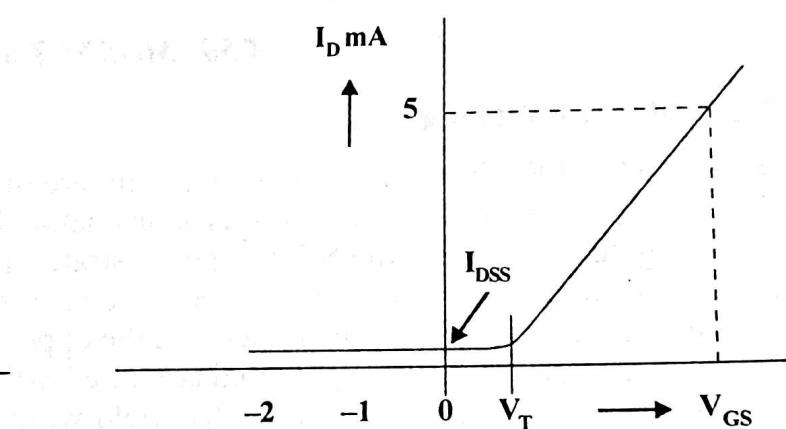


Fig 4.48 n-channel MOSFET

The volt-ampere drain characteristic of an n-channel enhancement mode MOSFET are as shown in Fig. 4.49.



(a) *Drain characteristics*



(b) *Gate characteristics*

Fig 4.49

The current I_D for $V_{GS} \leq 0$ is very small being of the order of few nano amperes. As V_{GS} is made positive, the current I_D increases, slowly first and then much more rapidly with an increase in V_{GS} (Fig. 4.49(b)). Sometimes the manufacturers specify gate, source threshold voltage V_{GST} at which I_D reaches some defined small value $\approx 10\mu\text{A}$. For a voltage $< V_{GST}$, (V_{GS} threshold) I_D is very small. $I_{D(ON)}$ of MOSFET is the maximum value of I_D which remains constant for different values of V_{DS} .

In the ohmic region, the drain characteristic is given by

$$I_D = \frac{\mu C_0 w}{2L} [2(V_{GS} - V_T) V_{DS} - V_{DS}^2]$$

where ,

μ = Majority carriers mobility.

C_0 = Gate capacitance per unit area.

L = Channel length.

w = Channel width perpendicular to C

The ohmic region in the I_D vs V_{DS} characteristic of FET or MOSFET is also known as **triode region**, because like in a triode I_D increases with V_{DS} . The constant current region is known as **pentode region** because the current remains constant with V_{DS} .

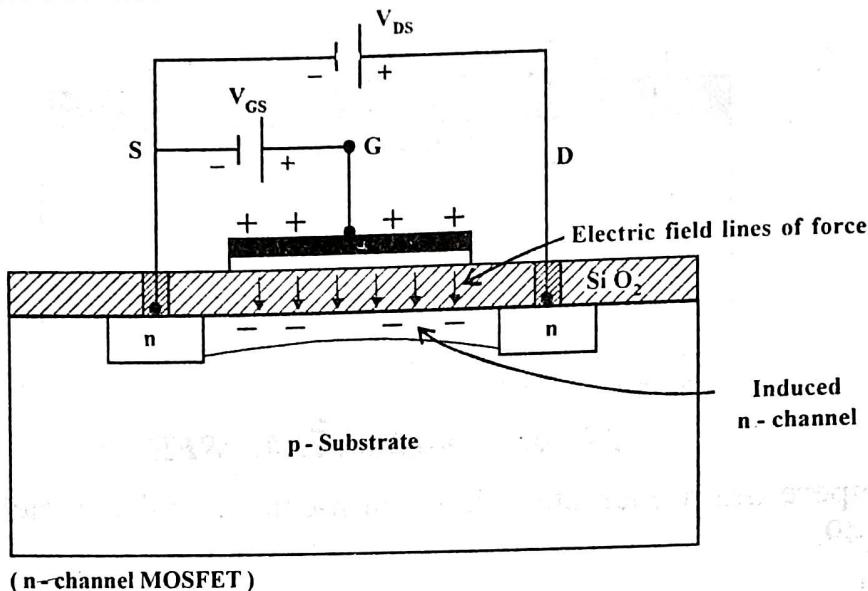


Fig 4.50 MOSFET structure

4.12.2 MOSFET OPERATION

Consider a MOSFET in which source and drain are of n-type. Suppose a negative potential is applied between gate and source. SiO_2 is an insulator. It is sandwiched between two conducting regions the gate (metal) and the S.C p-type substrate. Therefore, equivalent capacitor is formed, with SiO_2 as the dielectric whenever a positive charge is applied to one plate of a capacitor a corresponding negative charge is induced on the opposite plate by the action of the electric field within the dielectric. A positive potential is applied to the gate. So a negative charge is induced on the opposite plate by the action of electric field within the dielectric, in the p - substrate. This charge results from the minority carriers (electrons) which are attracted towards the area below the gate, in the p - type substrate. The electrons in the p - substrate are attracted towards the lower region of SiO_2 layer because there is positive field acting from the gate through SiO_2 layer, because of the applied positive potential to the gate V_{GS} . As more number of electrons are attracted towards this region, the hole density in the p - substrate (below the SiO_2 layer between n - type source and drain only) decrease. This is true only in the relatively small region of the substrate directly below the gate. An n - type region now extends continuously from source to drain. The n - channel below the gate is said to be induced because it is produced by the process of electric inductor. If the positive gate potential is removed, the induced channel disappears.

If the gate voltage is further increased, greater number of negative charge carriers are attracted towards the induced channel. So as the carriers density increases, the effective channel resistance decreases, because there are large number of free carriers (electrons). So the resistance seen by the V_{DS} depends on the voltage applied to the gate. The higher the gate potential, the lower the channel resistance, and the higher drain current I_D . This process is referred to as

enhancement because I_D increases, and the resulting MOSFET is called *enhancement type MOSFET*. The resistance looking into the gate is high since the oxide is an insulator. The resistance will be of the order of $10^{15}\Omega$ and the capacitance value will also be large.

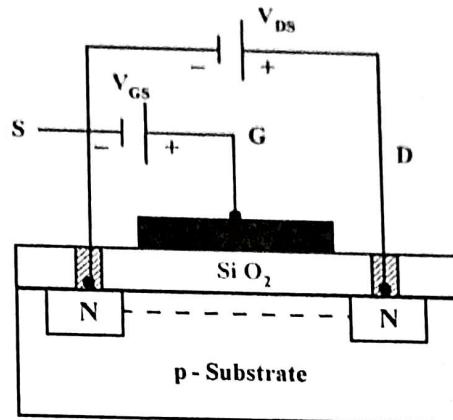


Fig 4.51 MOSFET biasing.

Depletion type MOSFET can also be constructed in the same way. These are also known as DE MOSFETs. Here as the gate voltage increases, the channel is depleted of carriers. So channel resistance increases.

Here the region below the gate is doped n - type. If negative voltage is applied to the gate, negative charge on the gate induces equal positive charge i.e., holes. These holes will recombine with the electrons of the n - channel between sources drain since channel resistivity increases. The channel is depleted of carriers. Therefore I_D decreases as V_{GS} increases. (negative voltage) If we apply positive voltage to V_{GS} , then this becomes enhancement type.

4.12.3 MOSFET CHARACTERISTICS

There are two types of MOS FETs,

1. Enhancement type
2. Depletion type.

Depletion type MOSFET can also be used as enhancement type. But enhancement type cannot be used as depletion type. So to distinguish these two, the name is given as depletion type MOSFET which can also be used in enhancement mode.

As V_{GS} is increased in positive values ($0, +1, +2$ etc) if I_D increases, then it is enhancement mode of operation because I_D is enhanced or increased.

As V_{GS} is increased in negative values ($0, -1, -2$, etc) if I_D decreases, then it is depletion mode of operation.

Consider n - channel MOSFET, depletion type. Fig. 4.52.

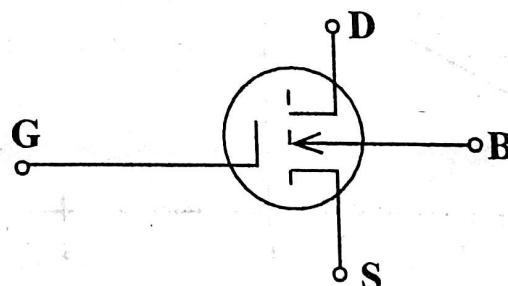


Fig 4.52 n - channel MOSFET.

DRAIN CHARACTERISTIC : I_D versus V_{DS}

When $V_{GS} = 0V$, for a given V_{DS} , significant current flows just like in a JFET. When the gate is made negative (i.e., $V_{GS} = -1V$), it is as if a negative voltage is applied for one plate of plate capacitor. So a positive charge will be induced below the gate in between the n type source and drain. Because it is semiconductor electrons and holes are induced in it below the gate. The channel between the source and drain will be depleted of majority carriers electrons, because these induced holes will recombine with the electrons. Hence, the free electron concentration in the channel between source and drain decreases or channel resistivity increases. Therefore current decreases as V_{GS} is made more negative i.e., $-1, -2, \dots$ etc. This is the depletion mode of operation because the channel will be depleted of majority carriers as V_{GS} is made negative (for n-channel MOSFET).

In a FET, there is a p - n junction between gate and source. But in MOSFET, there is no such p - n junction. Therefore, positive voltage positive V_{GS} can also be applied between gate and source. Now a negative charge is induced in the channel, thereby increase free electron

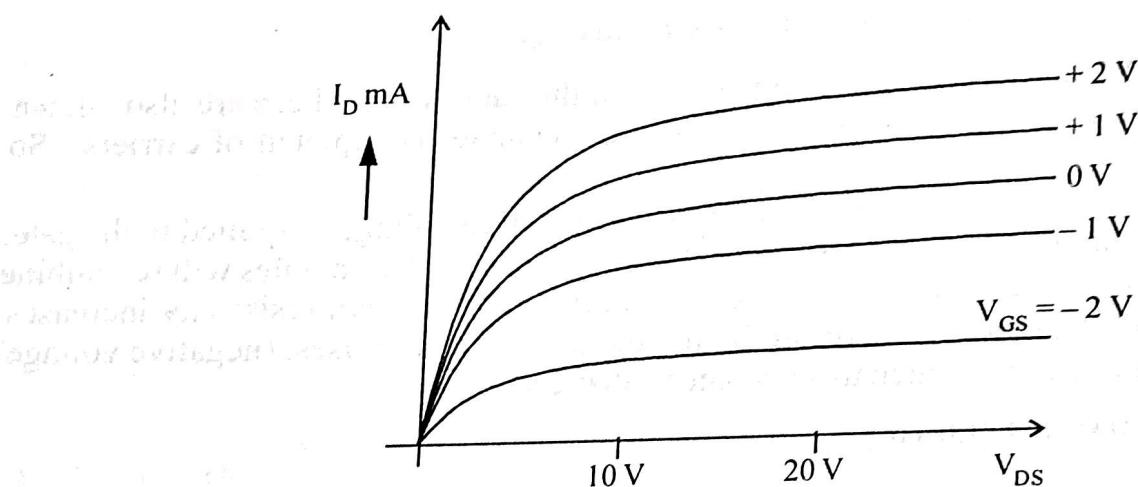


Fig 4.53 Drain characteristics (N MOS).

concentration. So channel conductivity increases and hence I_D increases. Thus, the current is enhanced. So, the device can be used both in enhancement mode and depletion mode.

In the transfer characteristic as V_{GS} increases, V_D increases. Similarly in the depletion mode as V_{GS} is increases in negative values, I_D decreases

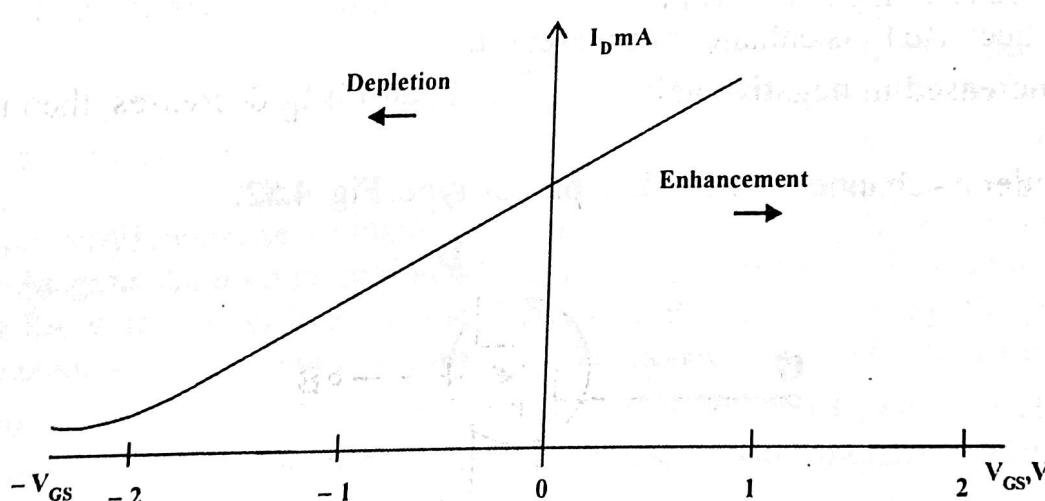


Fig 4.54 Gate characteristics

Transistor Characteristics

A JFET is a depletion type, because as V_{GS} is made positive (+1, +2 etc for n-channel FET) I_D increases. So it can be used in enhancement type. But there is no other type of JFET which is used only in enhancement mode and no depletion mode, hence no distinction is made.

4.12.4 MOSFET GATE PROTECTION

The SiO_2 layer of gate is extremely thin, it will be easily damaged by excessive voltage. If the gate is left open circuited, the electric field will be large enough (due to accumulation of charge) to cause punch through in the SiO_2 layer or the dielectric. To prevent this damage, some MOS devices are fabricated with zener diode between gate and substrate. When the potential at the gate is large, the zener will conduct and the potential at the gate will be limited to the zener breakdown voltage. When the potential at the gate is not large, the zener is open circuited and has no effect on the device.

If the body (bulk) of MOS transistor (MOSFET) is p - type Silicon, and if two 'n' regions separated by the channel length are diffused into the substrate to form source and drain n-channel enhancement device (designated as NMOS) is obtained. In NMOS, the induced mobile channel surface charges would be *electrons*.

Similarly, if we take n -type substrate and diffuse two p - regions separated by the channel length to form source and drain, PMOSFET will be formed. Here in the induced mobile channel surface charges would be *holes*.

4.12.5 COMPARISON OF p-CHANNEL AND n-CHANNEL MOSFETS

Initially there were some fabrication difficulties with n-channel MOSFETs. But in 1974, these difficulties were overcome and mass productions of n-channel MOSFETs began. Thus NMOSFETs have replaced PMOSs and PMOSFETs have almost become obsolete.

The hole mobility in Silicon at normal fields is $500 \text{ cm}^2/\text{v.sec}$. Electron mobility = $1300 \text{ cm}^2/\text{v.Sec}$. Therefore p-channel ON resistance will be twice that of n-channel MOSFET ON resistance (ON resistance means the resistance of the device when I_D is maximum for a given V_{DS}) ON resistance depends upon ' μ ' of carriers because $\sigma = \frac{1}{\rho} = ne\mu_n$ or $pe\mu_p$.

If the ON resistance of a p-channel device were to be reduced or to make equal to that of n - channel device, at the same values of I_D and V_{DS} etc, then the p-channel device must have more than twice the area of the n-channel device. Therefore n - channel devices will be smaller

or packing density of n-channel devices is more ($R = \frac{\rho l}{A}$.R is decreased by increase in A).

The second advantage of the NMOS devices is fast switching. The operating speed is limited by the internal RC time constant of the device. The capacitance is proportional to the junction cross sections.

The third advantage is NMOS devices are TTL compatible since the applied gate voltage and drain supply are positive for an n - channel enhancement MOS.

(Because in n-channel MOS, source and drain are n-type. So drain is made positive. For enhancement type the gate which is Al metal is made positive).

4.12.6 ADVANTAGES OF NMOS OVER PMOS

1. NMOS devices are fast switching devices since electron mobility is less than holes.
2. NMOS devices are TTL compatible since V_{GS} and V_D to be applied for NMOS devices are positive
3. Packing density of NMOS devices is more
4. The ON resistance is less because conductivity of NMOS devices is more since μ of electrons is greater than that of holes.

4.13 THE DEPLETION MOSFET

In enhancement type MOSFET, a channel is not diffused. It is of the same type (p-type or n-type) as the bulk or substrate. But if a channel is diffused between source and drain with the same type of impurity as used for the source and drain diffusion depletion type MOSFET will be formed.

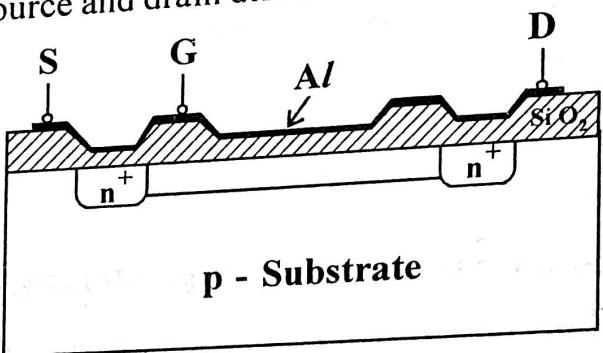


Fig 4.55 Depletion MOSFET.

The conductivity of the channel in the case of depletion type is much less compared to enhancement type. The characteristics of depletion type MOSFETs are exactly similar to that of JFET.

When V_{DS} is positive and $V_{GS} = 0$, large drain current denoted as I_{DSS} (Drain to source current saturation value) flows. If V_{GS} is made negative, positive charges are induced in the channel through SiO_2 of the gate capacitor. But the current in MOSFET is due to majority carriers. So the induced positive charges in the channel reduces the resultant current I_{DS} . As V_{GS} is made more negative, more positive charges are induced in the channel. Therefore its conductivity further decreases and hence I_D decreases as V_{GS} is made more negative (for n-channel depletion type). The current I_D decreases because, the electrons from the source recombine with the induced positive charges. So the number of electrons reaching the drain reduces and hence I_D decreases. So because of the recombination of the majority carriers, with the induced charges in the channel, the majority carriers will be depleted. Hence, this type of MOSFET is known as **depletion type MOSFET**. JFET and depletion MOSFET have identical characteristics.

A MOSFET of depletion type can also be used as enhancement type. In the case of n-channel depletion type (source and drain are n-type), if we apply positive voltage to the gate-source junction, negative charges are induced in the channel. So, the majority carriers (electrons in the source) are more and hence I_D will be very large. Thus, depletion type MOSFET can also be used as enhancement type by applying positive voltage to the gate (for n-channel type).

Transistor Characteristics

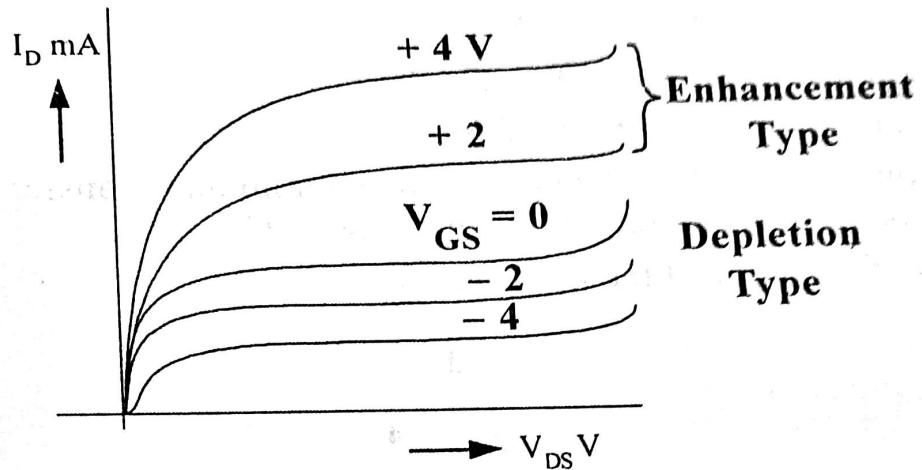


Fig 4.56 Drain characteristics of DMOSFET.

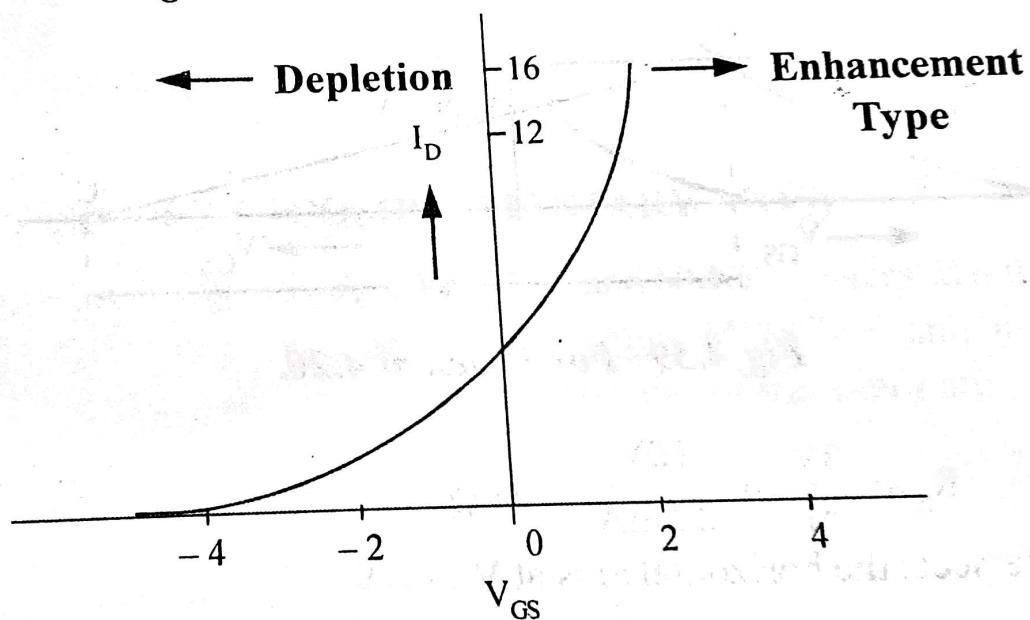


Fig 4.57 Gate characteristics of depletion type MOSFET.