				or $[1 + R_s(\mu + 1)] \parallel R_D$
A_v	$-g_m(r_d \parallel R_D)$	$-g_m R_D$	$\dfrac{-g_m R_D}{1+g_m R_s + \dfrac{R_s + R_D}{r_d}}$	$\dfrac{-g_m R_D}{1+g_m R_s}$

Table 10.3

(Dec-2000)

10.5 Common Drain Circuit (Source Follower)

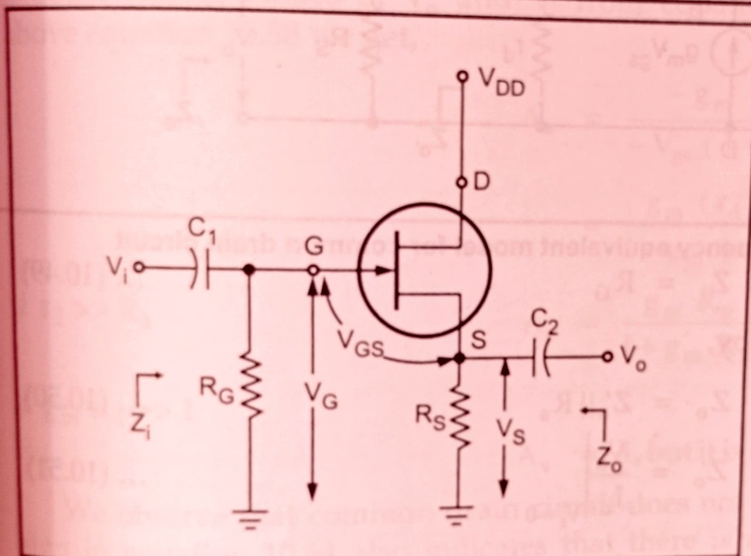

Fig. 10.21 Common drain amplifier circuit

In common drain amplifier circuit input is applied between gate and source and output taken between source and drain.

Fig. 10.21 shows common drain configuration.

It shows that the output is taken from source and when the dc supply is replaced by its short circuit equivalent the drain is grounded and thus common between input and output.

In the common drain circuit the source voltage V_s is given as,

$$V_s = V_G + V_{GS}$$

When a signal is applied to the JFET gate via C_1, V_G varies with the signal. As V_{GS} is fairly constant and $V_s = V_G + V_{GS}$, V_s varies with V_i. For example, if V_i increases by 0.25 V, V_s also approximately increases by 0.25 V. Because the output voltage at the source (V_s) follows changes in the signal voltage applied to the gate, this circuit is also called as source follower.

Fig. 10.22 shows the low frequency equivalent model for the common drain amplifier circuit shown in Fig. 10.21.

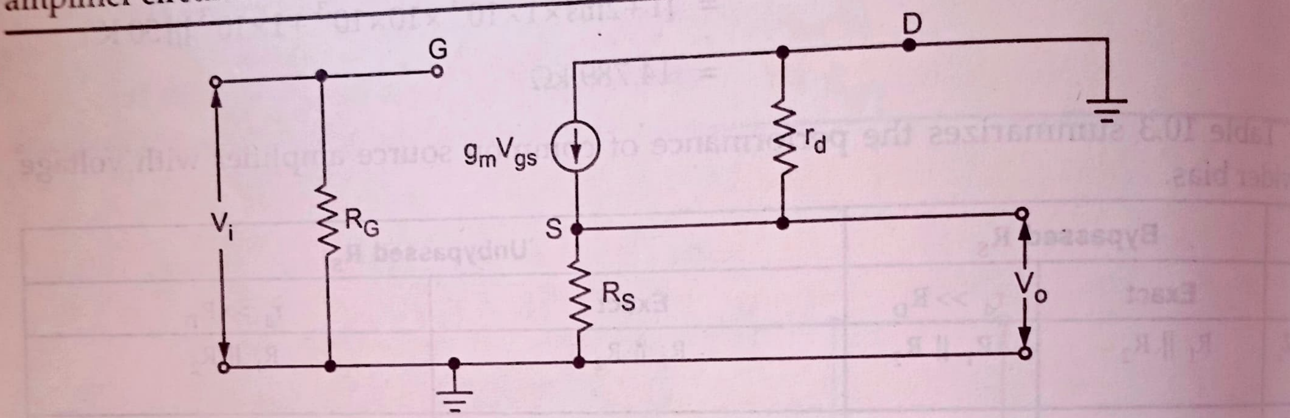

Fig. 10.22 Low frequency equivalent model for common drain circuit

This low frequency equivalent circuit can be simplified as shown in the Fig. 10.21.

Input Impedance Z_i :

Looking at Fig. 10.23 Z_i can written as,

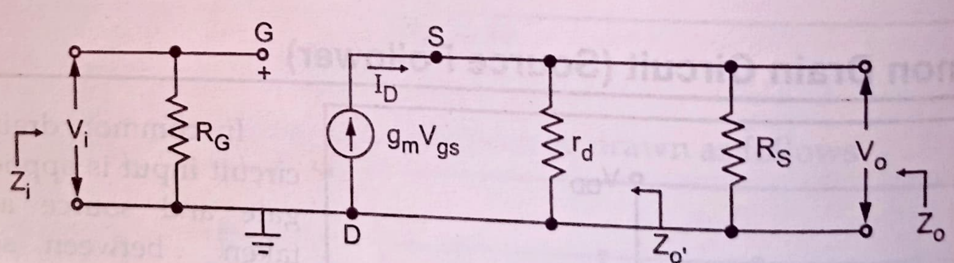

Fig. 10.23 Simplified low frequency equivalent model for common drain circuit

$$Z_i = R_G \qquad \text{... (10.49)}$$

Output Impedance Z_o : It is given by,

$$Z_o = Z'_o || R_s \qquad \text{... (10.50)}$$

where

$$Z'_o = \left.\frac{V_o}{I_d}\right|_{V_i = 0} \qquad \text{... (10.51)}$$

Applying KVL to the outer loop we can have,

$$V_i + V_{gs} - V_o = 0 \qquad \text{...(10.52)}$$