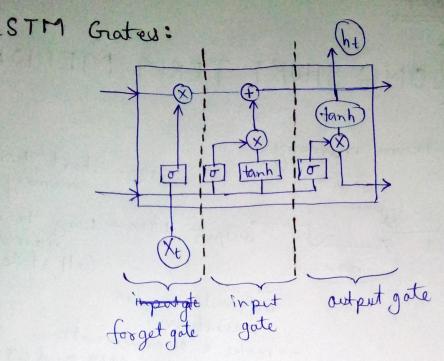
LSTM (LONG SHORT TERM MEMORY)

Long short term memory (cell state) Difficult/complex anchitecture make a communication between the STM and LTM ht-T RNIN h++1 h+1 t=1

anchitecture of LSTM

t++1



- (i) forget gate:

 Bosid on werent input decide what is

 serious from LTM.
- (ii) Input gote:
 Bosed on evenent input it decide what
 will add in LTM.
- (iii) Output Grate:

 Boundar current in put it decide what

 Boundar current in put it decide what
 is extoort from LTM and shate it as a

 result/autput.

 also at given stage create a STM