AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
International Credit Hours Engineering Programs (i.CHEP)

Project Document
Logic Design

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Program: CESS

Group : 2

Section : 3

Course Code CSE 111	*Course Name* **Logic design**	
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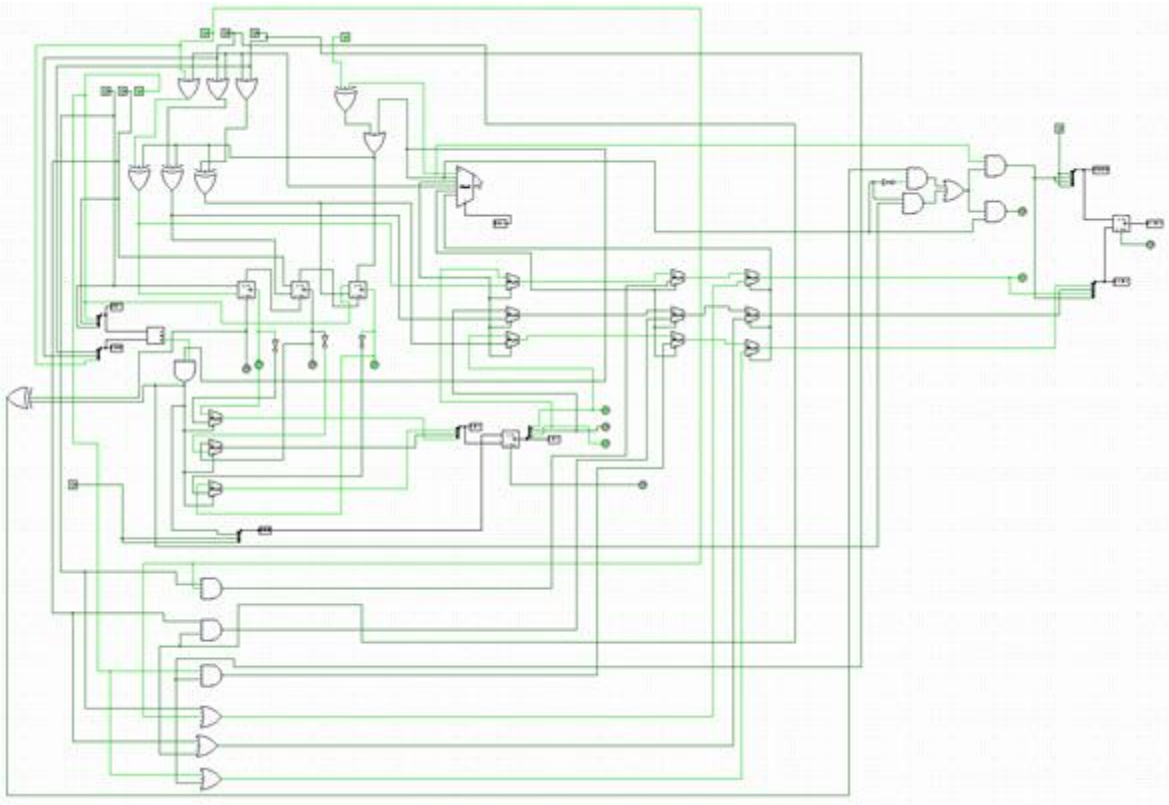
Project Document

Purpose

The purpose of writing these documents is to ensure the user is understanding how the process of each arithmetic logical operation is chosen and the number associated with it.

Also, to explain how Logic gates are used in the design to function correctly according to the given inputs, and this is done by analyzing the functionality of each part with pictures to visualize the electronic circuit.

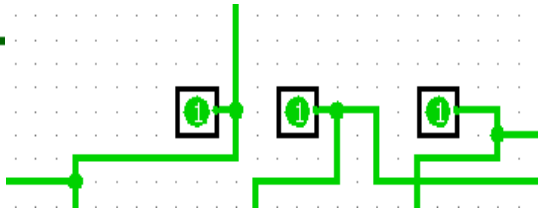
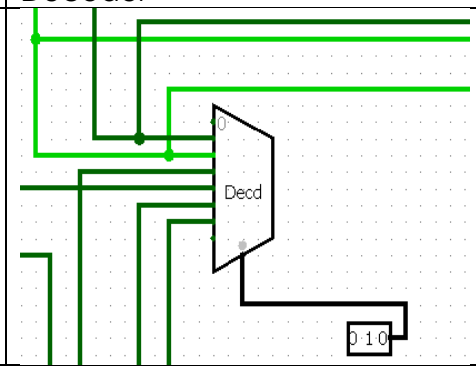
Design



Topics

Inputs/decoder:

- We have 3 bits for input A, 3 bits for input B and 3 bits as a control input.

Input A	Input B	Decoder
		

Control inputs are used as selection inputs for the 3*8 decoder to choose one of the 6 operations

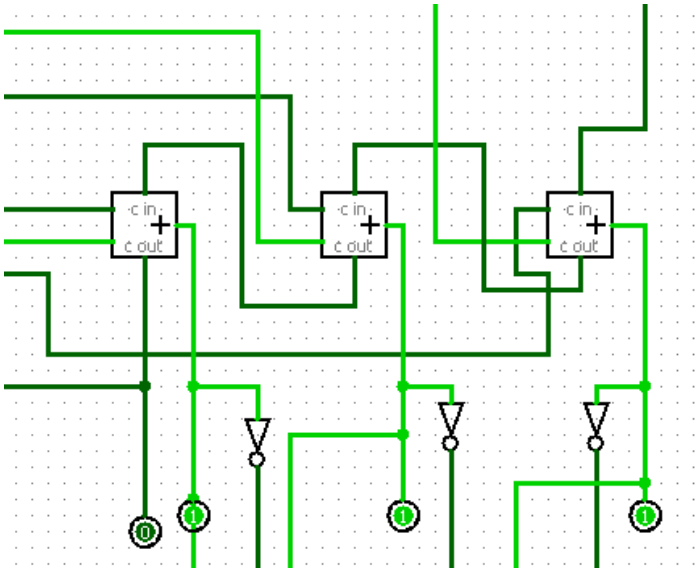
- Addition
- Subtraction
- Compliment
- Increment
- A AND B
- A OR B

The following inputs correspond to the following operations

Inputs	**Operations**
001	Addition
010	Subtraction
011	Compliment
100	Increment
101	AND
110	OR

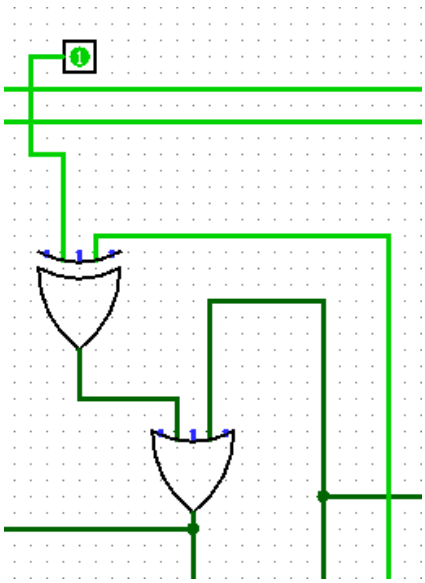
Operations:

- Addition/Subtraction
    - By using full adders to do the first 4 operations, with a carry in depending on the operation, if it's addition the carry in will be 0 and if it's subtraction the carry in will be 1.

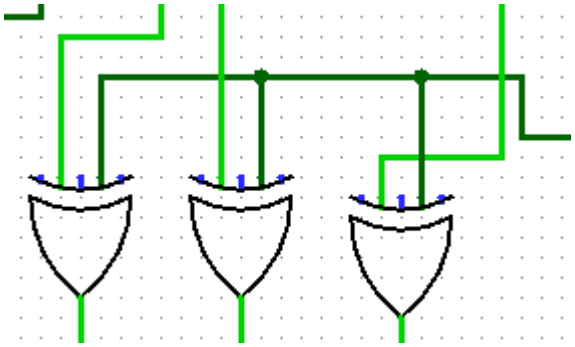


    - Then using this circuit (of XOR/OR gates) to determine the carry in to the full adder depending upon the operation.

      The inputs to the XOR are logic "1" and the "001" output of the decoder, then the output is OR with the "010" output of the decoder.



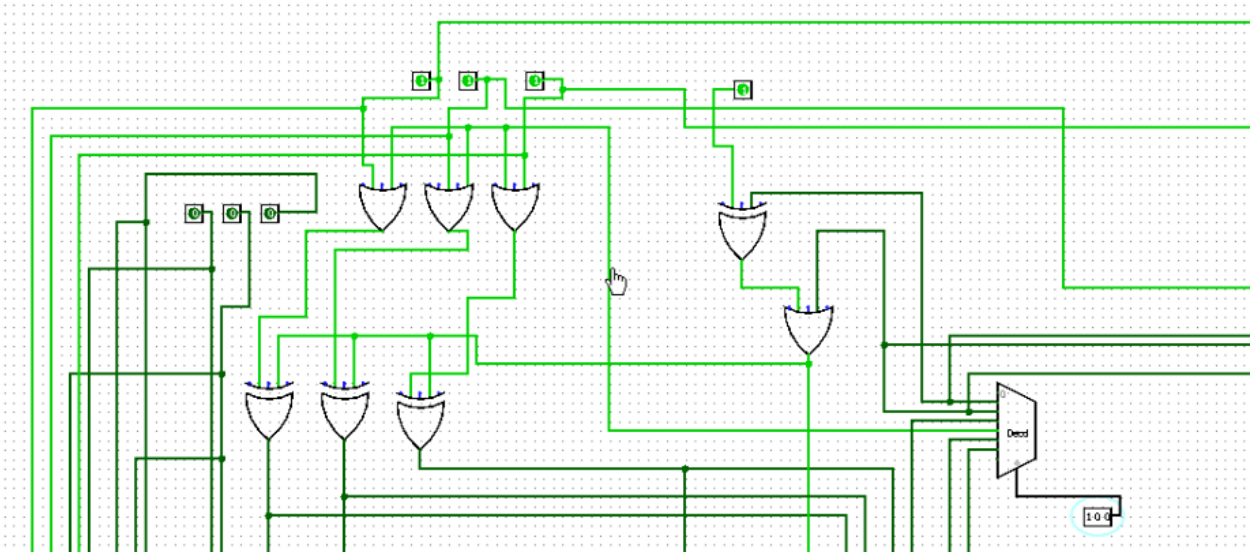
- The input B is XOR with the output of the previous circuit, to give us the compliment of B or the same input B.



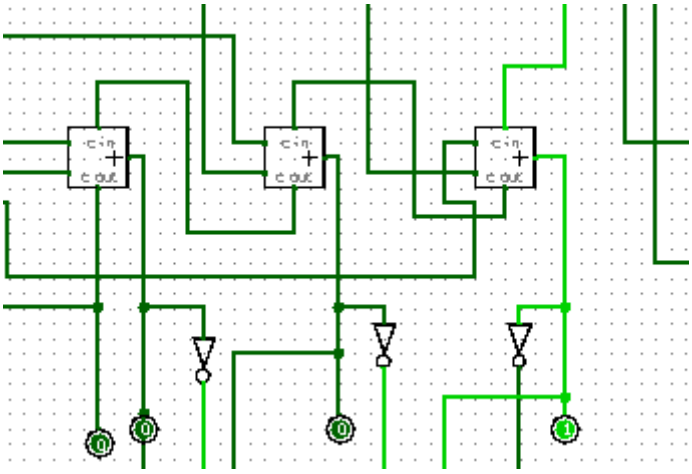
- Compliment

  The compliment is taken from the previous operation, as if the input B is XOR with 1 will give us B'

- Increment
  - The "100" output of the decoder is OR with input B to give us output 1, the output on the right side will give us logic "1", then both outputs are XOR with each other resulting in input B equal 0

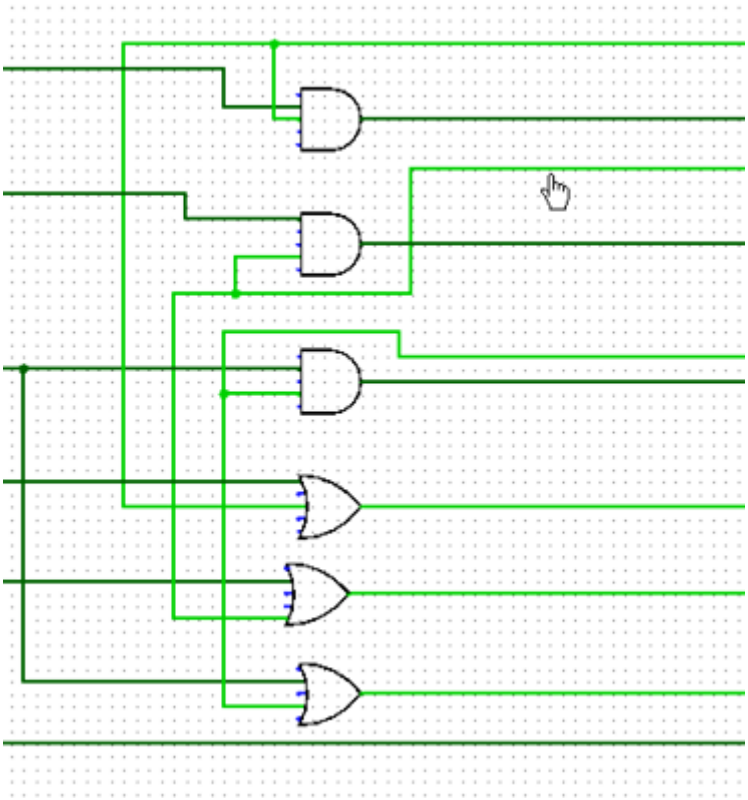


- The logic “1” on the right side will enter the full adder as a carry in with input A as the only input to the full adder, resulting in incrementing by 1.



- A AND/OR B

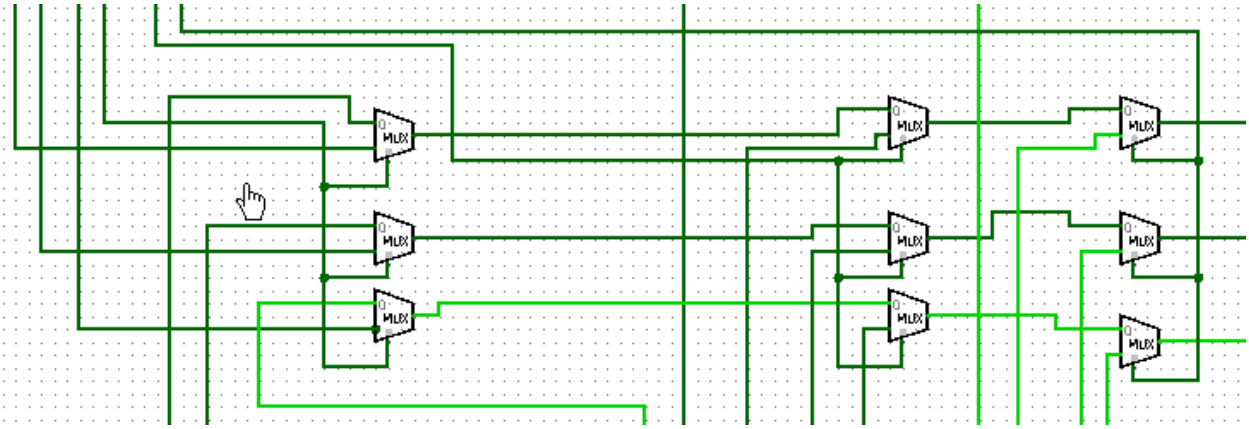
  Each bit in input A is OR/AND with the corresponding bit in input B.



Selection of output:

- Multiplexers(MUX)

  We will discuss the multiplexers on 3 stages (from left to right)



  - Stage 1

    Since, addition, subtraction and increment by one are considered the same operation in this circuit so we didn't need to include a multiplexer stage to choose between them.
    The first stage will choose between addition/subtraction and increment by 1 and the compliment of input B, by having the "011" output of the decoder
    as the selection input for the MUX.

  - Stage 2

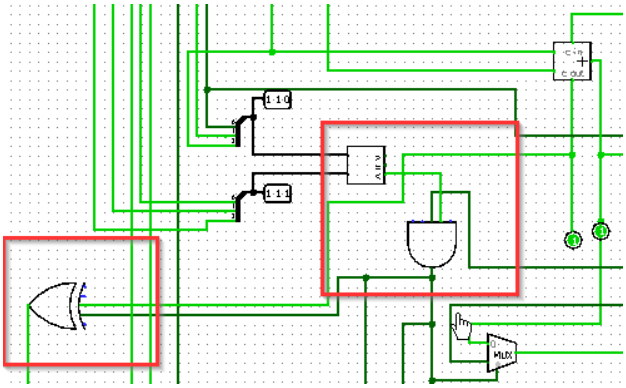
    This stage will compare between the output of stage 1 and the AND operation using the "101" output of the decoder as the selection input for the MUX.

  - Stage 3

    This stage will compare between the output of stage 2 and the OR operation using the "110" output of the decoder as the selection input for the MUX.

- Special cases
  - Bit overflow in addition/ Negative bit in subtraction

    We solved the 2 problems using this circuit by checking if input B is bigger than input A (using a magnitude comparator), then we will AND the result with "010" output of the decoder to check if we are operating on subtraction, and if not then the result of the comparator will be XOR with the M.S.B. (carry out of the full adder) because the operation will be addition.

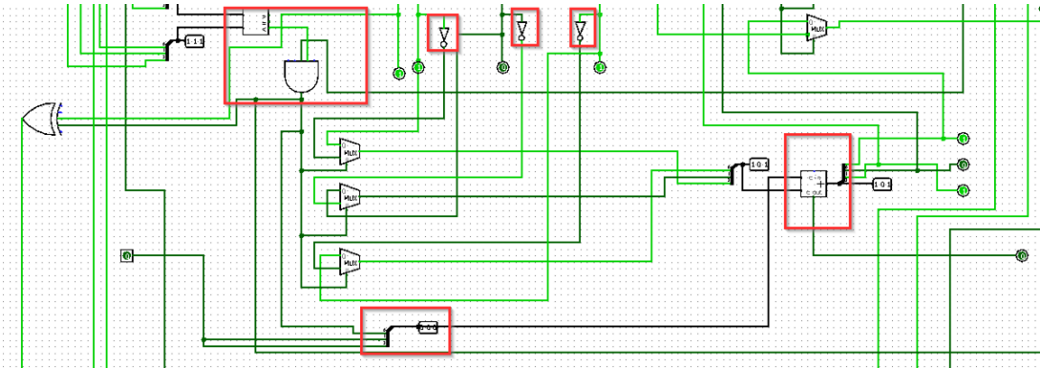


  - Changing to 2's compliment to signed magnitude (if the result is negative in subtraction)

    First we check if input B is bigger than input A (using a magnitude comparator), then we will AND the result with "010" output of the decoder to check if we are operating on subtraction.
    If the result is logic "1" the result will be the carry in of the full adder on the right.

    The result of the AND gate will be the selection bit of the MUX to choose between the result as it is and the compliment of the result,

    The MUX will choose the compliment of the full adder result if the selection bit equals to 1, otherwise the result will be displayed as it is.

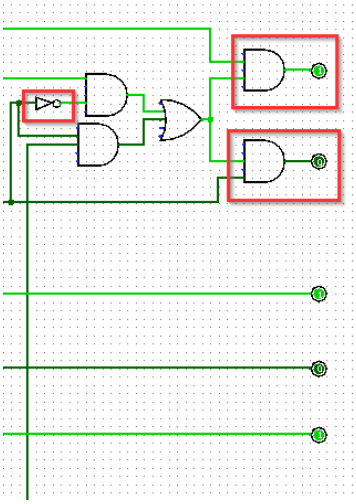


- Why the circuits generates 5 outputs

  The first 2 outputs from top are used to determine the negative sign and the overflow bit cases connected to one of the 2 seven segment displays.

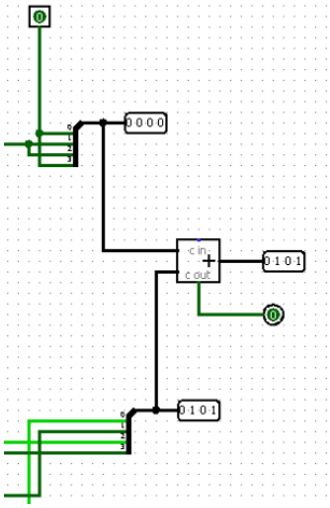
  The first red box refers to the overflow bit in addition, and the second red box refers to the second segment display.

  The last 3 bits are the magnitude displayed on the first 7 segment display



- Converting the output to BCD if the binary exceeds 9

  By checking the overflow bit we can deduce whether or not we're going to add 6 or not.



- The outputs

  They consist of 5 bits the 2 most significant bits will never be the same as one of them will responsible for displaying the negative and the other is responsible for displaying the overflow bit on the 2nd seven segment display.
  The last 3 bits are the inputs to the BCD to seven segment decoder which its outputs are going to be the inputs to the 7 segment display.