Computer Organization and Architecture assignments

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Choose the correct Answer;

١. The _____ format is usually used to store data.
a) BCD
b) Decimal
c) Hexadecimal
d) Octal
Answer :

٢. The ٨-bit encoding format used to store data in a computer is _____
a) ASCII
b) EBCDIC
c) ANCI
d) USCII
Answer :

٣. A source program is usually in _____
a) Assembly language
b) Machine level language
c) High-level language
d) Natural language
Answer:

٤. Which memory device is generally made of semiconductors?
a) RAM
b) Hard-disk
c) Floppy disk
d) Cd disk
Answer:

٥. The small extremely fast, RAM's are called as _____
a) Cache
b) Heaps
c) Accumulators
d) Stacks
Answer:

٦. The ALU makes use of _____ to store the intermediate results.
a) Accumulators
b) Registers
c) Heap
d) Stack
Answer:

٧. The control unit controls other units by generating _____
a) Control signals
b) Timing signals
c) Transfer signals
d) Command Signals
Answer:

٨. _____ are numbers and encoded characters, generally used as operands.
a) Input
b) Data

c) Information
d) Stored Values
Answer:

٩. The Input devices can send information to the processor.
a) When the SIN status flag is set
b) When the data arrives regardless of the SIN flag
c) Neither of the cases
d) Either of the cases
Answer:

١٠. _____ bus structure is usually used to connect I/O devices.
a) Single bus
b) Multiple bus
c) Star bus
d) Rambus
Answer:

١١. The I/O interface required to connect the I/O device to the bus consists of _____
a) Address decoder and registers
b) Control circuits
c) Address decoder, registers and Control circuits
d) Only Control circuits
Answer:

١٢. To reduce the memory access time we generally make use of _____
a) Heaps
b) Higher capacity RAM's
c) SDRAM's
d) Cache's
Answer:

١٣. _____ is generally used to increase the apparent size of physical memory.
a) Secondary memory
b) Virtual memory
c) Hard-disk
d) Disks
Answer:

١٤. MFC stands for _____
a) Memory Format Caches
b) Memory Function Complete
c) Memory Find Command
d) Mass Format Command
Answer:
١٥. The time delay between two successive initiations of memory operation _____
a) Memory access time
b) Memory search time
c) Memory cycle time
d) Instruction delay
Answer:

Assignment _٢: Basic Operational Concept

١. The decoded instruction is stored in _____
a) IR
b) PC
c) Registers
d) MDR
Answer:

٢. The instruction -> Add LOCA, R٠ does _____
a) Adds the value of LOCA to R٠ and stores in the temp register
b) Adds the value of R٠ to the address of LOCA
c) Adds the values of both LOCA and R٠ and stores it in R٠
d) Adds the value of LOCA with a value in accumulator and stores it in R٠
Answer:

٣. Which registers can interact with the secondary storage?
a) MAR
b) PC
c) IR
d) R٠
Answer:

٤. During the execution of a program which gets initialized first?
a) MDR
b) IR
c) PC
d) MAR
Answer:

٥. Which of the register/s of the processor is/are connected to Memory Bus?
a) PC
b) MAR
c) IR
d) Both PC and MAR
Answer:

٦. ISP stands for _____
a) Instruction Set Processor
b) Information Standard Processing
c) Interchange Standard Protocol
d) Interrupt Service Procedure
Answer:

٧. The internal components of the processor are connected by _____
a) Processor intra-connectivity circuitry
b) Processor bus
c) Memory bus
d) Rambus
Answer:

٨. _____ is used to choose between incrementing the PC or performing ALU operations.
a) Conditional codes
b) Multiplexer
c) Control unit
d) None of the mentioned
Answer:

٩. The registers, ALU and the interconnection between them are collectively called as _____
a) process route
b) information trail
c) information path
d) data path
Answer:

١٠. _____ is used to store data in registers.
a) D flip flop
b) JK flip flop
c) RS flip flop
d) None of the mentioned
Answer:.

BUS Structure

1. The main virtue for using single Bus structure is _____
a) Fast data transfers
b) Cost effective connectivity and speed
c) Cost effective connectivity and ease of attaching peripheral devices
d) None of the mentioned

Answer:
2. _____ are used to overcome the difference in data transfer speeds of various devices.
a) Speed enhancing circuitory
b) Bridge circuits
c) Multiple Buses
d) Buffer registers
Answer:
3. To extend the connectivity of the processor bus we use _____
a) PCI bus
b) SCSI bus
c) Controllers
d) Multiple bus
Answer:
4. IBM developed a bus standard for their line of computers 'PC AT' called _____
a) IB bus
b) M-bus
c) ISA
d) None of the mentioned
Answer:
5. The bus used to connect the monitor to the CPU is _____
a) PCI bus
b) SCSI bus
c) Memory bus
d) Rambus
Answer:
6. ANSI stands for _____
a) American National Standards Institute
b) American National Standard Interface
c) American Network Standard Interfacing
d) American Network Security Interrupt
Answer:
7. _____ register Connected to the Processor bus is a single-way transfer capable.
a) PC
b) IR
c) Temp
d) Z
Answer: d
8. In multiple Bus organisation, the registers are collectively placed and referred as _____
a) Set registers
b) Register file
c) Register Block

d) Map registers
Answer :

9. The main advantage of multiple bus organisation over a single bus is _____
a) Reduction in the number of cycles for execution
b) Increase in size of the registers
c) Better Connectivity
d) None of the mentioned
Answer:
10. The ISA standard Buses are used to connect _____
a) RAM and processor
b) GPU and processor
c) Harddisk and Processor
d) CD/DVD drives and Processor
Answer: c

Performance of a System

1. During the execution of the instructions, a copy of the instructions is placed in the _____
a) Register
b) RAM
c) System heap
d) Cache
Answer:
2. Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?
a) A
b) B
c) Both take the same time
d) Insufficient information
Answer:
3. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____
a) Super-scaling
b) Pipe-lining
c) Parallel Computation
d) None of the mentioned
Answer:
4. For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?
a) ISA
b) ANSA
c) Super-scalar
d) All of the mentioned
Answer:
5. The clock rate of the processor can be improved by _____
a) Improving the IC technology of the logic circuits
b) Reducing the amount of processing done in one step
c) By using the overclocking method
d) All of the mentioned
Answer:
6. An optimizing Compiler does _____
a) Better compilation of the given piece of code
b) Takes advantage of the type of processor and reduces its process time
c) Does better memory management
d) None of the mentioned
Answer:
7. The ultimate goal of a compiler is to _____
a) Reduce the clock cycles for a programming task
b) Reduce the size of the object code
c) Be versatile
d) Be able to detect even the smallest of errors
Answer:
8. SPEC stands for _____
a) Standard Performance Evaluation Code
b) System Processing Enhancing Code

c) System Performance Evaluation Corporation
d) Standard Processing Enhancement Corporation
Answer: c
9. As of 2000, the reference system to find the performance of a system is _____
a) Ultra SPARC 10
b) SUN SPARC
c) SUN II
d) None of the mentioned
Answer:
10. When Performing a looping operation, the instruction gets stored in the _____
a) Registers
b) Cache
c) System Heap
d) System stack
Answer:
11. The average number of steps taken to execute the set of instructions can be made to be less than one by following _____
a) ISA
b) Pipe-lining
c) Super-scaling
d) Sequential
Answer:
12. If a processor clock is rated as 1250 million cycles per second, then its clock period is _____
a) $1.9 * 10^{-10}$ sec
b) $1.6 * 10^{-9}$ sec
c) $1.25 * 10^{-10}$ sec
d) $8 * 10^{-10}$ sec
Answer:
13. If the instruction, Add R1, R2, R3 is executed in a system that is pipe-lined, then the value of S is (Where S is a term of the Basic performance equation)?
a) 3
b) ~2
c) ~1
d) 6
Answer:
14. CISC stands for _____
a) Complete Instruction Sequential Compilation
b) Computer Integrated Sequential Compiler
c) Complex Instruction Set Computer
d) Complex Instruction Sequential Compilation
Answer:
15. As of 2000, the reference system to find the SPEC rating are built with _____ Processor.
a) Intel Atom SParc 300Mhz
b) Ultra SPARC -IIi 300MHZ
c) Amd Neutrino series
d) ASUS A series 450 Mhz
Answer: