CMOS Processing:

Paper: “Seeing Double”

Paper:“EUV Chipmaking Inches Forward”

Q1: What defines the resolution of the photolithography process?

Proportional to the wavelengths.
Aperture of the lenses
R = k*(wavelength/AP)

Q2: What are the main blocking points of EUV lithography?

- EUV Light source not bright enough.
- Optical assemblies expensive
- Small defects on the mask are hard to detect

Q3: Describe the idea of double-patterning lithography! What is the advantage, what are the main technical problems?

Advantage: R = R/2 (better resolution)

Q4: What are the options regarding the lithography process for the next-next generation 10nm node?

- EUV
- E-beam

Q5: A new FET-transistor type got introduced with Intel 22nm CMOS technology: Fin-FET

Do internet research: What are main two advantages of using Fin-FET over standard planar MOS-FET?

Fin-FET: 2 main advantages: - Lower power consumption because of lower input (gate) capacitance
- Less chip area per transistor because of third dimension used for the gate width (FIN height).

class: Fri,Nov/10