

UVLO Protection

When VBat falls below 16 V, the OUT pin of U3 is asserted low, pulling the EN pins of the 5 V buck converter and the 12 V buck converter to GND, thereby disabling both converters.

Table 6-1. Truth Table

CONDITION	OUTPUT	STATUS
SENSE > V_{IT+}	OUT high	Output high impedance
SENSE < V_{IT-}	OUT low	Output asserted

Sheet: /
File: Power_management_V2.kicad_sch

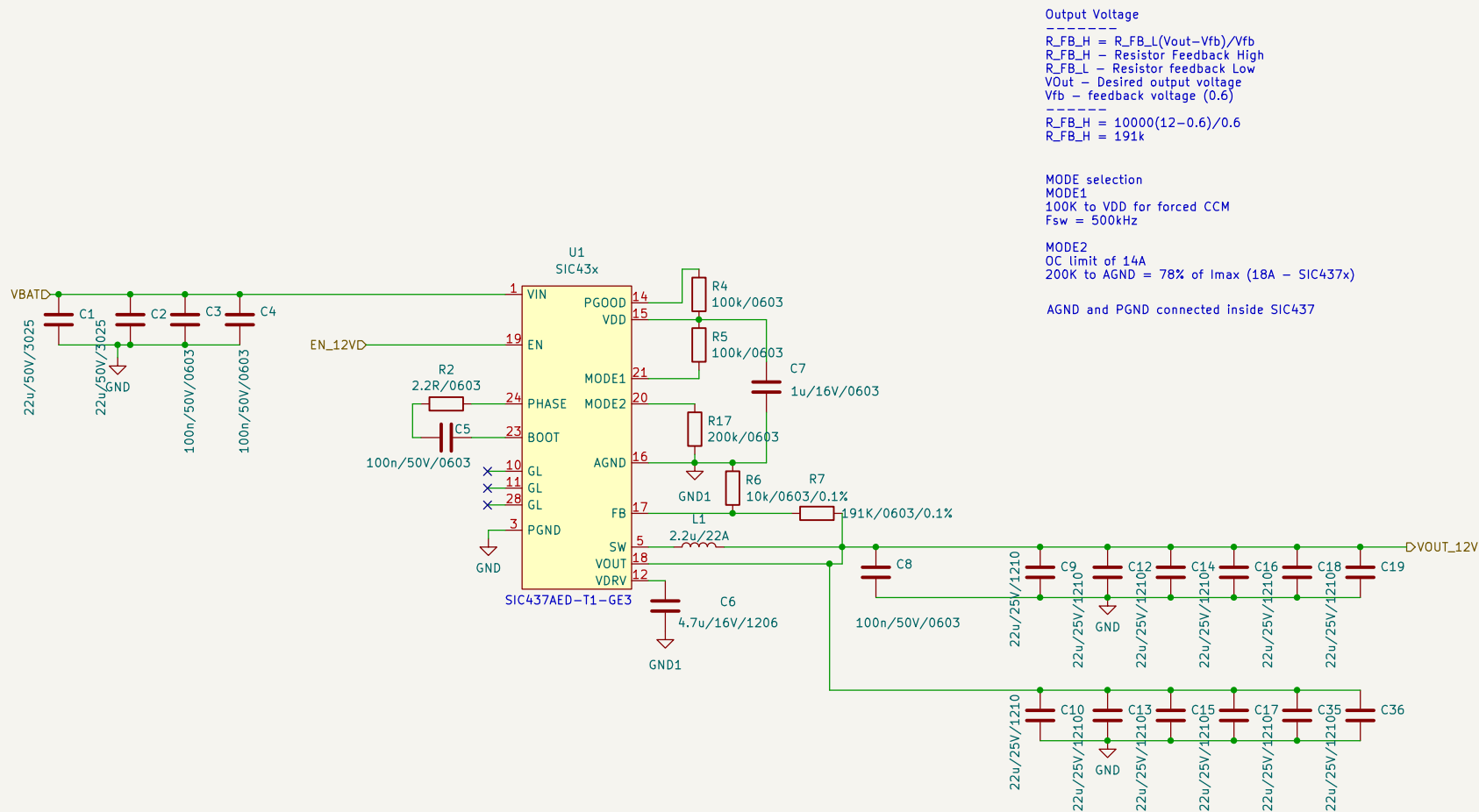
Title: Diptek Power Board V2

Size: A4 Date: 2025-08-26

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Rev: 2

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Sheet: /12V/
 File: 12V.kicad_sch

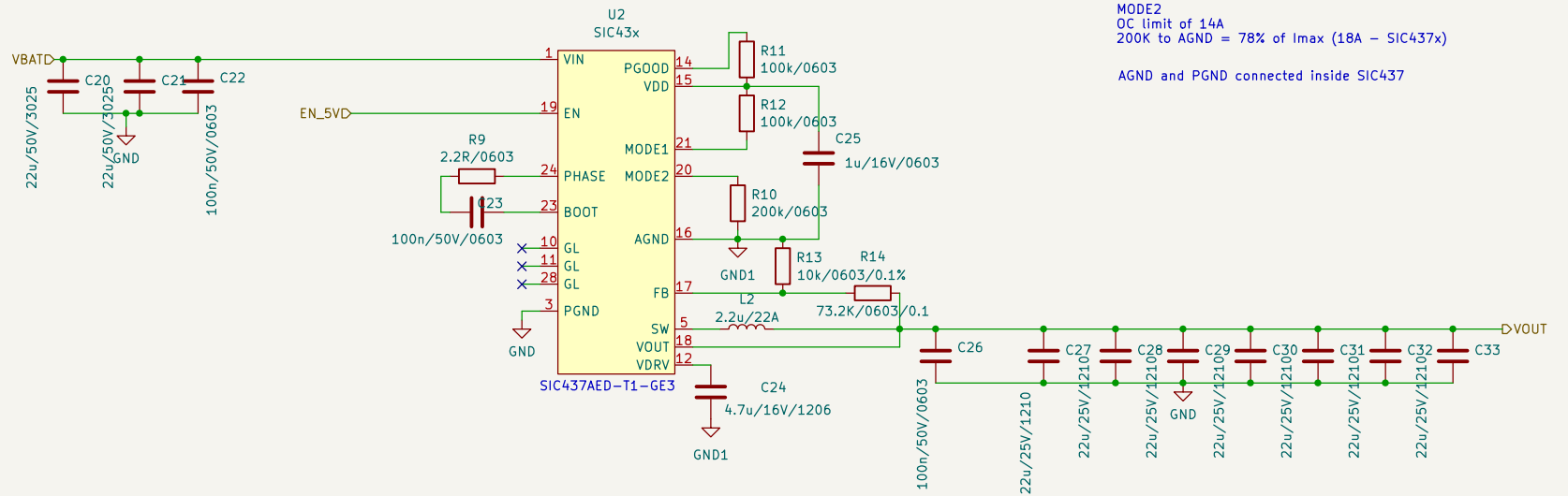
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Output Voltage

$R_{FB_H} = R_{FB_L}(V_{out} - V_{fb})/V_{fb}$
 R_{FB_H} - Resistor feedback High
 R_{FB_L} - Resistor feedback Low
 V_{out} - Desired output voltage
 V_{fb} - feedback voltage (0.6)

$R_{FB_H} = 10000(5 - 0.6)/0.6$
 $R_{FB_H} = 73.2k$

MODE selection

MODE1
 100K to VDD for forced CCM
 $f_{sw} = 500kHz$

MODE2

OC limit of 14A
 200K to AGND = 78% of I_{max} (18A - SIC437x)

AGND and PGND connected inside SIC437

Sheet: /5V/
 File: 5V.kicad_sch

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Size: A4 Date: 2025-08-26

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