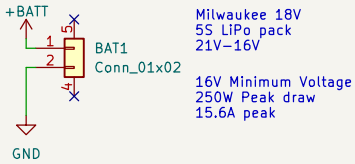

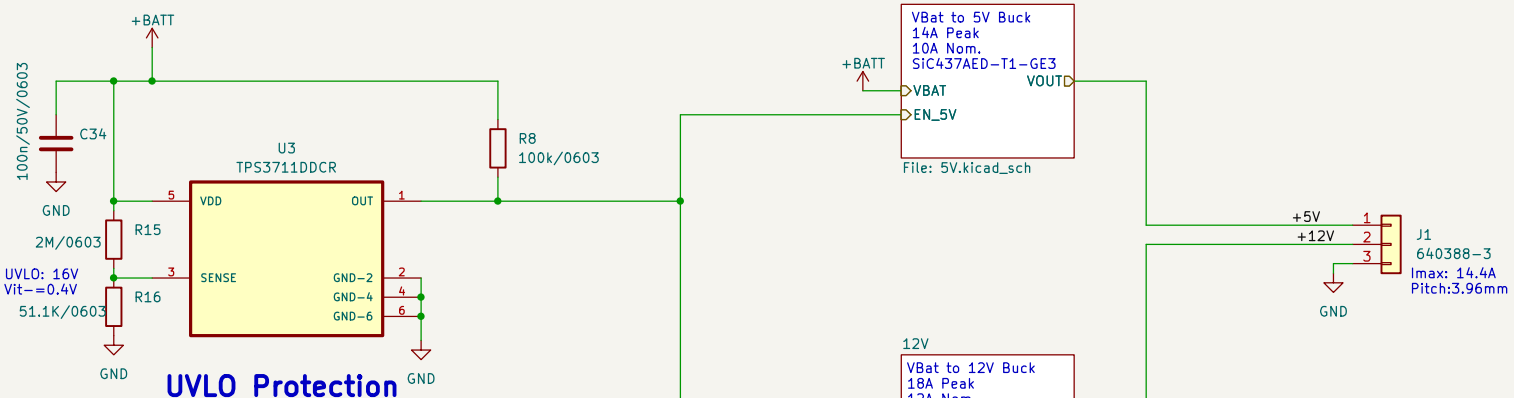

UVLO Protection

When VBat falls below 16 V, the OUT pin of U3 is asserted low, pulling the EN pins of the 5 V buck converter and the 12 V buck converter to GND, thereby disabling both converters.

Table 6-1. Truth Table

CONDITION	OUTPUT	STATUS
SENSE > V_{IT+}	OUT high	Output high impedance
SENSE < V_{IT-}	OUT low	Output asserted

Sheet: /
File: Power_management_V2.kicad_sch

Title: Diptek Power Board V2

Size: A4 | Date: 2025–08–26 | **Rev: 2**
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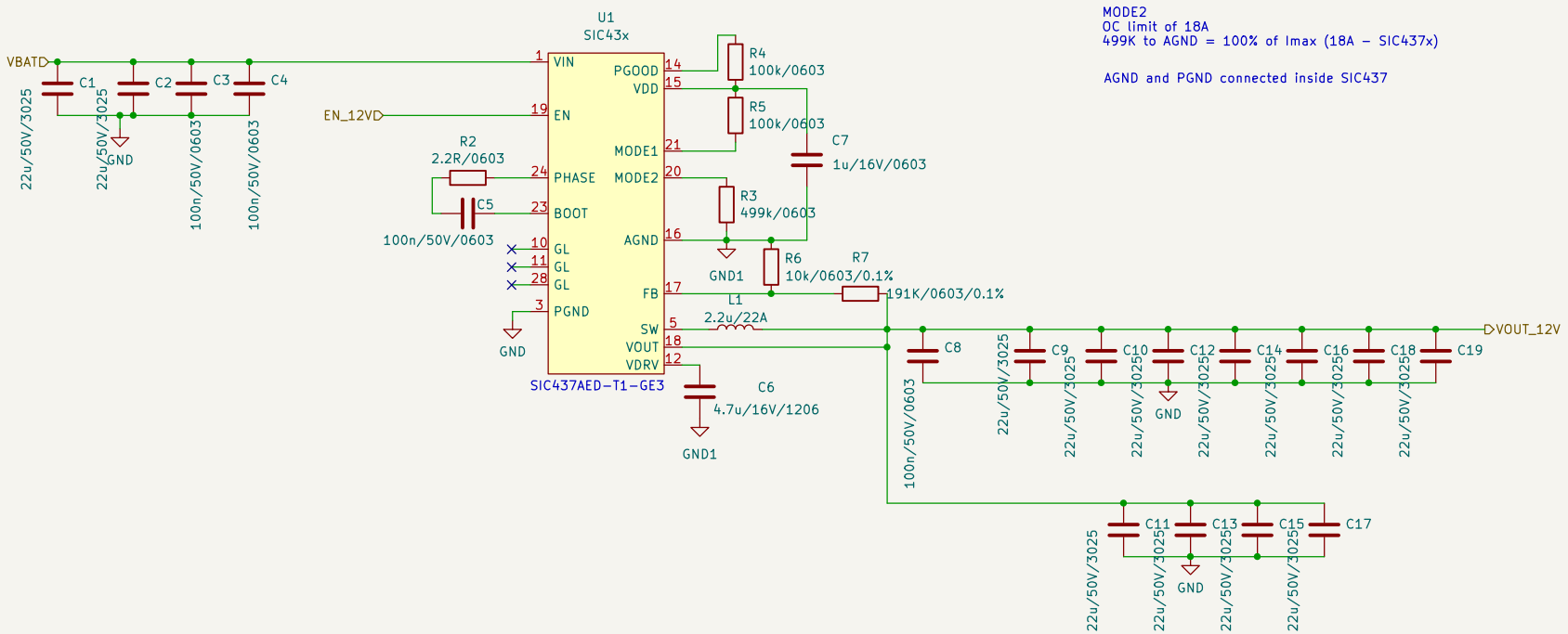

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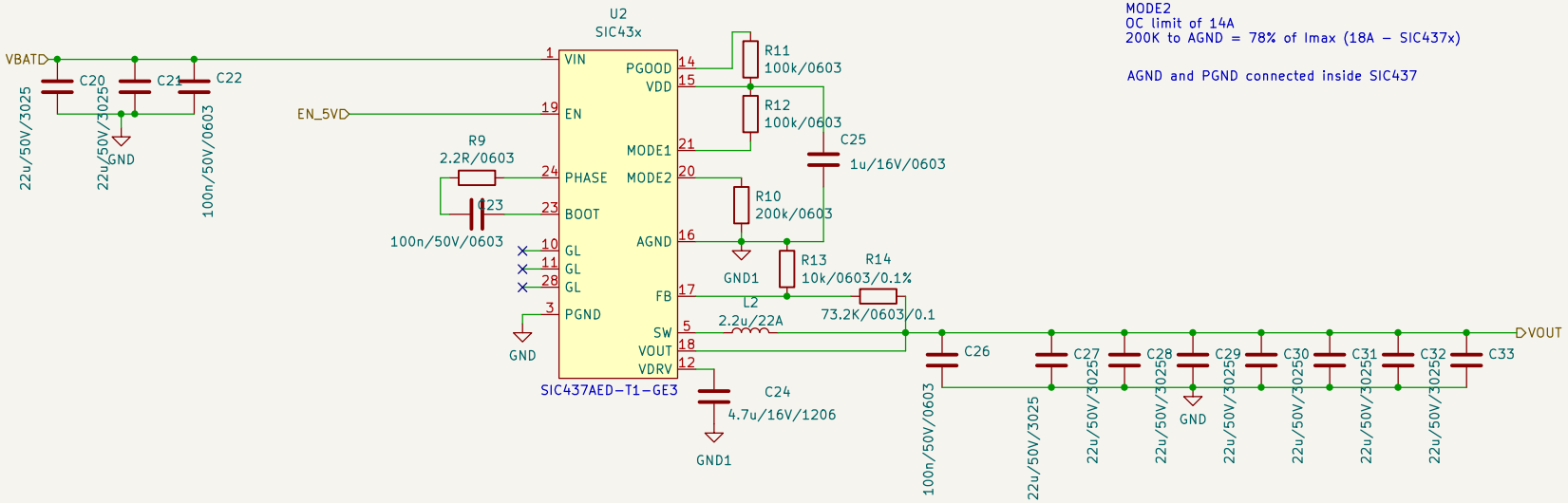

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