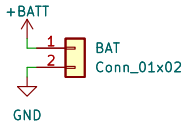
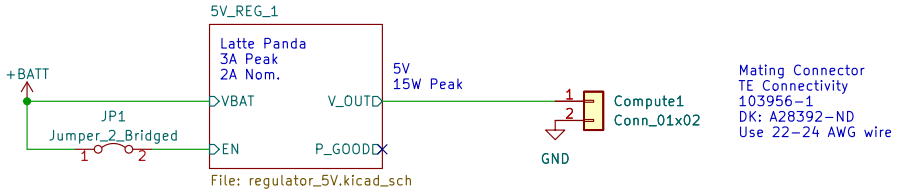
Milwaukee 18V
5S LiPo pack
21V–16V

16V Minimum Voltage
250W Peak draw
15.6A peak

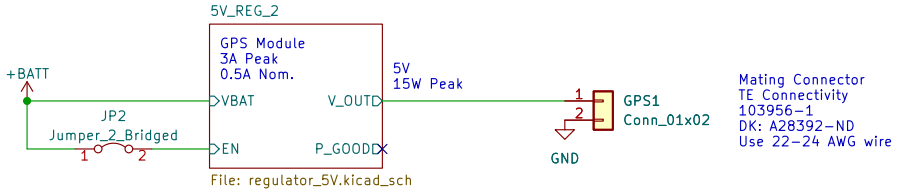


Mating Housing
Molex Ultra-Fit
1722563102
DK: WM26332-ND

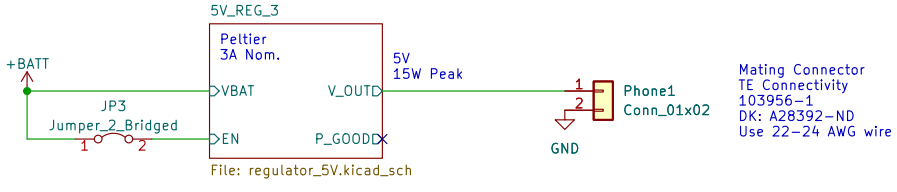
Mating Contact
Molex Ultra-Fit
1722536012
DK: 900-1722536012CT-ND



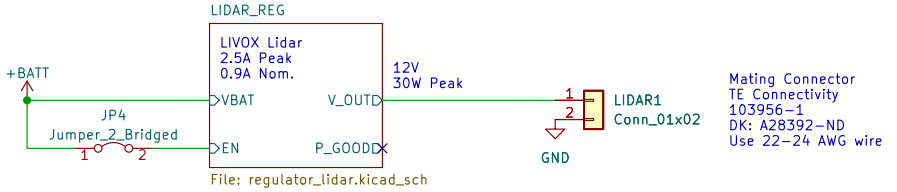
Mating Connector
TE Connectivity
103956-1
DK: A28392-ND
Use 22-24 AWG wire



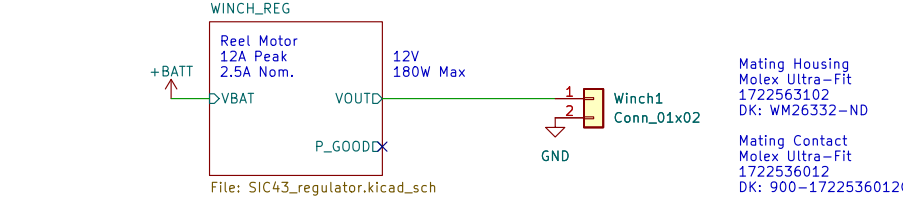
Mating Connector
TE Connectivity
103956-1
DK: A28392-ND
Use 22-24 AWG wire



Mating Connector
TE Connectivity
103956-1
DK: A28392-ND
Use 22-24 AWG wire



Mating Connector
TE Connectivity
103956-1
DK: A28392-ND
Use 22-24 AWG wire



Mating Housing
Molex Ultra-Fit
1722563102
DK: WM26332-ND

Mating Contact
Molex Ultra-Fit
1722536012
DK: 900-1722536012CT-ND

Released for discussion
Preliminary Design
Raw Matter IO Pty Ltd

Sheet: /
File: power_management.kicad_sch

Title: Diptek 5S LiPo Power distribution

Size: A4	Date: 2022-10-26	**Rev:**
KiCad E.D.A. kicad (6.0.7)		Id: 1/6

Iin = (Vout*Iout)/(Vin*Ef)
Ef is efficiency

Iin = 17.5/(15.5*0.8)
Iin = 1.411A (max)

VBAT
C1
10u 10%
X7R
GND

EN
R3
0.04W
R1
13K
R4
0.003W
R2
976
GND

ENABLE
---
has UVLO feature with hysteresis
AP633* disables once EN < 3.08V
R3 = (0.915*Von-Voff)/(4.127uA)
R4 = (1.08*R3)/(Voff-1.08+5.5uA*R3)
Von is rising edge to enable reg
Voff is falling edge to disable

Von = 3.4 * 5 = 17V
Voff = 3.1 * 5 = 15.5V
If Voff > 3.1 equations are -'ve
At 3.4V per cell, battery is below 20% capacity

R3 = 13k
R4 = 990 (976 avail.)

P_GOOD
P_GOOD is an open drain Output
5M Pullup to VIN

U1
AP63356QZV-7
1 VIN
2 EN
5 PG
8 GND
6 BST
9 SW
3 FB
4 COMP
GND
GND

C2
100n

L1
8.2u

L1 Calc
++++++
L=Vout*(Vin-Vout)/(Vin*ΔIL*Fsw)
ΔIL is the inductor current ripple
Vout= 5V
Fsw = 450kHz
ΔIL = 30%->50% * Imax = 1.051.75
---
from AP6333_inductor.py
4.4uH <= L1 <= 8.1uH
Select larger L for lower ripple factor
+++++++
From datasheet
RL <= 30mΩ
Irating >= 135% Imax = 4.72A

R3
158k
C3
47p
C4
22uF
C5
22uF
V_OUT

ESR dominates VOut ripple
Ripple = ΔIL(ESR+1/(8*Fsw*COUT)

R4
30k
GND

Compensation loop
Ground this pin for internal
loop compensation

Vout Setpoint

Vout = (1+R1/R2)*0.8

With 1% tolerance resistor

156.4k < R1 < 159.5k
29.7k < R2 < 30.3k
4.93 < Vout < 5.098
5.013 Vout nominal

If voltage drop is an issue
with R1 = 160k & R2 = 29k
5.214 Vout nominal

DFM Notes:

47pF pacakge size should be reduced
R3 & R4 package size reduced
R3 & R4 accuracy effect on UVLO calculated
L1 with custom footprint

Layout Recommendations

2Oz copper

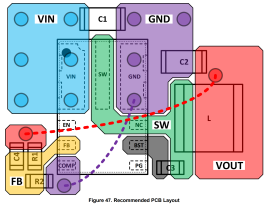


Figure 47. Recommended PCB Layout

Released for discussion
Preliminary Design
Raw Matter IO Pty Ltd
Sheet: /5V_REG_1/
File: regulator_5V.kicad_sch

Title: 5V Buck Converter

Size: A4	Date: 2022-10-26	**Rev: 1**
KiCad E.D.A. kicad (6.0.7)		Id: 2/6

Iin = (Vout*Iout)/(Vin*Ef)
Ef is efficiency

Iin = 17.5/(15.5*0.8)
Iin = 1.411A (max)

VBAT
C6
10u 10%
X7R
GND

EN
R3
0.04W
R5
13K
R4
0.003W
R6
976
GND

ENABLE
---
has UVLO feature with hysteresis
AP633* disables once EN < 3.08V
R3 = (0.915*Von-Voff)/(4.127uA)
R4 = (1.08*R3)/(Voff-1.08+5.5uA*R3)
Von is rising edge to enable reg
Voff is falling edge to disable

Von = 3.4 * 5 = 17V
Voff = 3.1 * 5 = 15.5V
If Voff > 3.1 equations are -'ve
At 3.4V per cell, battery is below 20% capacity

R3 = 13k
R4 = 990 (976 avail.)

P_GOOD
P_GOOD is an open drain Output
5M Pullup to VIN

U2
AP63356QZV-7
1 VIN
2 EN
5 PG
8 GND
6 BST
9 SW
3 FB
4 COMP
GND
GND

C7
100n
L2
8.2u
V_OUT

L1 Calc
++++++
L=Vout*(Vin-Vout)/(Vin*ΔIL*Fsw)
ΔIL is the inductor current ripple
Vout= 5V
Fsw = 450kHz
ΔIL = 30%->50% * Imax = 1.051.75
---
from AP6333_inductor.py
4.4uH <= L1 <= 8.1uH
Select larger L for lower ripple factor
+++++++
From datasheet
RL <= 30mΩ
Irating >= 135% Imax = 4.72A

R7
158k
C8
47p
C9
22uF
C10
22uF
R8
30k
GND
GND

ESR dominates VOut ripple
Ripple = ΔIL(ESR+1/(8*Fsw*COUT)

Compensation loop
Ground this pin for internal
loop compensation

Vout Setpoint

Vout = (1+R1/R2)*0.8

With 1% tolerance resistor

156.4k < R1 < 159.5k
29.7k < R2 < 30.3k
4.93 < Vout < 5.098
5.013 Vout nominal

If voltage drop is an issue
with R1 = 160k & R2 = 29k
5.214 Vout nominal

DFM Notes:

47pF pacakge size should be reduced
R3 & R4 package size reduced
R3 & R4 accuracy effect on UVLO calculated
L1 with custom footprint

Layout Recommendations

2Oz copper

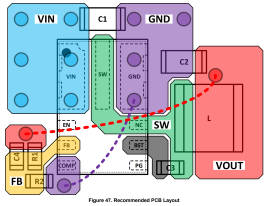


Figure 47. Recommended PCB Layout

Released for discussion
Preliminary Design
Raw Matter IO Pty Ltd
Sheet: /5V_REG_2/
File: regulator_5V.kicad_sch

Title: 5V Buck Converter

Size: A4	Date: 2022-10-26	**Rev: 1**
KiCad E.D.A. kicad (6.0.7)		Id: 3/6

Iin = (Vout*Iout)/(Vin*Ef)
Ef is efficiency

Iin = 17.5/(15.5*0.8)
Iin = 1.411A (max)

VBAT
C11
10u 10%
X7R
GND

EN
R3
0.04W
R9
13K
R4
0.003W
R10
976
GND

ENABLE
---
has UVLO feature with hysteresis
AP633* disables once EN < 3.08V
R3 = (0.915*Von-Voff)/(4.127uA)
R4 = (1.08*R3)/(Voff-1.08+5.5uA*R3)
Von is rising edge to enable reg
Voff is falling edge to disable

Von = 3.4 * 5 = 17V
Voff = 3.1 * 5 = 15.5V
If Voff > 3.1 equations are -'ve
At 3.4V per cell, battery is below 20% capacity

R3 = 13k
R4 = 990 (976 avail.)

P_GOOD
P_GOOD is an open drain Output
5M Pullup to VIN

U3
AP63356QZV-7
1 VIN
2 EN
5 PG
8 GND
6 BST
9 SW
3 FB
4 COMP
GND
GND

C12
100n

L3
8.2u

L1 Calc
++++++
L=Vout*(Vin-Vout)/(Vin*ΔIL*Fsw)
ΔIL is the inductor current ripple
Vout= 5V
Fsw = 450kHz
ΔIL = 30%->50% * Imax = 1.051.75
---
from AP6333_inductor.py
4.4uH <= L1 <= 8.1uH
Select larger L for lower ripple factor
+++++++
From datasheet
RL <= 30mΩ
Irating >= 135% Imax = 4.72A

Compensation loop
Ground this pin for internal
loop compensation

R11
158k
C13
47p
R12
30k
GND

C14
22uF
C15
22uF
GND

V_OUT

ESR dominates VOut ripple
Ripple = ΔIL(ESR+1/(8*Fsw*COUT)

Vout Setpoint

Vout = (1+R1/R2)*0.8

With 1% tolerance resistor

156.4k < R1 < 159.5k
29.7k < R2 < 30.3k
4.93 < Vout < 5.098
5.013 Vout nominal

If voltage drop is an issue
with R1 = 160k & R2 = 29k
5.214 Vout nominal

DFM Notes:

47pF pacakge size should be reduced
R3 & R4 package size reduced
R3 & R4 accuracy effect on UVLO calculated
L1 with custom footprint

Layout Recommendations

2Oz copper

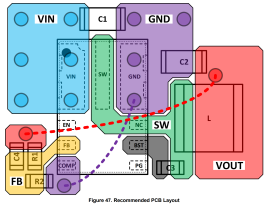


Figure 47. Recommended PCB Layout

Released for discussion
Preliminary Design
Raw Matter IO Pty Ltd
Sheet: /5V_REG_3/
File: regulator_5V.kicad_sch

Title: 5V Buck Converter

Size: A4	Date: 2022-10-26	**Rev: 1**
KiCad E.D.A. kicad (6.0.7)		Id: 4/6

Iin = (Vout*Iout)/(Vin*Ef)
Ef is efficiency

Iin = 17.5/(15.5*0.8)
Iin = 1.411A (max)

VBAT
C16
10u 10%
X7R
GND

EN
R3
0.04W
R13
13K
R4
0.003W
R14
976
GND

ENABLE
---
has UVLO feature with hysteresis
AP633* disables once EN < 3.08V
R3 = (0.915*Von-Voff)/(4.127uA)
R4 = (1.08*R3)/(Voff-1.08+5.5uA*R3)
Von is rising edge to enable reg
Voff is falling edge to disable

Von = 3.4 * 5 = 17V
Voff = 3.1 * 5 = 15.5V
If Voff > 3.1 equations are -'ve
At 3.4V per cell, battery is below 20% capacity

R3 = 13k
R4 = 990 (976 avail.)

P_GOOD
P_GOOD is an open drain Output
5M Pullup to VIN

U4
AP63356QZV-7
1 VIN
2 EN
5 PG
8 GND
6 BST
9 SW
3 FB
4 COMP
GND
GND

C17
100n
L4
8.2u
V_OUT

L1 Calc
++++++
L=Vout*(Vin-Vout)/(Vin*ΔIL*Fsw)
ΔIL is the inductor current ripple
Vout= 5V
Fsw = 450kHz
ΔIL = 30%->50% * Imax = 1.051.75
----
from AP6333_inductor.py
4.4uH <= L1 <= 8.1uH
Select larger L for lower ripple factor
+++++++
From datasheet
RL <= 30mΩ
Irating >= 135% Imax = 4.72A

Compensation loop
Ground this pin for internal
loop compensation

R15
422k
C18
47p
R16
30k
GND
C19
22uF
C20
22uF
GND

ESR dominates VOut ripple
Ripple = ΔIL(ESR+1/(8*Fsw*COUT)

Vout Setpoint

Vout = (1+R1/R2)*0.8

With 1% tolerance resistor

417.8k < R1 < 426.2k
29.7k < R2 < 30.3k
11.83 < Vout < 12.28
12.05 Vout nominal

DFM Notes:

47pF pacakge size should be reduced
R3 & R4 package size reduced
R3 & R4 accuracy effect on UVLO calculated
L1 with custom footprint

Layout Recommendations

2Oz copper

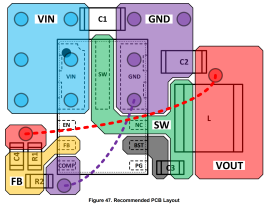
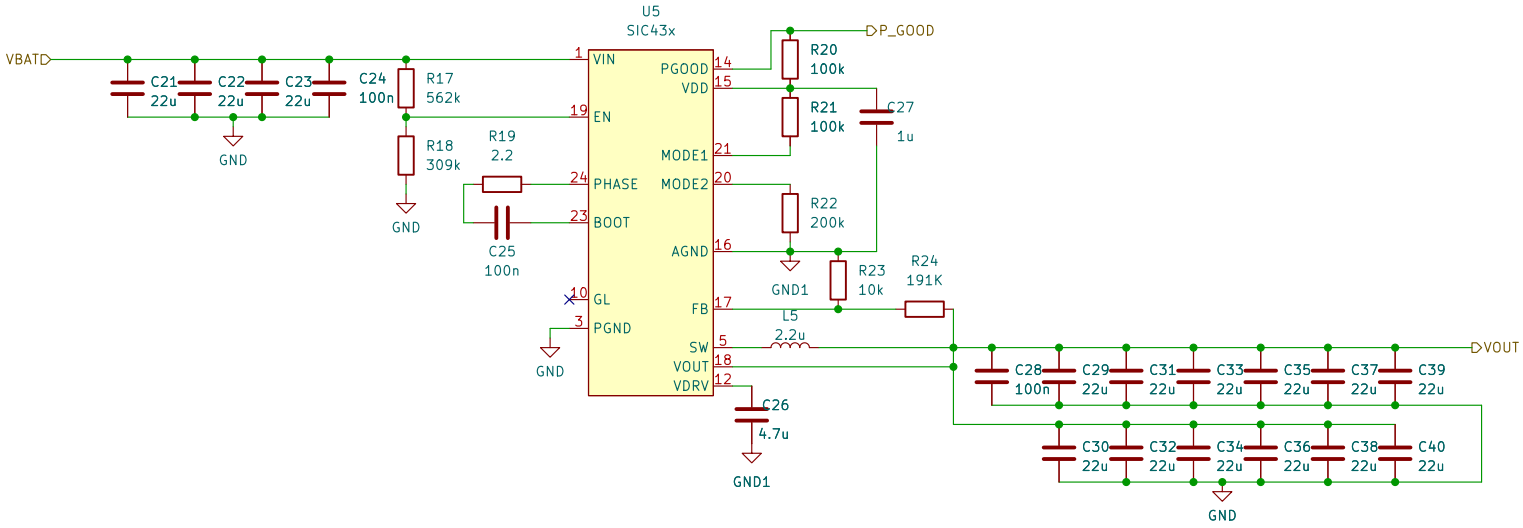


Figure 47. Recommended PCB Layout

Released for discussion
Preliminary Design
Raw Matter IO Pty Ltd
Sheet: /LIDAR_REG/
File: regulator_lidar.kicad_sch

Title: 12V Buck Converter

Size: A4	Date: 2022-10-26	**Rev: 1**
KiCad E.D.A. kicad (6.0.7)		Id: 5/6



Released for discussion
Preliminary Design
Raw Matter IO Pty Ltd

Sheet: /WINCH_REG/
File: SIC43_regulator.kicad_sch

Title:

Size: A4	Date: 2022-10-26	**Rev:**
KiCad E.D.A. kicad (6.0.7)		Id: 6/6