DESIGN AND ANALYSIS OF PHASE LOCKED LOOP IN 90nm CMOS

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***Abstract*- Power has become one of the most important concerns in design convergence for multi gigahertz communication systems such as optical data links, wireless products, microprocessor & ASIC/SOC designs. Power consumption has become a bottleneck in microprocessor design. In an effort to reduce the power consumption of the circuit, the supply voltage can be reduced leading to reduction of dynamic and static power consumption. Lowering the supply voltage, however, also reduces the performance of the circuit, which is usually unacceptable. Phase Lock Loop (PLL) is an important analog circuit used in various communication applications such as frequency synthesizer, radio, computer, clock generation, clock recovery, etc. Since all these applications are operating at different frequency, satisfying design constraints for PLL with respect to type of PLL operating frequency, Bandwidth, Settling time and other parameters is an critical and time consuming issue. Phase locked-loops (PLLs) are commonly used to generate well-timed on-chip clocks in high performance digital systems. Modern wireless communication systems employ Phase Locked Loop (PLL) mainly for synchronization, clock synthesis, skew and jitter reduction. Because of the increase in the speed of the circuit operation, there is a need of a PLL circuit with faster locking ability. Many present communication systems operate in the GHz frequency range. Hence there is a necessity of a PLL which must operate in the GHz range with less lock time. PLL is a mixed signal circuit as its architecture involves both digital and analog signal processing units. The present work is implemented in Cadence 90nm CMOS technology.**

I. INTRODUCTION

Phase-locked loops (PLLs) are widely used in radio frequency synthesis. The PLL based frequency synthesizer is one of the key building blocks of an RF front-end transceiver. The PLL frequency synthesizer system is mainly designed to ensure the accuracy of its output frequency under operating conditions. Phase noise is one of the most critical performance parameters of the frequency synthesizer. The goal to meet strict phase noise, Spurious-level performance and fine frequency resolution with reasonable levels of power consumption remains a challenging task for the circuit designer.

Phase locked loop is the heart of the many modern electronics as well as communication system. Recently plenty of the researches have conducted on the design of phase locked loop (PLL) circuit and still research is going on this topic. Most of the researches have conducted to realize a higher lock range PLL with lesser lock time and have tolerable phase noise. PLL being a mixed signal circuit involves design challenge at high frequency. Since its inspection in early 1930s, where it was used in the synchronization of the horizontal and vertical scans of television, it has come to an advanced form of integrated circuit (IC). Today found uses in many other applications. The first PLL ICs were available around 1965; it was built using purely analog component. Recent advances in integrated circuit design techniques have led to the development of high performance PLL which has become more economical and reliable. Now a whole PLL circuit can be integrated as a part of a larger circuit on a single chip.

A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL is capable of tracking the phase changes that falls in this bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock C_{Kref} to produce a high- frequency clock C_{Kout} this is known as clock synthesis.

A PLL has a negative feedback control system circuit. The main objective of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is achieved after many iterations of comparison of the reference and feedback signals. In this lock mode the phase of the reference and feedback signal is zero.

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After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant.

In general a PLL consists of five main blocks:

1. Phase Detector or Phase Frequency Detector (PD or PFD)
2. Charge Pump (CP).
3. Low Pass Filter (LPF).
4. Voltage Controlled Oscillator (VCO).
5. Divide by N Counter.

II. PLL ARCHITECTURE

The architecture of a charge-pump PLL is shown below:

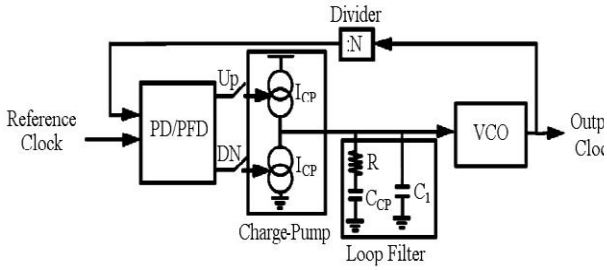

Fig 1. Architecture of PLL

A) PHASE FREQUENCY DETECTOR

The "Phase frequency Detector" (PFD) is one of the main part in PLL circuits. It compares the phase and frequency difference between the reference clock and the feedback clock. Depending upon the phase and frequency deviation, it generates two output signals "UP" and "DOWN". There are different types to implement this. Some of them are XOR based, D-flip flop based and by using tri state PFD etc.

B) CHARGE PUMP AND LOOP FILTER.

Charge pump circuit is an important block of the whole PLL system. It converts the phase or frequency difference information into a voltage, used to tune the VCO. Charge pump circuit is used to combine both the outputs of the PFD and give a single output which is fed to the input of the filter. Charge pump circuit gives a constant current of value I_{PDI} which should be insensitive to the supply voltage variation. The amplitude of the current always remains same but the polarity changes which depend on the value of the "UP" and "DOWN" signal. The passive low pass loop filter is used to convert back the charge pump current into the voltage. The output voltage of the loop filter controls the oscillation frequency of the VCO. There are certain non-idealities in charge pump, certain critical parameters involved in the design of charge pump are dynamic range, charge pump current, spurs.

C) VOLTAGE CONTROLLED OSCILLATOR

An oscillator is an autonomous system which generates a periodic output without any input. The most popular type of the VCO circuit is the current starved voltage controlled oscillator (CSVCO).

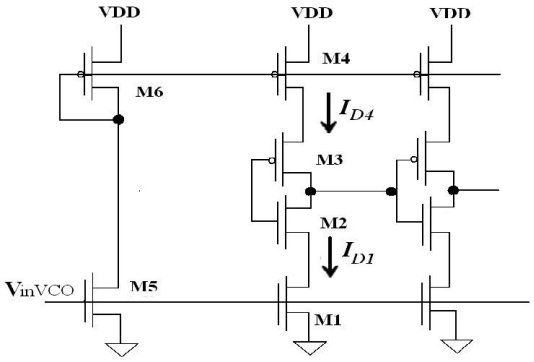

Fig 2. Simplified view of a current starved VCO

D) FREQUENCY DIVIDER

The output of the VCO is fed back to the input of PFD through the frequency divider circuit. The frequency divider in the PLL circuit forms a closed loop. It is the one which converts the oscillator high output frequency to a lower frequency which can be compared to a reference source. As the VCO is operated in the multi-GHz range, the PLL requires high frequency dividers. However, the requirement of the channel selection in the frequency synthesizer demands a programmable frequency divider. The four key design issues related to the design of the programmable dividers are the high input frequency, programmability of the division ratio, power consumption and input sensitivity (minimum amplitude of the input signal). In general, the power consumption of the divider is linearly proportional to the operating frequency. Its maximum operating frequency depends on the architecture style, supply voltage and output load. Dividers are classified in to two types mainly, analog and digital dividers. The design of analogue dividers are based on the

injection locking technique where as digital dividers are implemented using dynamic or static latches and flip-flops.

III. DESIGN AND SYNTHESIS OF PLL

The schematic level design entry of the circuits is carried out in the CADENCE Virtuoso Analog Design Environment. In order to analyze the performances, these circuits are simulated in the Spectre simulator of CADENCE tool.

A) VCO DESIGN

Since VCO is the heart of the whole PLL system, it should be designed in a proper manner. The design steps for the current starved VCO are as follows.

Step 1: Find the value of the propagation delay for each stage of the inverter in the VCO circuit using the following equation.

$$\tau_P = \frac{1}{N_f}$$

Where $\tau_P = \tau_{phl} = \tau_{plh} =$ half of the propagation delay time of the inverter.

N = number of inverter stages.

f = Required center frequency of oscillation.

Step 2: Find the (W/L) ratio for transistors in the different inverter stages using the equation in below.

$$\left(\frac{W}{L}\right)_n = \frac{C_{load}}{\tau_{phl}\mu_n\left(V_{dd} - V_{T,n}\right)}\left(\frac{2V_{T,n}}{V_{dd} - V_{T,n}} + \ln\left(\frac{4\left(V_{dd} - V_{T,n}\right)}{V_{dd}} - 1\right)\right)$$

$$\left(\frac{W}{L}\right)_p = \frac{C_{load}}{\tau_{phl}\mu_n\left(V_{dd} - V_{T,n}\right)}\left(\frac{2V_{T,p}}{V_{dd} - V_{T,p}} + \ln\left(\frac{4\left(V_{dd} - V_{T,p}\right)}{V_{dd}} - 1\right)\right)$$

Step 3: After finding (W/L) ratios, find the values for W and L.

Step 4: Find the value of the total capacitance from the expression

$$C_{tot} = \frac{5}{2}C_{ox}(L_pW_p + L_nW_n)$$

Where C_{ox} is the oxide capacitance.

L_p, W_p, L_n, W_n is the width and length of the PMOS and NMOS transistors in the inverter stages.

Step 5: Calculate the value of drain current for certain frequency which is given by

$$I_{Dcenter} = NC_{tot}V_{dd}f$$

Step 6: Find the (W/L) ratio for the current starved transistors in the circuit from the drain current expression which is represented as

$$\left(\frac{W}{L}\right)_n = \frac{2I_{Dcenter}}{\mu_nC_{ox}\left(V_{gs} - V_{T,n}\right)^2}$$

$$\left(\frac{W}{L}\right)_p = 2.5 \times \left(\frac{W}{L}\right)_n$$

B) DESIGN OF PHASE LOCKED LOOP

The value of the charge pump current and the component parameters of the loop filter play a major role in the design of the phase locked loop circuit. The value of the lock time mainly depends upon these parameters. So while designing the circuit proper care should be taken in calculating these parameters. For the given values of reference(Fref) and output frequency(Fout) as well as the lock in range, the following steps to be carried out in designing the filter circuit.

Step 1: Find the value of the divider circuit to be used which is given by

$$n = \frac{F_{out}}{F_{ref}}$$

Step 2: Find the value of the natural frequency (ω_n) from the lock in range as given below

$$\text{Lock in range} = 2 \times \zeta \times \omega_n$$

Step 3: Find the value of the charge pump gain (K_{PDI}) from the charge pump current used in the circuit which is given by

$$K_{PDI} = \frac{I_{PUMP}}{2\pi} \text{ (Amps/radian)}$$

Step 4: Find the value of the gain of the VCO circuit from the characteristics curve using the following expression.

$$K_{PDI} = \frac{f_{max} - f_{min}}{V_{max} - V_{min}} \text{ (Hz/V)}$$

Step 5: Find the values of the loop filter component parameters using the following expressions.

$$C_1 = \frac{K_{PDI} \times K_{VCO}}{N{\omega_n}^2}$$

$$C_2 = \frac{C_1}{10}$$

$$R = \frac{2\zeta}{\omega_n C1}$$

IV. SIMULATION RESULTS

A) PHASE FREQUENCY DETECTOR

The two D flip flops configuration used are identical to each other. Here an inverter is used to invert the output of a nand gate to form it as and.

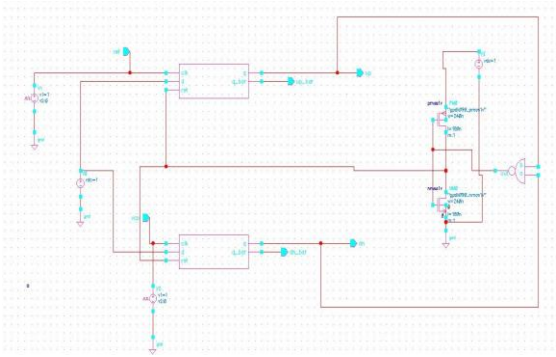

Fig 3. Phase Frequency Detector circuit

Simulation results of this Phase frequency detector are:

Fig 4. Simulation results of a PFD

B) CHARGE PUMP AND LOW PASS FILTER

The circuit of the charge pump along with the PFD is shown below.

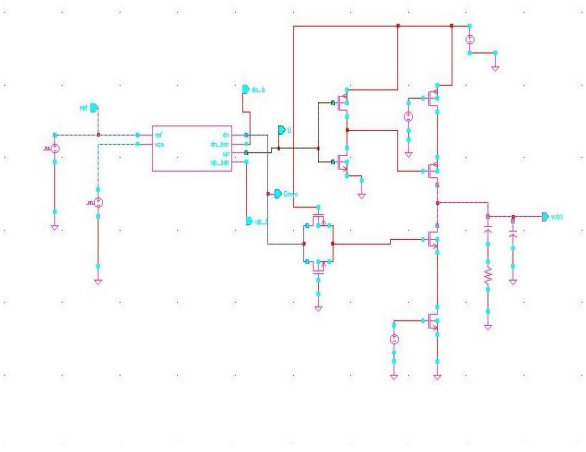

Fig 5. Charge Pump and loop filter circuit along with PFD.

The simulation result which is shown in the figure below gives an increase in the control voltage at the output of the loop filter circuit. From the figure it's clear that the control voltage increases for a period during which the UP signal of the PFD remains high. In the other case a decrease in the control voltage is produced at the output of the filter circuit which is shown in the figure. When the rising of feedback signal leads the reference signal rising edge the control voltage decreases for the period during which the DOWN signal of the PFD remains high.

Fig 6. Simulated output of Charge Pump and loop filter circuit along with PFD.

C) VOLTAGE CONTROLLED OSCILLATOR

The schematic of the current-starved VCO is shown in figure. Voltage Controlled Oscillators are widely used in communication systems. For cost reasons, it is always desirable to minimize transistor count and the number of external parts needed to build a given system.

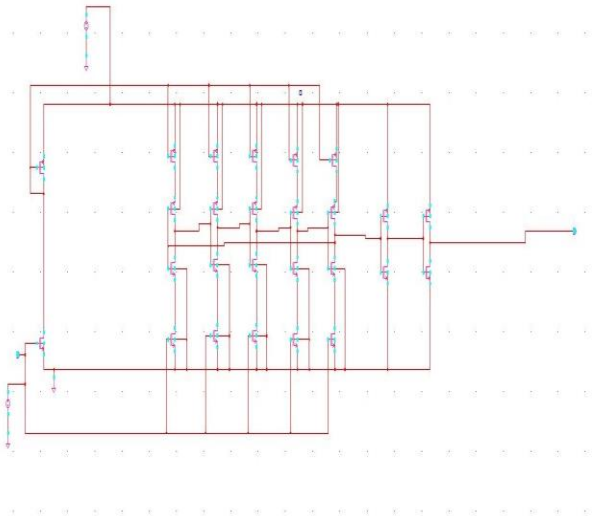

Fig 7. Schematic of Current starved VCO

Here we use two inverters at the end because to get the correct wave shapes. Without the inverters the output swing will be not a perfect square wave.

Fig 8. Output of VCO with inverters.

The average power of the VCO is calculated and is obtained as 0.5mW

Fig 9. Power of the VCO

D) PHASE LOCKED LOOP

A complete Phase Locked Loop is formed by the interconnection of all the blocks. The schematic of the PLL is seen as.

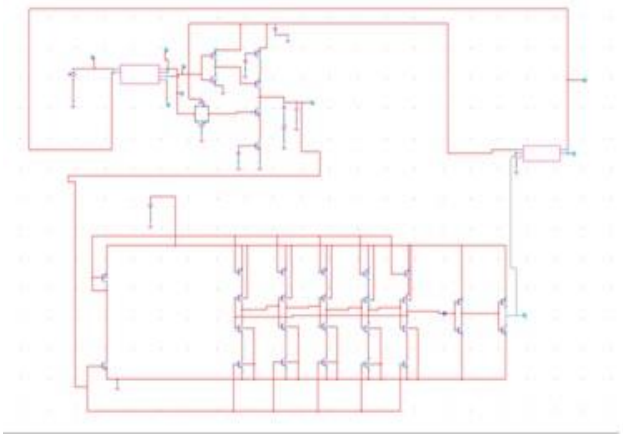

Fig 10. Phase Locked Loop

The output of the charge pump and loop filter circuit i.e. the control voltage will maintain a constant value when the references signal and feedback signal are in lock. The control voltage of PLL for the schematic level is shown in the Figure.

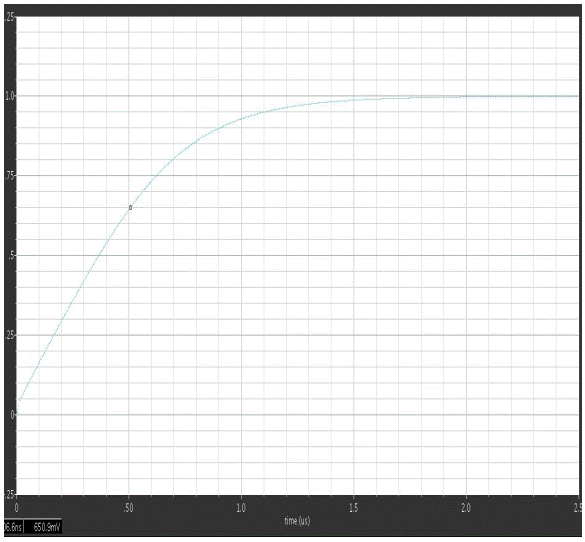

Fig 11. Variation of Control Voltage

From the figure it is clear that the control voltage saturates at 1.5us. So the lock time for the PLL is 1.5us.

So the present Phase locked loop achieved a lock in time of 1.5us with a power supply of 1V. It achieved a output frequency of oscillator as 800MHz with power dissipation of 0.5mW.

The current starved VCO design specifications are mentioned in the following table.

Table 1. VCO Design specifications.

Parameter	Value
Center frequency	800MHz
No. of inverter stages	5
Load Capacitance	65fF
Supply Voltage	1V

With different reference input noise acting such as reference source noise, data jitter, phase noise on FM input signal, etc. we have to check them as a low-pass transfer function. It is passed through multiplier which is multiplied by 2. All we can do is try to avoid making it worse with our loop. A narrow bandwidth loop filter will help to suppress high frequency noise coming into the PLL from the reference port.

The whole PLL system design specifications and parameters are shown in the table.

Table 3.3 PLL design specifications and parameters

Parameter	Value
Reference frequency	400MHz
Output frequency	800MHz
Lock in time	1.5us
Supply Voltage	1V
Divider Circuit	By 2
Capacitor (C_1)	15pf
Capacitor (C_2)	1.5pf
Resistor(R)	1.38Kohm

VI. CONCLUSION

The lock time of the PLL mainly depends upon the type of PFD architecture used and the parameters of the charge pump and loop filter. So by properly choosing the PFD architecture and adjusting the charge pump current and the loop filter component values a better lock time can be achieved. The Centre frequency of oscillation of the VCO depends upon the sizing of the transistors. The frequency deviation from the desired value can be reduced by properly choosing the transistor sizes. In this work a PLL with a better lock time is presented. The lock time of the PLL is found to be 1.5µs. The oscillator consumes a power of 0.5uW with a supply voltage of 1V. Implemented PLL is a charge pump PLL which is implemented in the Cadence 90nm CMOS technology.

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