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Design of a Low Power PLL in 90nm CMOS Technology

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***Abstract* –A PLL is a key element in clock generation and wireless transceivers. This paper presents the design of fast locking PLL. The PLL is designed in Virtuoso tool by Cadence in Analog Design Environment using GPDK 90nm CMOS technology with operating frequency of 1GHz and lock time of 100ns. A current starved VCO is exploited to bring down power consumed and achieve high frequency. Various simulations were performed using Spectre simulator. The PLL consumes total power of 4.2mW at supply voltage of 1.8V.**

Index Terms - Phase frequency detector (PFD), charge pump(CP), low pass filter, voltage controlled oscillator (VCO), phase-locked loops (PLLs).

I. Introduction

A PLL is a closed loop control system, which maintains the phase and frequency of output signal and reference signal constant. A PLL recognises the differences in phase which are in bandwidth of PLL. A PLL can be used as a clock synthesizer in which a lower frequency signal CLK_{ref} is multiplied by integer to generate a higher frequency clock CLK_{out}. The architecture of the PLL is of negative feedback type. The primary goal of the PLL is to produce a clock which has same phase and frequency as that of reference clock. Once the phase and frequency are matched PLL goes into locked state. This is accomplished by correcting error between the reference and feedback signal. A PLL has blocks as shown in Figure 1.

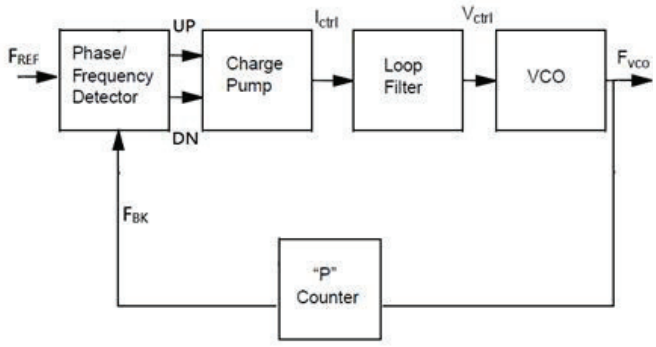

Fig.1: Basic PLL block diagram

Phase and frequency of reference and the feedback signal are compared by PFD. As per the phase and frequency difference, two output currents "UP" and "DOWN" are generated. These output currents are converted into voltage by charge pump block. The output from the CP block is given to a "Low Pass Filter" (LPF) which remove higher DC components and gives control voltage. The output of the "Voltage Controlled Oscillator" (VCO) is decided by the LPF output. When PFD produces an "UP" signal, LPF output voltage increases thus increasing the frequency of VCO output. Similarly, with the "DOWN" signal, the frequency of VCO output signal decreases. Being feedback system, this VCO output is given to the PFD through counter block.

$$H(S) = \frac{\frac{IPKVCO}{2\pi CP}}{S2 + \frac{IPKVCO}{2\pi CP}} \quad (1)$$

A. Phase Frequency Detector

The phase and frequency of the input and feedback signal are compared by PFD. As per the error between these two signals, PFD supplies two output signals "UP" and "DOWN" [9]. The implemented PFD circuit is shown in Figure 2.

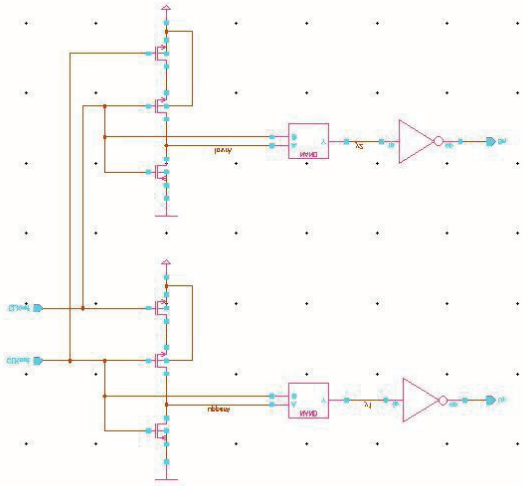

Fig. 2: PFD circuit

B. Charge Pump and Low Pass Filter

Charge pump block converts the output of a PFD block to a voltage, which controls the VCO. When the UP signal is high, positive current I_{PDI} flows through the circuit increasing

control voltage. When the down signal becomes high, negative current IPDI flows through the circuit which decreases control voltage. The output current of charge pump [3] is given below,

$$I_{PDI} = K_{PDI} \times \Delta\emptyset \quad (2)$$

$$Where\ K_{PDI} = \frac{I_{PUMP}}{2\pi}$$

$$\Delta\emptyset = \emptyset_{IN} - \emptyset_{REF}$$

The VCO control voltage is given by,

$$VctlVCO = Kf \times IPDI \quad (3)$$

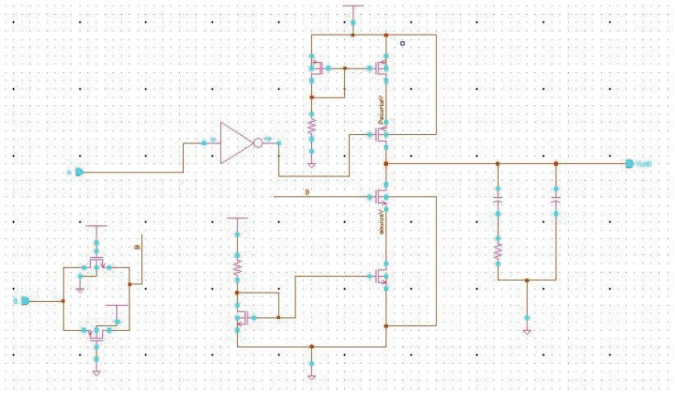

Fig. 3: CP and LPF circuit

The low pass loop filter does the conversion of charge pump current into voltage. The frequency of VCO depends on the LPF output. If charge pump current is positive then oscillation frequency increases else decreases. Fig. 3 shows the implementation of CP and LPF.

C. Voltage Controlled Oscillator

A current starved VCO is implemented in this work. The circuit is similar to basic ring oscillator with two extra transistors, one on the top of PMOS and one below NMOS. The upper and lower transistors are used to limit the current flowing through each inverter, hence called current starved VCO. The inverter stages are implemented as presented in [6], [7]. The circuit diagram of the CSVCO is as shown in Fig. 4

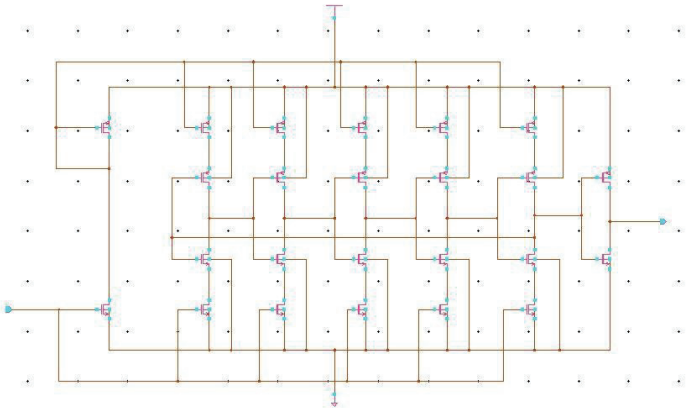

Fig.4 CSVCO circuit

D. Frequency Divider

The VCO output is given to the PFD through divide by two counter circuit. The frequency of VCO output is divided by two by this counter block. Two D-flip flops are employed to implement the counter circuit, as shown in fig. 5.

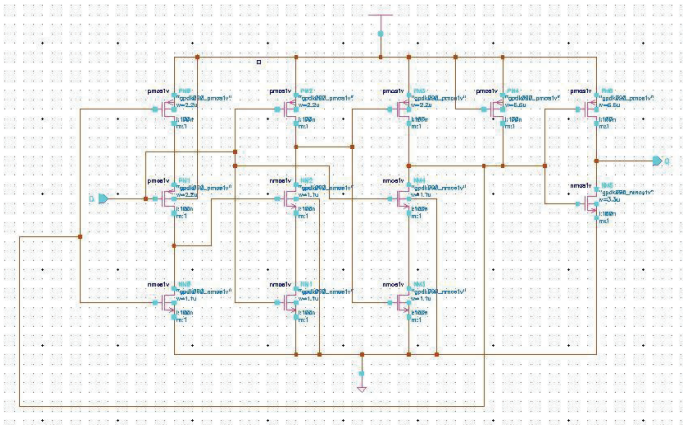

Fig. 5: Frequency divider circuit

II. SIMULATION RESULTS

The PLL is designed in Virtuoso tool by CADENCE in Analog Environment using gpdk 90nm technology. Result analysis, power consumption, lock time calculation is done using Spectre simulator. The control voltage plot of the VCO is shown in figure 9. The PLL gets locked at 100ns where both phase and frequency are matched as shown below in fig 9. The results of proposed work are better than results of [10] in terms of lock time and power consumption, where lock time is half and power consumption is three times less than [10]. The simulation results of PLL are presented in Table 1.

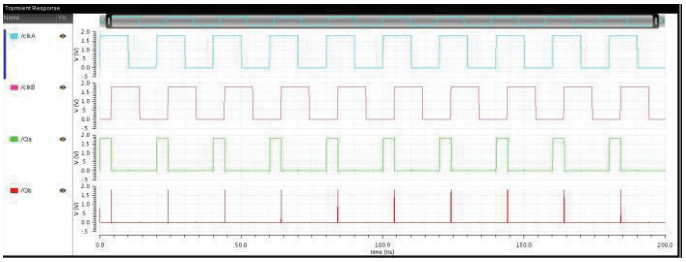

Fig.6: Output of PFD with reference signal leading the feedback signal

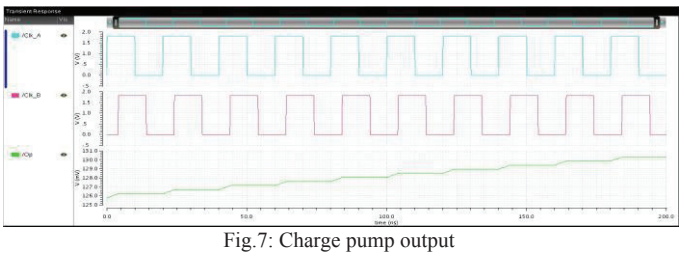

Fig.7: Charge pump output

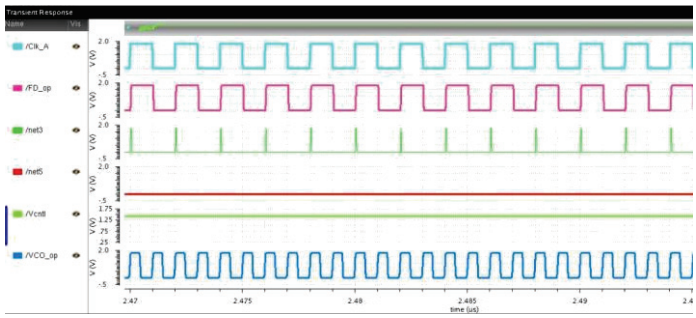

Fig.8: Waveforms of PLL in locked state

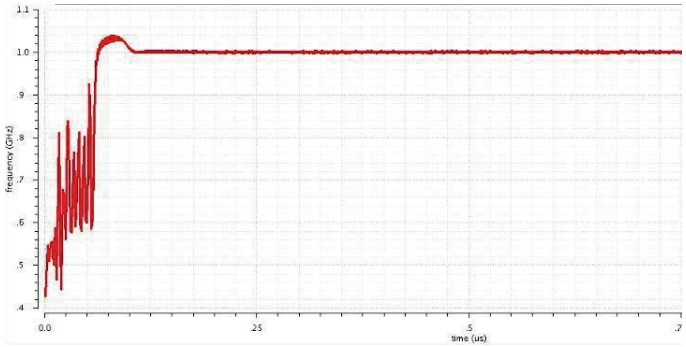

Fig. 9: Frequency of VCO

TABLE 1: SIMULATION RESULTS OF PLL

	This Work	Results of [10]
Technology	90nm	90nm
Power Supply	1.8	1.8
Lock time	100ns	280.6ns
Power Consumption	4.2mW	11.9mW

III. CONCLUSION

A PLL is implemented in Virtuoso tool by Cadence in Analog Design Environment using GPDK 90 CMOS technology with D.C. supply voltage of 1.8V. For simulation Spectre simulator is used. This work presents a PLL having a minimum lock time and comparatively low power. PLL gets locked at 100ns. VCO control voltage is 1.4V in locked state. Total power consumption is of 4.2mW. Power consumption depends on supply voltage. So, by choosing supply voltage as 1.2V and sizing the transistors, power consumption can be minimized further. Design allows high speed operation and low power consumption.

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