

Design and Implementation of 1 GHz Current Starved Voltage Controlled Oscillator (VCO) for PLL Using 90nm CMOS Technology

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Abstract— In wireless communication system the phase locked loop plays important role, specially Voltage Controlled Oscillator. It is an electronic device which is used for the purpose of generating a signal. Applications range is very vast, which includes clock generation in various microprocessors to carrier synthesis in cellular telephones, requiring a large range of different oscillators/signal generation topologies and the performance parameters differs as the need changes . VCO can be designed and built using many circuit techniques. This paper presents one of the ways to design and implementation of CMOS voltage controlled oscillators (VCO) for pll. A VCO is an oscillator circuit, where the control voltage controls the oscillator output frequency. In this paper CSVCO is has been designed Cadence Design Suite using GPDK 90nm CMOS Technology with supply voltage 1.8v. Intern Virtuoso Analog Design Environment tool of Cadence have used to design and simulate schematic. Simulation results are calculated for all process corners, temperature (-40°C to +100°C).

Keywords— CMOS VCO, Current-Starved VCO, Phase locked loop.

I. INTRODUCTION

In a wireless communication system the quality of the communication link is determined by the characteristics of the VCO, in today's wireless communication systems higher frequency range is required by the VCOs. VCOs using CMOS technology used for low frequency applications, but in Case of submicron processes have allowed CMOS oscillators to achieve higher frequencies in the Gigahertz range [2]. This range is made possible with the help of automatic swing control. VCO can be built by using many circuit techniques [5]. In this paper designing of CMOS VCO using cadence tool. There are so many design requirements for VCO, which are phase stability, large electrical tuning range, large gain factor, capability of accepting wideband modulation, cost but the important factor in designing the VCO is the linearity of the device, on the basis of which the comparison between CMOS VCOs is described [6]. With reference to digital phones that use the circuits, low power consumption, small

size and low fabrication costs is one of the important design factors in low power VLSI design. In order to achieve a higher quality factor, CMOS oscillators is designed in the form of Ring Oscillators [3], [7].

II. CURRENT STARVED VCO

Current starved Voltage Controlled Oscillator (CSVCO) is designed using ring oscillator and its operation is similar to that in the schematic circuit shown in Figure 1, MOSFETs M2 and M3 transistors together operate as an inverter, while MOSFETs M1 and M4 transistors together operate as the current sources. The transistors M1 and M4, limits the current available for the inverter, M2 and M3 transistors. In other words, the inverter is starved for the current. The MOSFET's M5 and M6 drain currents are same and are set through the input control voltage. The currents in M5 and M6 transistors are mirrored form of each inverter or current source stage. The upper PMOS transistors are connected via the gate of M6 and the source voltage is applied to the gates of all lower NMOS transistor in [4].

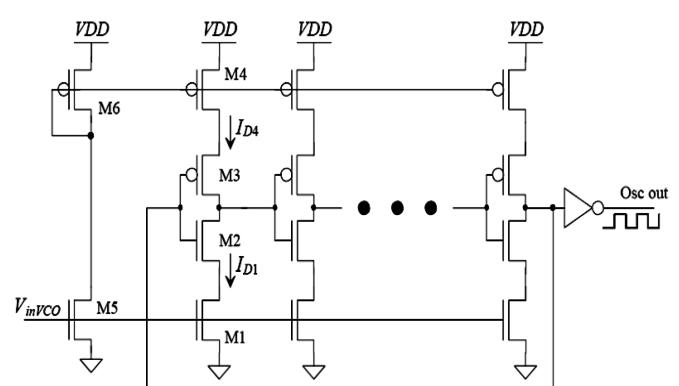


Figure 1 Current-Starved VCO

III. DESIGN OF VCO

To determine the design equations for the current-starved VCO, the total capacitance on the drains M2 and M3 is given by

$$\begin{aligned} C_{tot} &= C_{out} + C_{in} \\ C_{tot} &= C_{ox}(W_p L_p + W_n L_n) + \frac{3}{2} C_{ox}(W_p L_p + W_n L_n) \end{aligned} \quad (1)$$

Equation 1 gives the output and input capacitances of the inverter. The equation can be written in more useful form as

$$C_{tot} = \frac{5}{2} C_{ox}(W_p L_p + W_n L_n) \quad (2)$$

The time taken to charge C_{tot} from zero to V_{SP} with the constant current I_{D4} is given by

$$t_1 = C_{tot} \cdot \frac{V_{SP}}{I_{D4}} \quad (3)$$

Where the time taken to discharge C_{tot} from VDD to V_{SP} is given by

$$t_2 = C_{tot} \cdot \frac{VDD - V_{SP}}{I_{D1}} \quad (4)$$

If $I_{D4} = I_{D1} = I_D$ (which is labelled as $I_{Dcenter}$ when $V_{inVCO} = VDD/2$), then the sum of t_1 and t_2 is simply

$$t_1 + t_2 = C_{tot} \cdot \frac{VDD}{I_D} \quad (5)$$

The oscillation frequency to the current starved VCO for N (an odd number ≥ 5) of stages is

$$f_{osc} = \frac{1}{N(t_1 + t_2)} = \frac{1}{N \cdot C_{tot} \cdot VDD} \quad (6)$$

The central frequency (f_{centre}) is given in equation 3.6 for the VCO when $I_D = I_{Dcenter}$. The VCO stops oscillating and neglecting the sub-threshold current of the device, and hence $V_{inVCO} < V_{THN}$. Therefore, $V_{min} = V_{THN}$ and $f_{min} = 0$.

The maximum VCO oscillation frequency, f_{max} , is determined by finding I_D when $V_{inVCO} = VDD$. At the maximum frequency, $V_{max} = VDD$.

Output of the current starved VCO normally has its output buffered through one or two inverters. While attaching to a large load capacitance on the output of the VCO can

significantly affect the oscillation frequency else lower the gain of the oscillator enough to kill oscillations altogether.

The average current drawn by the VCO is given by

$$I_{avg} = N \cdot \frac{VDD \cdot C_{tot}}{T} = N \cdot VDD \cdot C_{tot} \cdot f_{osc} \quad (7)$$

Or

$$I_{avg} = I_D \quad (8)$$

The average power dissipated by the VCO is given by

$$P_{avg} = I_{avg} \cdot VDD = VDD \cdot I_D \quad (9)$$

The power dissipation in the mirror MOSFETs M5 and M6 is also included then the power is increased from that given by the equation 9, as we know that $I_D = I_{D5} = I_{D6}$. For low power dissipation, the current I_D should be kept low, or in other words oscillation frequency is low [4].

Table 1: Design parameters of the CSVCO circuit

Parameter	Value
Width of Current starved PMOS (W_{PCS})	$2.33\mu m$
Width of Current Starved NMOS(W_{nCS})	140nm
Width of PMOS in Inverter(W_p)	$2.44\mu m$
Width of NMOS in Inverter(W_n)	150nm
LPCS = LnCS = LP = Ln = L	100nm

IV. SIMULATION RESULT OF CURRENT STARVED VCO

The actual clock generated by a PLL arrives from the voltage controlled oscillator (VCO), which generates the periodic oscillation. The frequency of this oscillation can be controlled by modulating control voltage. In Phase Locked Loop, the control voltage corresponds to some filtered form of the phase error. With response to this, the VCO adjusts its frequency. As the Voltage Controlled Oscillator frequency is reduced by the control voltage and the phase error is driven towards zero.

The simulation of current starved VCO is performed on Cadence Design Suite which is shown in figure 2. Here control voltage V_{inVCO} set to 900mV. For the required condition of oscillation feedback is driven back before the inverter stage. The results displayed in figure 1.3. For an output frequency of 1 GHz, the input voltage, V_{inVCO} , was set to 900mV.

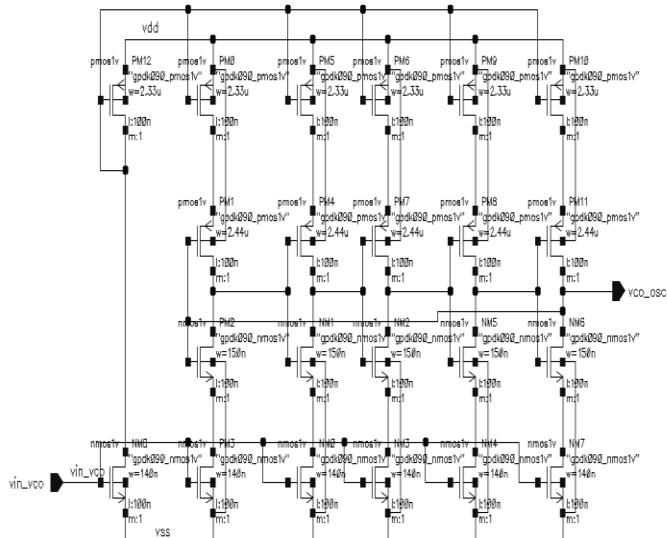


Figure 2. Schematic of Current Starved VCO

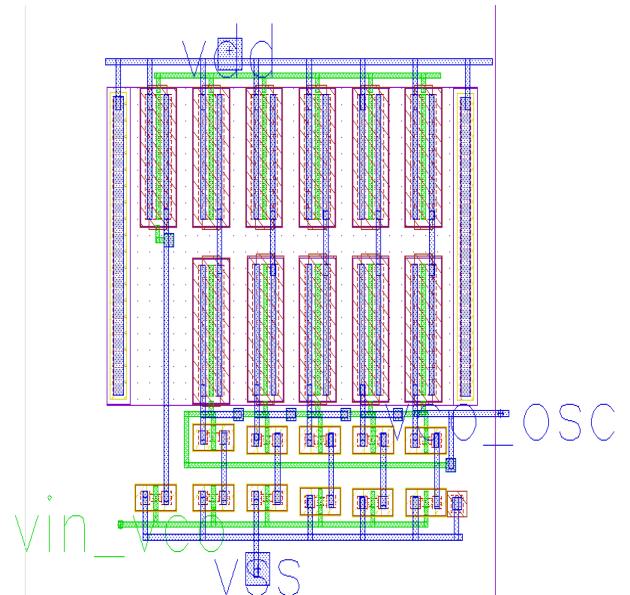


Figure 5. Layout of Current-Starved VCO

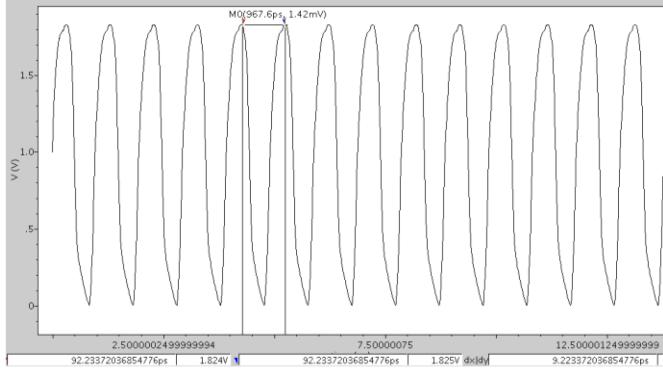
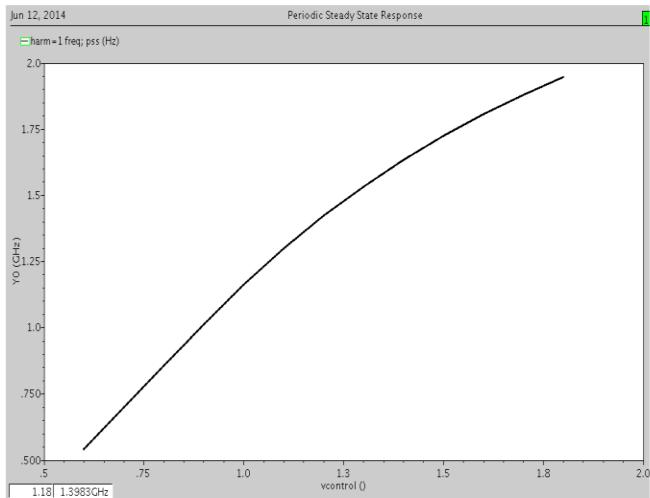
Figure 3. Simulation result of Current Starved VCO at $V_{inVCO} = 900\text{mV}$ 

Figure 4. Transfer characteristic of current starved VCO

The applied input voltage is varied from 0 to 1.8V, in steps of 0.1V, and then time period is calculated at different values for the obtained voltages from the waveform result. Frequency is calculated by taking inverse of the time period. The Table 2 shows values of the time periods and frequencies at different values of voltages. The transfer characteristic of the current starved VCO is given in figure 4, here the curve which is almost linear as predict at the time of designing.

The problem with this design the output oscillation frequency is not linearly related to control voltage (easy to verify using the simulation result shown in figure 3 above). Having a nonlinear VCO gain can greatly reduce the quality of the performance of the PLL (Phase Locked Loop).The output of the PLL can jitter or it may not lock at all when the VCO gain is nonlinear [4].

Table 2: Variation of Frequency with Input Control Voltage (Vin VCO)

Control Voltage (VC)(in volt)	Frequency of Oscillation (f) (in MHz)
0.1	23.29
0.2	87.48
0.3	179.37
0.4	265.32
0.5	406.83
0.6	675.21
0.7	715.81
0.8	851
0.9	1050
1.0	1140
1.1	1290
1.2	1440
1.3	1530
1.4	1697
1.5	1745
1.6	1836
1.7	1879
1.8	1940

Table 3: Simulation parameters of CSVCO

Parameter	Schematic Result
Frequency(f)	1.012 GHz
Average Current	214.8 uA
Phase Noise 1GHz offset	-138 dBc/Hz
Power(P)	386.64 uW

Table 4: Frequency, Average Current, Total Power dissipation at different temperatures (vdd=1.8) Process Corners Typical (NN).

Temperature (degree Celsius)	Frequency in Hz	Average Current (uA)	Power consumption (uW)
-50	1.0405G	287.7	517.86
-40	1.345G	276.7	498.06
-30	1.288G	266.1	478.8
-20	1.233G	256.08	460.94
-10	1.182G	246.5	443.7
0	1.133G	273.3	427.14
10	1.087G	228.6	411.48
20	1.044G	220.4	396
30	1.002G	212.4	382.32
40	962.1M	204.8	368.6
50	924.5M	197.6	354.6
60	913.3M	190.7	343.26
70	854.7M	184.0	331.2
80	822M	177.7	319.86
90	812.7M	171.7	309.06
100	782M	165.9	298.62

Table 5: Frequency, Average Current, Total Power dissipation for different process corners (vdd=1.8) (Temp=27).

Process Corners	Frequency in Hz	Average Current (uA)	Power consumption (uW)
Typical(NN)	1.025G	214.8	386.64
Slow Slow(SS)	740M	149.5	269
Slow Fast(SF)	748.5M	159.37	286.86
Fast Slow(FS)	1.313G	265.3	477.54
Fast Fast(FF)	1.261G	283.3	509.94

V. CONCLUSION

In this paper we observed that in current starved voltage controlled oscillator (VCO) generates 1GHz frequency at input control voltage (V_{in} VCO) of 900mV. Since Phase locked loop (PLL) is widely used in wireless communication and communication systems, hence we can generate any desire frequency based on application requirements.

VI. REFERENCES

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