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MAX86178

Ultra-Low-Power, Clinical-Grade Vital-Sign AFE

PRELIMINARY

General Description

The MAX86178 is a highly integrated, multiple vital-sign monitoring device with a complete photoplethysmogram (PPG), electrocardiogram (ECG) and biopotential (BioZ) analog front end (AFE) for wearable applications. The MAX86178 offers high performance for wellness and clinical applications with low power for long battery life.

The PPG data acquisition system supports up to 6 LEDs and 4 photodiode inputs. The LEDs are programmable from two high-current, 8-bit LED drivers. The receive path has two low-noise, high-resolution readout channels that each include independent 20-bit ADCs and industry-leading ambient light cancellation (ALC) circuits, producing the highest performing integrated optical data acquisition system on the market today.

The ECG channel has EMI filtering, internal lead biasing, right-leg drive, and extensive calibration voltages for built-in self-test. The ECG channel also has high-input impedance, low noise, high CMRR, programmable gain, an anti-aliasing low-pass filter, and a high-resolution ADC. It is designed to meet IEC 60601-2-47 Ambulatory ECG Systems monitoring compliance requirements.

The BioZ receive channel has EMI filtering and extensive calibration features. The BioZ receive channel also has high input impedance, low noise, programmable gain, low-pass and high-pass filter options, and a high-resolution ADC. There are several modes for generating input stimulus: balanced square-wave source/sink current, sine-wave current, and both sine-wave and square-wave voltage stimuli. A wide range of stimulus magnitudes and frequencies is available.

The MAX86178 has DC and AC lead-off detection, a flexible timing system, and a PLL. All three sensor channels are synchronized. The MAX86178 is available in a 7 x 7 49-bump wafer-level package (WLP) with package dimensions of 2.77mm x 2.57mm, and operates over -40°C to +85°C temperature range.

Applications

- Wearable Vital-Sign Monitors
- Ambulatory Heart Monitors
- Pulse-Oximetry Devices
- Smart-Clothing Applications
- Impedance Cardiography/Hemodynamic Monitors
- Single- and Multi-Frequency Bioimpedance Analysis
- Pulse Arrival Time (PAT), Pulse Travel Time (PTT), Pulse Wave Velocity (PWV) Assessments

Benefits and Features

PPG

- Dual-Channel Optical Data-Acquisition System
- 115dB SpO₂ System SNR; 112dB SNR at 16µA
- Excellent Ambient Range and Rejection Capability
 - > 200µA Ambient Photodetector Current
 - > 90dB Ambient Rejection at 120Hz with Averaging

ECG

- Clinical Grade ECG Acquisition System
 - 15.3 ENOB with 0.72µVRMS (0.05Hz to 40Hz)
 - 230fARMS Input-Current Noise (0.05Hz to 40Hz, +25°C)
- Fully Differential Signal with CMRR > 110dB at 50Hz and 60Hz
- High Input Impedance > 1GΩ for Extremely Low Common-to-Differential Mode Conversion
- High DC-Differential Input Range of ±1300mV (typ 1.8V) Allows a Wide Variety of Electrodes to be Used
- High AC-Dynamic Range of 200mVp-p Prevents Saturation Due to Motion, or Varying Half-Cell Potentials

BIOZ

- High-Performance BioZ Data Acquisition System
- Low-Noise BioZ Receive Channel (17 ENOB, 0.16µVRMS)
- Sine-Wave, Square-Wave, Current and Voltage Stimulus (16Hz to 806kHz)
- BIA/BIS Measurement with High Absolute Resistance and Reactance Accuracy

SYSTEM

- Ultra-Low-Power Systems for Wearable Devices
- DC and AC Lead-Off Detect Capability
- Shutdown Current of 0.5µA (typ)
- 256-Word FIFO for ECG, PPG, and BioZ
- Flexible Interrupt and Multi-AFE Synchronization
- FIFO Timing Data Allows Synchronized PPG, ECG, and BioZ

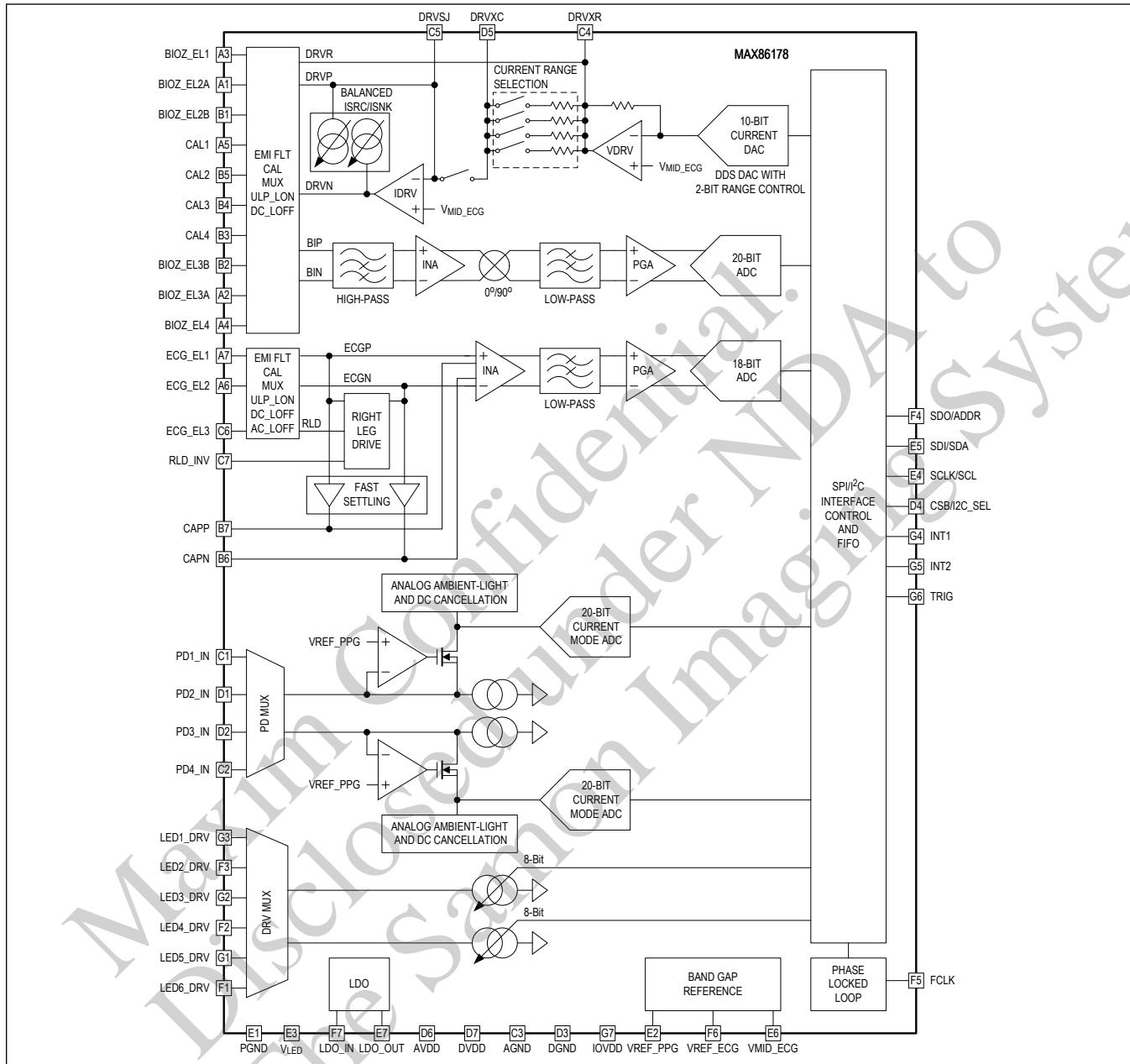
[Ordering Information](#) appears at end of data sheet.



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Simplified Block Diagram



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Absolute Maximum Ratings

LDO_IN to AGND	-0.3V to +6.0V	TRIG, FCLK, INT1, INT2 to DGND	-0.3V to +6.0V
IOVDD to DGND.....	-0.3V to +6.0V	SDO/ADDR to DGND	-0.3V to (IOVDD + 0.3V)
AVDD to AGND	-0.3V to +2.2V	Output Short-Circuit Duration.....	Continuous
DVDD to DGND	-0.3V to +2.2V	All Other Pins to AGND.....	-0.3V to +2.2V
V _{LED} to PGND.....	-0.3V to +6.0V	Continuous Current into Any Pin.....	±50mA
AVDD to DVDD	-0.3V to +0.3V	Operating Temperature Range	-40°C to +85°C
DGND, PGND to AGND	-0.3V to +0.3V	Junction Temperature	+150°C
PDm_IN to AGND.....	-0.3V to +2.2V	Storage Temperature Range	-65°C to +150°C
LEDn_DRV to PGND	-0.3V to (V _{LED} + 0.3V)	Lead Temperature (Soldering, 10sec)	+300°C
CSB/I2C_SEL, SCLK/SCL, SDI/SDA to DGND	-0.3V to +6.0V	Soldering Temperature (Reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

49 WLP

Package Code	N492A2+1
Outline Number	21-100520
Land Pattern Number	Refer to Application Note 1891
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	48.76°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](#). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](#).

Electrical Characteristics

(V_{LDO_IN} = 3.7V, V_{LED} = 3.7V, V_{AVDD} = 1.8V, V_{DVDD} = 1.8V, V_{IOVDD} = 1.8V, T_A = +25°C, MIN/MAX are from T_A = -40°C to +85°C, unless otherwise noted.) (Notes 1, 2,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
LDO_IN Supply Voltage	V _{LDO_IN}	Guaranteed by DC PSRR	2.3	5.5		V
LDO_OUT Voltage	V _{LDO_OUT}	V _{LDO_IN} > 2.3V, LDO_OUT Load Current = 10mA.	1.70	1.8	1.95	V
IOVDD Supply Voltage	V _{IOVDD}	Guaranteed by Digital I/O V _{IL} and V _{IH} Thresholds	1.70	5.5		V
V _{LED} Supply Voltage (Note 3)	V _{LED}	Guaranteed by DC PSRR	3.1	5.5		V
AVDD Supply Voltage	V _{AVDD}	Guaranteed by DC PSRR	1.7	1.8	2.0	V
DVDD Supply Voltage	V _{DVDD}	Guaranteed by Scan Test	1.7	1.8	2.0	V

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Electrical Characteristics (continued)

($V_{LDO_IN} = 3.7V$, $V_{LED} = 3.7V$, $V_{AVDD} = 1.8V$, $V_{DVDD} = 1.8V$, $V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, MIN/MAX are from $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Notes 1, 2,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY / PPG SUPPLY CURRENT						
PPG Supply Current ($I_{AVDD} + I_{DVDD}$)	I _{PPG}	Single Channel, One Meas/Frame (Note 4a)	FR = 512fps	91	140	µA
			FR = 64fps	16		
			FR = 8fps	7.5		
		Single Channel, Four Meas/Frame (Note 4a)	FR = 512fps	325	450	
			FR = 64fps	52		
			FR = 8fps	20		
		Dual Channel, One Meas/Frame (Note 4b)	FR = 512fps	140	210	
			FR = 64fps	23		
			FR = 8fps	9.5		
		Dual Channel, Four Meas/Frame (Note 4b)	FR = 512fps	530	672	
			FR = 64fps	87		
			FR = 8fps	30		
V _{LED} Supply Current	I _{LED}	Single Channel, One Meas/Frame (Note 4a)	FR = 512fps	840	970	µA
			FR = 64fps	135		
			FR = 8fps	40		
POWER SUPPLY / ECG SUPPLY CURRENT						
Biopotential Channel Supply Current ($I_{AVDD}+I_{DVDD}$)	I _{BPC}	ECG Mode (Note 5)	RLD Amplifier Disabled, ECG Lead Bias = 100MΩ, M = 128, ECG_FDIV = 16, ECG_NDIV = 8, SR_ECG = 128sps	105	150	µA
			RLD Enabled, M = 128, ECG_FDIV = 16, ECG_NDIV = 8, SR_ECG = 128sps	107	150	
			RLD Amplifier Disabled, ECG Lead Bias = 100MΩ, M = 125, ECG_FDIV = 16, ECG_NDIV = 8, SR_ECG = 250sps	105	150	

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Electrical Characteristics (continued)

($V_{LDO_IN} = 3.7V$, $V_{LED} = 3.7V$, $V_{AVDD} = 1.8V$, $V_{DVDD} = 1.8V$, $V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, MIN/MAX are from $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Notes 1, 2,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY / BIOZ SUPPLY CURRENT						
BIA Supply Current ($I_{AVDD} + I_{DVDD}$)	I_{BIOZ}	BIA/BIS Conditions (Note 6a)	F_BIOZ = 1kHz, SR_BIOZ = 62.5sp, PLL_CLK = 16.384MHz	880		µA
			F_BIOZ = 50.048kHz, SR_BIOZ = 48.875sp, PLL_CLK = 12.812MHz	1030	2250	µA
			F_BIOZ = 50.048kHz, SR_BIOZ = 48.875sp, PLL_CLK = 12.812MHz, REF_CLK_SEL = 0	1020		µA
			F_BIOZ = 100.096kHz, SR_BIOZ = 48.875sp, PLL_CLK = 12.812MHz	1025		µA
			F_BIOZ = 249.856kHz, SR_BIOZ = 61sp, PLL_CLK = 15.991MHz	1100	2350	µA
			F_BIOZ = 499.712kHz, SR_BIOZ = 61sp, PLL_CLK = 15.991MHz	1130		µA
Respiration Supply Current ($I_{AVDD} + I_{DVDD}$)	I_{RESP}	Respiration Conditions (Note 6b)	F_RESP = 32kHz, SR_RESP = 62.5sp, PLL_CLK = 8.192MHz , RESP_EN = 1	325	425	µA
			F_BIOZ = 32kHz, SR_BIOZ = 31.25sp, PLL_CLK = 4.096MHz, BIOZ_DRV_MODE = H-Bridge, DRVP and DRVN unconnected	150		µA

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($V_{LDO_IN} = 3.7V$, $V_{LED} = 3.7V$, $V_{AVDD} = 1.8V$, $V_{DVDD} = 1.8V$, $V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, MIN/MAX are from $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Notes 1, 2,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ICG Supply Current ($I_{AVDD} + I_{DVDD}$)	I_{ICG}	ICG Conditions (Note 6c)		1925		μA
GSR/EDA Supply Current ($I_{AVDD} + I_{DVDD}$)	I_{GSR_EDA}	GSR/EDA Conditions (Note 6d)		220		μA
POWER SUPPLY / ECG + BIOZ SUPPLY CURRENT						
ECG + BIOZ Supply Current ($I_{AVDD} + I_{DVDD}$)		Respiration and ECG Conditions (Note 7)		285	450	μA
POWER SUPPLY / PPG + ECG + BIOZ SUPPLY CURRENT						
PPG + ECG + BIOZ Supply Current ($I_{AVDD} + I_{DVDD}$)		Respiration, ECG, and PPG Conditions (Note 8)		435		μA
POWER SUPPLY / IOVDD SUPPLY CURRENT						
IOVDD Supply Current	I_{IOVDD}	SCLK = 24MHz		11.5	17	μA
POWER SUPPLY / SHUTDOWN CURRENT						
Shutdown Current ($I_{AVDD} + I_{DVDD}$)	I_{SHDN}	$T_A = +25^\circ C$	1.2	3		μA
				25		
V_{LED} Shutdown Current	I_{VLED_SHDN}	$T_A = +25^\circ C$		0.25		μA
				0.5		
IOVDD Shutdown Current	I_{IOVDD_SHDN}			0.5		μA
Lead-On Detect Current		$EN_ECG_LON = 1$ or $EN_BIOZ_LON = 1$	3.6	28		μA
PPG CHARACTERISTICS / READOUT CHANNEL						
ADC Resolution			20			bits
INL	INL_{RX}	$MEASx_TINT = 117.0\mu s$		± 10		LSB
		$MEASx_TINT = 14.6\mu s$		± 40		
DNL	DNL_{RX}	$MEASx_TINT = 117.0\mu s$		± 3		LSB
		$MEASx_TINT = 14.6\mu s$		± 10		
ADC Full-Scale Input Current	I_{FS}	$MEASx_PPGy_ADC_RGE = 0x0$	4.0			μA
		$MEASx_PPGy_ADC_RGE = 0x1$	8.0			
		$MEASx_PPGy_ADC_RGE = 0x2$	16.0			
		$MEASx_PPGy_ADC_RGE = 0x3$	32.0			

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Electrical Characteristics (continued)

($V_{LDO_IN} = 3.7V$, $V_{LED} = 3.7V$, $V_{AVDD} = 1.8V$, $V_{DVDD} = 1.8V$, $V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, MIN/MAX are from $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Notes 1, 2,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Offset DAC Full-Scale Current		MEASx_PPGy_DACOFF = 0xE		30.0		µA
ADC Integration Time	t _{INT}	MEASx_TINT = 0x0		14.6		µs
		MEASx_TINT = 0x1		29.2		
		MEASx_TINT = 0x2		58.6		
		MEASx_TINT = 0x3		117.1		
Minimum Free-Running Frame Rate		CLK_FREQ_SEL = 32.768kHz		1		fps
Maximum Free-Running Frame Rate		CLK_FREQ_SEL = 32.768kHz		2048		fps
Internal Power-Up Time				200		µs
ADC Clock Frequency			9.8	10	10.2	MHz
DC Ambient-Light Rejection Range	ALR	ALC_OVF_ENx = 1	0		200	µA
Dynamic Ambient-Light Rejection		I _{EXPOSURE} = 1µA, I _{AMBIENT} = 1µA DC with 0.4µAp-p 120Hz sinewave		80		dB
DC Ambient-Light Rejection		I _{EXPOSURE} = 1µA, I _{AMBIENT} = 1µA and 30µA		0.5		nA
Dark Current Offset	DC_O	ALC = ON, PDm_BIAS = 0x1, MEASx_TINT = 117.0µs		±1		Counts
Dark Current-Input Referred Noise		MEASx_TINT = 14.6µs		212		pARMS
		MEASx_TINT = 29.2µs		150		
		MEASx_TINT = 58.6µs		106		
		MEASx_TINT = 117.1µs		75		
V _{DD} DC PSR		V _{AVDD} , V _{DVDD} = 1.7V to 2.0V (Internal Loop Back mode)	MEASx_TINT = 14.6µs		0.9	%FS/V
			MEASx_TINT = 29.2µs		0.8	
			MEASx_TINT = 58.6µs		0.7	
			MEASx_TINT = 117.1µs	0.7	1.25	
PPG CHARACTERISTICS / LED DRIVER						
LED Current Resolution				8		bits
Driver DNL	DNL _{TX}	MEASx_LED_RGE = 0x3	-1		+1	LSB
Driver INL	INL _{TX}	MEASx_LED_RGE = 0x3		±1		LSB

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Electrical Characteristics (continued)

($V_{LDO_IN} = 3.7V$, $V_{LED} = 3.7V$, $V_{AVDD} = 1.8V$, $V_{DVDD} = 1.8V$, $V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, MIN/MAX are from $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Notes 1, 2,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Full-Scale LED Current	I_{LED}	MEASx_DRVy_PA = 0xFF	MEASx_LED_RGE = 0x0	32		mA
			MEASx_LED_RGE = 0x1	64		
			MEASx_LED_RGE = 0x2	96		
			MEASx_LED_RGE = 0x3	116	128	140
LED Driver Rise Time		MEASx_DRVy_PA = 0xFF, 10% to 90%, All LED Range Settings		3		μs
LED Driver Fall Time		MEASx_DRVy_PA = 0xFF, 10% to 90%, All LED Range Settings		3		μs
Minimum Output Voltage	V_{OL}	MEASx_DRVy_PA = 0xFF, 95% of the Desired LED Current	MEASx_LED_RGE = 0x0	170		mV
			MEASx_LED_RGE = 0x1	260		
			MEASx_LED_RGE = 0x2	380		
			MEASx_LED_RGE = 0x3	500	800	
LED Driver DC V_{LED} PSR		MEASx_DRVy_PA = 0xFF, $V_{LEDn_DRV} = 1.2V$, $V_{LED} = 3.1V$ to 5.5V	MEASx_LED_RGE = 32mA	± 16		$\mu A/V$
			MEASx_LED_RGE = 64mA	± 13		$\mu A/V$
			MEASx_LED_RGE = 96mA	± 14		
			MEASx_LED_RGE = 128mA	-200	± 18	+200
LED Driver Compliance Interrupt Threshold		MEASx_LED_RGE = 0x0	115	148	180	mV
		MEASx_LED_RGE = 0x1	255	287	320	
		MEASx_LED_RGE = 0x2	395	425	460	
		MEASx_LED_RGE = 0x3	530	560	600	
ECG CHARACTERISTICS / READOUT CHANNEL						
Input-Voltage Range	V_{ECGP} , V_{ECGN}	$f_{IN} = 64Hz$, $V_{IN} = 12mV_{P-P}$, shift from gain at $0.76V < 2.5\%$	0.3	AVDD-0.6		V
		$f_{IN} = 64Hz$, $V_{IN} = 12mV_{P-P}$, shift from gain at $0.76V < 2.5\%$		0.15 to 1.35		
DC Differential-Input Range	$V_{ECGP-ECGN}$	$f_{IN} = 64Hz$, $V_{IN} = 12mV_{P-P}$, shift from gain at $0V < 2.5\%$	-1000	+1000		mV
AC Differential-Input Range	V_{IN}	$f_{IN} = 64Hz$, $INA_GAIN = 10V/V$, THD < 0.3%	170	195		mV_{P-P}

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($V_{LDO_IN} = 3.7V$, $V_{LED} = 3.7V$, $V_{AVDD} = 1.8V$, $V_{DVDD} = 1.8V$, $V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, MIN/MAX are from $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Notes 1, 2,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Input Range (Note 9)	CMRR	$f_{IN} = 64Hz$, Electrode Offset = $\pm 300mV$, $V_{CM} = 0.76V$, $T_A = +25^\circ C$	0Ω Source Impedance	100	114	dB
			ETI Impedance Mismatch as Described in Note 10		78	
			ETI Impedance Mismatch as Described in Note 10. RLD Closed Loop Gain = 97V/V.	100	107	
Input-Referred Noise (Note 9)		$T_A = 25^\circ C$	BW = 0.05Hz to 150Hz	0.99	1.6	μV_{RMS}
			BW = 0.05Hz to 150Hz	6.00	12	μV_{P-P}
			BW = 0.05Hz to 40Hz	0.72	1.3	μV_{RMS}
			BW = 0.05Hz to 40Hz	3.99	7.9	μV_{P-P}
			BW = 0.05Hz to 40Hz, ECG_INA_GAIN = 10V/V	0.95	1.9	μV_{RMS}
			BW = 0.05Hz to 40Hz, ECG_INA_GAIN = 10V/V	5.26	10.6	μV_{P-P}
Input-Current Noise Density		100MΩ external bias resistor to V_{MID_ECG}		37		fA/\sqrt{Hz}
ECGP and ECGN Input-Leakage Current		$V_{ECGP/N} = AVDD - 0.2V$ or $AGND + 0.2V$, $T_A = +25^\circ C$	-500	± 50	+500	pA
		$V_{ECGP/N} = AVDD - 0.2V$ or $AGND + 0.2V$	-2500		+2500	
Input Impedance (Note 9)	INA	Differential, $f_{IN} = 8Hz$		1.0		GΩ
		Differential, $f_{IN} = 64Hz$		0.74		
		Common-Mode, $f_{IN} = 8Hz$		14		
		Common-Mode, $f_{IN} = 64Hz$		5		
Total Harmonic Distortion	THD	$f_{IN} = 64Hz$, Electrode Offset = $\pm 300mV$	$V_{IN} = 65mV_{P-P}$	0.035		%
			$V_{IN} = 30mV_{P-P}$		0.3	
Biopotential-Channel Gain Setting	GCH	Selected by ECG_INA_GAIN and ECG_PGA_GAIN		2.5 to 960		V/V

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($V_{LDO_IN} = 3.7V$, $V_{LED} = 3.7V$, $V_{AVDD} = 1.8V$, $V_{DVDD} = 1.8V$, $V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, MIN/MAX are from $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Notes 1, 2,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Biopotential-Channel Gain Error		$f_{IN} = 64Hz$, $V_{IN} = 12mV_{P-P}$, $ECG_PGA_GAIN = X$	$ECG_INA_RGE = 0x0, 0x1, ECG_INA_GAIN = 0x0, 0x1, 0x2$	-2.5	± 1.8	+2.5	%
			$ECG_INA_RGE = 0x2, 0x3, ECG_INA_GAIN = 0x0, 0x1, 0x2$	-5.0	± 2.8	+5.0	
			$ECG_INA_RGE = X, ECG_INA_GAIN = 0x3$		± 5.0		
Biopotential-Channel Input-Referred Offset Voltage		$ECG_INA_GAIN = 20V/V$		± 400		μV	
ADC Resolution				18		bits	
ADC Sample Rate				64 to 2048		sps	
CAPP to CAPN Impedance	R_{HPF}	$f_{HPF_3dB} = 1/(2\pi \times R_{HPF} \times C_{HPF})$, $C_{HPF} = \text{Capacitance between CAPP and CAPN}$, $ECG_IMP_HI = 0$	240	400	650	$k\Omega$	
Analog High-Pass Filter Slew Current		Fast Recovery Enabled		100		μA	
		Fast Recovery Disabled		0.3			
Biopotential-Channel Power-Supply Rejection	$PSRR$	Lead Bias Disabled, $V_{ECGP} = V_{ECGN} = V_{MID_EC}$, Change in Input Referred Offset	$V_{LDO_IN} = 2.3V$ to $5.5V$,	94	114	dB	
			$V_{LDO_IN} = AGND$, $V_{AVDD} = V_{DVDD} = 1.7V$ to $2.0V$	84	97		

ECG CHARACTERISTICS / ECG MUX / DC/AC LEAD-OFF DETECTION

Full-Scale Current		Selected by ECG_LOFF_IMAG	5 to 400	nA
Full-Scale Current Accuracy		$ECG_LOFF_IMAG = 400nA$, $T_A = 25^\circ C$	± 5	$\%$
			-30 to +30	
Comparator Threshold	$V_{ECG_TH_H}$, $V_{ECG_TH_L}$	Selected by ECG_LOFF_THRESH	V_{MID_EC} $G \pm 25$	V_{MID_EC} $G \pm 400$
Comparator-Threshold Accuracy		$ECG_LOFF_THRESH = \pm 400mV$	-12.5 to +12.5	%
Full-Scale Electrode Resistance		$ECG_LOFF_IMAG = 400nA$, $ECG_LOFF_THRESH = \pm 25mV$	62.5	$k\Omega$
		$ECG_LOFF_IMAG = 5nA$, $ECG_LOFF_THRESH = \pm 400mV$	80	$M\Omega$
AC Lead-Off Frequency		Selected by ECG_LOFF_FREQ and ECG_ADC_CLK (see Timing Subsystem)	74 to 8192	Hz

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($V_{LDO_IN} = 3.7V$, $V_{LED} = 3.7V$, $V_{AVDD} = 1.8V$, $V_{DVDD} = 1.8V$, $V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, MIN/MAX are from $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Notes 1, 2,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ECG CHARACTERISTICS / ECG MUX / LEAD BIAS						
Lead-Bias Impedance		ECG Lead-Bias Enabled to V_{MID_ECG} or V_{RLD} (see the RLD_RBIAS bit)	ECG_RBIAS_VAL UE = 0x0	50		$M\Omega$
			ECG_RBIAS_VAL UE = 0x1	100		
			ECG_RBIAS_VAL UE = 0x2	200		
Lead-Bias Voltage		ECG Lead-Bias Enabled, RLD_RBIAS = 0	0.66	0.76	0.86	V
ECG CHARACTERISTICS / ECG MUX / CALIBRATION PULSE						
Calibration-Voltage Magnitude		Single-Ended	ECG_CAL_MAG = 0x0	0.25		mV
			ECG_CAL_MAG = 0x1	0.5		
Calibration-Voltage Magnitude Error		ECG_CAL_MAG = 0x1, Bipolar Mode (Note 11)	TA = $+25^\circ C$	-3	$+3$	%
				-6	$+6$	
Calibration-Voltage Frequency		Selected by ECG_CAL_FREQ		0.0156 to 256		Hz
Calibration-Voltage Pulse-Time		ECG_CAL_DUTY = 0x0, Selected by ECG_CAL_HIGH		0.03052 to 62.474		μs
			ECG_CAL_DUTY = 0x1	50		%
ECG CHARACTERISTICS / RIGHT LEG / BODY BIAS DRIVE						
Output-Voltage Range		RLD_GAIN = 24V/V, Shift from Small Signal Gain < 6.5%	0.45	$V_{AVDD} - 0.45$		V
RLD Out-of-Range Comparator Limits		High Limit, RLD_OOR asserted		$0.870 \times V_{AVDD}$		V
		Low Limit, RLD_OOR asserted		$0.127 \times V_{AVDD}$		
Input-Referred Noise of RLD Amplifier		BW = 0.05Hz to 150Hz		8		μV_{P-P}
DC Gain Accuracy		RLD_GAIN = 24V/V	-5	$+5$		%
		External Gain Resistor: RLD_EXT = 3.65M Ω , Nominal R _{INT} = 150k Ω , RLD_EXT_RES = 0x1	-14	± 9	$+14$	
BIOZ CHARACTERISTICS / RECEIVE PATH						
ADC Resolution				20		bits
ENOB		BIOZ_ADC_OSР = 128		16.3		bits
		BIOZ_ADC_OSР = 8		9.6		
ADC Sample Rate		Programmable, see <i>Timing Subsystem</i>		16 to 4546		sps
Phase-Measurement Accuracy at 16Hz		453k Ω in series with 22nF load at 16Hz after calibration (Note 12), $T_A = +25^\circ C$		± 1		deg

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($V_{LDO_IN} = 3.7V$, $V_{LED} = 3.7V$, $V_{AVDD} = 1.8V$, $V_{DVDD} = 1.8V$, $V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, MIN/MAX are from $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Notes 1, 2,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Phase-Measurement Accuracy at 50kHz		Cole Impedance ($800\Omega \parallel (2500\Omega + 1nF)$) load at 50kHz after calibration (Note 12), $T_A = +25^\circ C$. See TOC87 for Histogram Distribution (Note 9)	-0.1		+0.1	deg
Phase-Measurement Accuracy at 500kHz		316Ω in series with 1nF load at 500kHz after calibration (Note 12), $T_A = +25^\circ C$		±1		deg
Phase-Measurement Drift		Drift of impedance phase at 50kHz after calibration (Note 12), drift relative to $T_A = +25^\circ C$ (Note 9)		±0.01		deg/°C
Magnitude-Measurement Accuracy at 16Hz		453kΩ in series with 22nF load at 16Hz after calibration (Note 12), $T_A = +25^\circ C$		±1		%
Magnitude-Measurement Accuracy at 50kHz		Cole Impedance ($800\Omega \parallel (2500\Omega + 1nF)$) load at 50kHz after calibration (Note 12), $T_A = +25^\circ C$. See TOC86 for Histogram Distribution (Note 9)	-0.1		+0.1	%
Magnitude-Measurement Accuracy at 500kHz		316Ω in series with 1nF load at 500kHz after calibration (Note 12), $T_A = +25^\circ C$		±1		%
Magnitude-Measurement Drift		Drift of impedance magnitude at 50kHz after calibration (Note 12), drift relative to $T_A = +25^\circ C$		±0.01		%/°C
Impedance Repeatability		$R_{BODY} = 100k\Omega$, conditions for GSR (Note 13a)		4.4		Ω_{RMS}
		$R_{BODY} = 680\Omega$, conditions for respiration (Note 13b)		8.3		$m\Omega_{RMS}$
		$R_{BODY} = 25\Omega$, conditions for ICG/AED body impedance (Note 13c)		1.0		
DC Power-Supply Rejection	PSRR	$I_{DRV} = 64\mu A_{RMS}$, $F_{BIOZ} = 1kHz$, $BIOZ_GAIN = 10V/V$, $R_{BODY} = 1k\Omega$	$V_{LDO_IN} = 2.3V$ to $5.5V$	5	125	LSB/V
		$BIOZ_DRV_MODE = 0x1$, $BIOZ_VDRV_MAG = 50mV_{PK}$, $F_{BIOZ} = 64Hz$, $BIOZ_GAIN = 10V/V$	$LDO_IN = AGND$, $V_{AVDD} = V_{DVDD} = 1.7V$ to $2.0V$	600	4500	
		$BIOZ_DRV_MODE = 0x1$, $BIOZ_VDRV_MAG = 50mV_{PK}$, $F_{BIOZ} = 64Hz$, $BIOZ_GAIN = 10V/V$	$V_{LDO_IN} = 2.3V$ to $5.5V$	10	80	
		$BIOZ_DRV_MODE = 0x1$, $BIOZ_VDRV_MAG = 50mV_{PK}$, $F_{BIOZ} = 64Hz$, $BIOZ_GAIN = 10V/V$	$LDO_IN = AGND$, $V_{AVDD} = V_{DVDD} = 1.7V$ to $2.0V$	425	3500	
Channel Gain		Selected by $BIOZ_GAIN$		1 to 10		V/V
Channel-Gain Accuracy		$f_{IN}=1kHz$, $BIOZ_GAIN = 10V/V$, $V_{IN} = 100mV_{P-P}$	-5		+5	%
Input-Voltage Range		$f_{IN} = 1kHz$, $V_{IN} = 100mV_{P-P}$, $BIOZ_GAIN = 10V/V$, shift from gain at $0.76V < 2\%$	0.5	$V_{AVDD} - 0.75$		V

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($V_{LDO_IN} = 3.7V$, $V_{LED} = 3.7V$, $V_{AVDD} = 1.8V$, $V_{DVDD} = 1.8V$, $V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, MIN/MAX are from $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Notes 1, 2,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum AC-Differential Input Range		$f_{IN}=1\text{kHz}$, $BIOZ_GAIN = 1\text{V/V}$, shift from small-signal gain at $100\text{mV}_{P-P} < 2\%$		1000		mV_{P-P}
Input-Referred Voltage Noise		$R_{BODY} = 0\Omega$, DRVP and DRVN Disconnected, BW = 0.05Hz to 67Hz (Note 14)		1.6		μVRMS
Input-Referred Current Noise		DRVP and DRVN disconnected, BW = 0.05Hz to 67Hz (Note 14)		300		$\text{fA}/\sqrt{\text{Hz}}$
Input-Referred Offset Voltage		$R_{BODY} = 0\Omega$, $BIOZ_GAIN = 10\text{V/V}$, $BIOZ_AHPF = \text{bypassed}$, $BIOZ_DM_DIS = 1$	-3.0		+3.0	mV
Differential Input Impedance		Lead bias disabled, $BIOZ_AHPF = \text{bypassed}$, impedance at 1kHz		3.0 // 2.4		$\text{G}\Omega // \text{pF}$
Common-Mode Input Impedance		Lead bias disabled, $BIOZ_AHPF = \text{bypassed}$, impedance at 1kHz		2.2 // 1.5		$\text{G}\Omega // \text{pF}$
Input-Analog High-Pass Filter		Programmable from the Register Map		100 to 10,000		Hz
Input-Analog High-Pass Filter Variation		$BIOZ_AHPF = 200\text{Hz}$	-50		+100	%
Input-Analog High-Pass Filter Resistor (Differential)		Differential Filter Resistance	$BIOZ_AHPF = 0x8$	17.0	44.8	84.8
			$BIOZ_AHPF = 0x9$	10.6	23.1	40.3
			$BIOZ_AHPF = 0xA$	4.2	9.3	16.0
			$BIOZ_AHPF = 0xB$	2.3	4.6	7.1
			$BIOZ_AHPF = 0xC$	1.1	2.2	3.6
			$BIOZ_AHPF = 0xD$ or $0xE$	0.46	0.92	1.40
Input-Analog High-Pass Filter Bias Voltage	V_{MID_RX}		700	760	820	mV
Input-Leakage Current		$BIP, BIN = AVDD - 0.2V$ or $AGND + 0.2V$, $T_A = +25^\circ C$	$BIOZ_ELx$, CAL1 and CAL2	-2	0.1	+2
			CAL3 and CAL4 (Note 7)	-2	0.1	+2
BIOZ CHARACTERISTICS / TRANSMIT PATH						
DDS DAC Sine Wave Resolution				10		bits
Current-Drive THD		$I_{DRV} = 64\mu\text{A}_{\text{RMS}}$, $f_{STIM} = 50\text{kHz}$, $R_{BODY} = 1\text{k}\Omega$. Includes odd harmonics h3, h5, and h7.		0.05	0.25	%
Current-Drive Amplitude Resolution		See $BIOZ_VDRV_MAG$ and $BIOZ_IDRV_RGE$		4		bits
Current Drive (Range 1)		$BIOZ_VDRV_MAG = 0x0, 0x1, 0x2, 0x3$	$BIOZ_IDRV_RGE = 0x0$	16, 32, 80, 160		nA_{RMS}
Current Drive (Range 2)		$BIOZ_VDRV_MAG = 0x0, 0x1, 0x2, 0x3$	$BIOZ_IDRV_RGE = 0x1$	0.32, 0.64, 1.6, 3.2		μA_{RMS}

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($V_{LDO_IN} = 3.7V$, $V_{LED} = 3.7V$, $V_{AVDD} = 1.8V$, $V_{DVDD} = 1.8V$, $V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, MIN/MAX are from $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Notes 1, 2,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Drive (Range 3)		BIOZ_VDRV_MAG = 0x0, 0x1, 0x2, 0x3	6.4, 12.8, 32, 64			μA_{RMS}
Drive Current (Range 4)		BIOZ_VDRV_MAG = 0x0, 0x1, 0x2, 0x3	128, 256, 640, 1280			μA_{RMS}
Current-Drive Accuracy		$I_{DRV} \geq 32nA$	-6	+6		%
		$I_{DRV} = 16nA$	-10	+10		
Current-Drive Temperature Coefficient			250			ppm/ $^\circ C$
Short-Circuit Current		BIOZ_DRV_MODE = Voltage Mode, BIOZ_VDRV_MAG = 0x11, BIOZ_AMP_BW = 0x3, BIOZ_AMP_RGE = 0x3, DRVP, DRVN shorted to AGND, AVDD	120	650		μA
		BIOZ_DRV_MODE = H-Bridge Mode, DRVP, DRVN shorted to AGND, AVDD	0.69	1.65		mA
Drive Frequency Range			0.016 to 500			kHz
Current-Drive Compliance Voltage	V_{DRV_P} , V_{DRV_N}	BIOZ_DRV_MODE = 0x0, shift from current at $0.76V < \pm 4\%$	0.4	$V_{AVDD} - 0.4$		V
Current-Drive Out-of-Range Comparator Limits		EN_BIOZ_DRV_OOR = 1	0.27	$V_{AVDD} - 0.52$		V
Drive CM Voltage	V_{MID_TX}	Voltage at DRVSJ in Current Mode	700	760	820	mV

BIOZ CHARACTERISTICS / DIGITAL FILTER

Output-Digital Low-Pass Filter	BIOZ_DLPF = 0x1	0.005 x SR_BIO_Z	Hz
	BIOZ_DLPF = 0x2	0.02 x SR_BIO_Z	
	BIOZ_DLPF = 0x3	0.08 x SR_BIO_Z	
	BIOZ_DLPF $\geq 0x4$	0.25 x SR_BIO_Z	
	BIOZ_DHPF = 0x1	0.00025 x SR_BIO_Z	
	BIOZ_DHPF $\geq 0x2$	0.002 x SR_BIO_Z	

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($V_{LDO_IN} = 3.7V$, $V_{LED} = 3.7V$, $V_{AVDD} = 1.8V$, $V_{DVDD} = 1.8V$, $V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, MIN/MAX are from $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Notes 1, 2,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIOZ CHARACTERISTICS / RESPIRATION						
Current Amplitude		Programmable, see RESP_CGMA G	RESP(CG MAG 4 X = 0	8 to 96		µA
			RESP(CG MAG 4 X = 1	32 to 384		
Current-Amplitude Accuracy		RESP(CG MAG = 0x7	RESP(CG MAG 4 X = 0	-20	+20	%
			RESP(CG MAG 4 X = 1	-25	+25	
Current-Compliance Voltage		RESP(CG MAG 4X = 1, RESP(CG MAG = 384µA, shift from current at 0.76V < 5%	0.7		$V_{AVDD} -$ 0.7	V
Frequency Range		See Timing Subsystem		10 to 131		kHz
Impedance Repeatability		R _{BODY} = 680Ω, conditions for respiration (Note 13d)		6.3		mΩ _{RMS}
BIOZ I/O MUX / DC LEAD-OFF DETECTION						
Full-Scale Current		Selected by BIOZ_LOFF_IMAG	5, 10, 20, 50, 100			nA
Full-Scale Current Accuracy		BIOZ_LOFF_IMAG = 100nA	T _A = 25°C	±5		%
				-30	+30	
Comparator Threshold	V _{BIOZ_TH_H} , V _{BIOZ_TH_L}	Selected by BIOZ_LOFF_THRESH	V _{MID_ECG} G ± 200	V _{MID_ECG} G ± 575		mV
Comparator-Threshold Accuracy		BIOZ_LOFF_THRESH = ±575mV	-12.5	+12.5		%
Full-Scale Electrode Resistance		BIOZ_LOFF_IMAG = 100nA, BIOZ_LOFF_THRESH = ±200mV		4		MΩ
				100		
BIOZ I/O MUX / LEAD BIAS						
Lead-Bias Impedance		BioZ lead-bias enabled to V _{MID_ECG} or V _{RLD} (see the RLD_RBIAS bit)	BIOZ_RBIAS_VAL UE = 0x0	50		MΩ
			BIOZ_RBIAS_VAL UE = 0x1	100		
			BIOZ_RBIAS_VAL UE = 0x2	200		
Lead-Bias Voltage		BioZ lead-bias enabled, RLD_RBIAS = 0	660	760	860	mV
BIOZ I/O MUX / INTERNAL RESISTOR LOADS						
Internal BIA Resistive- Load Nominal Value	R _{VAL}	Selected by BMUX_RSEL	200, 500, 800, 5000			Ω
Internal GSR Resistive- Load Nominal Value	R _{GSR}	Selectable by BMUX_GSR_RSEL	25, 100, 500, 1000			kΩ

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($V_{LDO_IN} = 3.7V$, $V_{LED} = 3.7V$, $V_{AVDD} = 1.8V$, $V_{DVDD} = 1.8V$, $V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, MIN/MAX are from $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Notes 1, 2,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING SUBSYSTEM / PLL						
PLL Frequency Range		FCLK = 32.768kHz, FREQ_LOCK asserted < 3.5ms	4		28	MHz
PLL Lock Time		Change in FCLK to FREQ_LOCK asserted, MDIV = 0x356		1.2	3.5	ms
		Change in FCLK to PHASE_LOCK asserted, MDIV = 0x356		3.5	8.5	
FCLK Input Frequency		Must match CLK_FREQ_SEL		32.0 or 32.768		kHz
Maximum FCLK Rise Time (10% to 90%)	tRISE	$T_A = +25^\circ C$, $V_{IN} = 0V$ to $1.8V$		100		ns
Maximum FCLK Fall Time (90% to 10%)	tFALL	$T_A = +25^\circ C$, $V_{IN} = 1.8V$ to $0V$		100		ns
PLL External-Reference Jitter		Cycle-to-Cycle Period, PLL_LOCK_WNDW = 0		3		nsRMS
FCLK Input Capacitance	C_{FCLK}			15		pF
TIMING SUBSYSTEM / INTERNAL CLOCK						
Internal Oscillator	f_{CLKINT}	REF_CLK_SEL = 32kHz	-2	± 0.4	+2	%
		REF_CLK_SEL = 32.768kHz	-2	± 0.4	+2	
INTERNAL REFERENCE						
ECG Common-Mode Reference Output Voltage	V_{MID_ECG}		740	760	780	mV
ECG Common-Mode Reference Temperature Coefficient	TC_{MID_ECG}			10		ppm/ $^\circ C$
ECG Reference Output Voltage	V_{REF_ECG}		0.990	1.000	1.010	V
ECG Reference Temperature Coefficient	TC_{REF_ECG}			10		ppm/ $^\circ C$
PPG Reference Output Voltage	V_{REF_PPG}		1.15	1.205	1.215	V
PPG Reference Temperature Coefficient	TC_{REF_PPG}			10		ppm/ $^\circ C$
DIGITAL I/O CHARACTERISTICS						
Input-Voltage Low	V_{IL}	CSB/I2C_SEL, SDO/ADDR, SDI/SDA, SCLK/SCL, TRIG, FCLK			$0.2 \times V_{IOVDD}$	V
Input-Voltage High	V_{IH}	CSB/I2C_SEL, SDO/ADDR, SDI/SDA, SCLK/SCL, TRIG, FCLK		$0.8 \times V_{IOVDD}$		V
Input Hysteresis	V_{HYS}	CSB/I2C_SEL, SDO/ADDR, SDI/SDA, SCLK/SCL, TRIG, FCLK		525		mV
Input Capacitance	C_{IN}	CSB/I2C_SEL, SDO/ADDR, SDI/SDA, SCLK/SCL, TRIG, FCLK		10		pF

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Electrical Characteristics (continued)

($V_{LDO_IN} = 3.7V$, $V_{LED} = 3.7V$, $V_{AVDD} = 1.8V$, $V_{DVDD} = 1.8V$, $V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, MIN/MAX are from $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Notes 1, 2,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Leakage Current	I_{IN}	CSB/I ₂ C_SEL, SDO/ADDR, SDI/SDA, SCLK/SCL, TRIG, FCLK, $T_A = +25^\circ C$, $V_{IN} = V_{DGND}$ or V_{DVDD}	-1	+0.01	+1	μA
Output Low Voltage	V_{OL}	SDO, INT1, INT2, $I_{SINK} = 4mA$			0.4	V
Output High Voltage	V_{OH}	SDO, INT1, INT2, $I_{SOURCE} = 4mA$	$V_{IOVDD} - 0.4$			V
Open-Drain Output Low Voltage	V_{OL_OD}	INT1_OCFG = INT2_OCFG = 0, $I_{SINK} = 4mA$			0.4	V
I²C TIMING CHARACTERISTICS (Note 9)						
I ² C Write Address		SDO/ADDR is low		D8		Hex
		SDO/ADDR is high		DA		
I ² C Read Address		SDO/ADDR is low		D9		Hex
		SDO/ADDR is high		DB		
Serial Clock Frequency	f_{SCL}		100		400	kHz
Bus Free-Time Between STOP and START Conditions	t_{BUF}		1.3			μs
Hold-Time START and Repeat START Condition	$t_{HD,STA}$		0.6			μs
SCL Pulse-Width Low	t_{LOW}		1.3			μs
SCL Pulse-Width High	t_{HIGH}		0.6			μs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			μs
Data Hold Time	$t_{HD,DAT}$		0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			μs
Pulse-Width of Suppressed Spike	t_{SP}		0		50	ns
Bus Capacitance	C_B				400	pF
SDA and SCL Receiving Rise Time	t_R		$20 + 0.1C_B$		300	ns
SDA and SCL Receiving Fall Time	t_F		$20 + 0.1C_B$		300	ns
SDA Transmitting Fall Time	t_{TF}		$20 + 0.1C_B$		300	ns
SPI TIMING CHARACTERISTICS (Note 9)						
SCLK Frequency	f_{SCLK}		0.1		24	MHz
SCLK Period	t_{CP}		41.7			ns
SCLK Pulse-Width High	t_{CH}		18			ns
SCLK Pulse-Width Low	t_{CL}		18			ns

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Electrical Characteristics (continued)

($V_{LDO_IN} = 3.7V$, $V_{LED} = 3.7V$, $V_{AVDD} = 1.8V$, $V_{DVDD} = 1.8V$, $V_{IOVDD} = 1.8V$, $T_A = +25^\circ C$, MIN/MAX are from $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Notes 1, 2,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CSB-Fall to SCLK-Rise Setup Time	t_{CSS0}	Applies to the 1 st SCLK rising edge after CSB/I ₂ C_SEL goes low	20			ns
CSB-Fall to SCLK-Rise Hold Time	t_{CSH0}	Applies to the inactive rising edge preceding the 1 st rising edge	10			ns
Last SCLK Rise to CSB Rise	t_{CSH1}	Applies to the last SCLK rising edge in a transaction	20			ns
Last SCLK Rise to Next CSB Fall	t_{CSF}	Applies to the last SCLK rising edge to the next CSB falling edge (new transaction)	60			ns
CSB Pulse-Width High	t_{CSPW}		40			ns
SDI to SCLK-Rise Setup Time	t_{DS}		10			ns
SDI to SCLK-Rise Hold Time	t_{DH}		5			ns
SCLK Fall to SDO Transition	t_{DOT}	$C_{LOAD} = 30\text{pF}$			15	ns
CSB Fall to SDO Fall	t_{DOE}	$C_{LOAD} = 0\text{pF}$	10			ns
CSB Rise to SDO Hi-Z	t_{DOZ}	Disable time			30	ns
TRIG Pulse-Width	t_{TRIG}		1			μs
DIGITAL I/O TIMING CHARACTERISTICS						
TIMING_SYS_RESET Delay on INT2 (Note 9)		Relative to rising edge of FCLK			10	ns
TIMING_SYS_RESET Setup Time on TRIG		Relative to falling edge of FCLK			≥ 10	ns
TIMING_SYS_RESET Hold Time on TRIG		Relative to falling edge of FCLK			≥ 10	ns

Note 1: Limits are 100% tested at $T_A = +25^\circ C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization

Note 2: All register settings use default values, unless otherwise noted below or in specific EC conditions.

$\text{REF_CLK_SEL} = 0$, $\text{CLK_FREQ_SEL} = 1$, $\text{FR_CLK_DIV} = 32$ ($f_{\text{FRAME}} = 1\text{kfps}$),

$\text{CHPF} = 10\mu\text{F}$

Note 3: V_{LED} should be set greater than the minimum output voltage + LED forward voltage.

Note 4: FR = PPG Frame Rate

- a. $\text{MEASx_DRVy_PA} = 0x7F$, $\text{REF_CLK_SEL} = 1$, $\text{PPG1_PWRDN} = 0$, $\text{PPG2_PWRDN} = 1$
- b. $\text{MEASx_DRVy_PA} = 0x7F$, $\text{REF_CLK_SEL} = 1$, $\text{PPG1_PWRDN} = 0$, $\text{PPG2_PWRDN} = 0$

Note 5: PLL Enabled, FCLK = 32768Hz, ECG_INA_GAIN = 20V/V

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Note 6: FCLK = 32768Hz, REF_CLK_SEL = 1, IDR_V = 32µARMS, BIOZ_GAIN = 10V/V, BIOZ_DRV_MODE = Current Drive, BIOZ_INA_MODE = low power mode, DRVP shorted to DRVN (unless otherwise noted).

- a. Digital filters disabled, BIOZ_AMP_RGE = medium-high, BIOZ_AMP_BW = medium-high, BIOZ_INA_MODE = high-power.
- b. BIOZ_DL_{PF} = 0.08 x SR_BIOZ, BIOZ_AHPF = bypass.
- c. BIOZ_DL_{PF} = 0.25 x SR_BIOZ, BIOZ_DHPF = 0.002 x SR_BIOZ, IDR_V = 1.28mA_{RMS}, BIOZ_AMP_RGE = medium-high, BIOZ_AMP_BW = medium-high, BIOZ_INA_MODE = high-power.
- d. Digital filters disabled, BIOZ_AMP_RGE = low, BIOZ_AMP_BW = low.

Register settings for F_BIOZ:

F_BIOZ [Hz]	SR [Hz]	PLL [Hz]	M	BIOZ_KDIV	BIOZ_DAC_OS _R	BIOZ_NDIV	BIOZ_ADC_OS _R
1000	62.5	16,384,000	500	64	256	512	512
50,048	48.875	12,812,288	391	1	256	512	512
100,096	48.875	12,812,288	391	1	128	512	512
100,096	97.75	12,812,289	391	1	128	512	256
249,856	61	15,990,784	488	1	64	512	512
499,712	61	15,990,784	488	1	32	512	512
32,000	62.5	8,192,000	250	1	256	256	512
64	32	4,194,304	128	256	256	256	512

Note 7: M = 125, PLL_CLK = 4.096MHz, BIOZ_KDIV = 1, BIOZ_DAC_OS_R = 128, F_RESP = 32kHz, BIOZ_NDIV = 256, BIOZ_ADC_OS_R = 512, SR_RESP = 31.25sps, ECG_FDIV = 1, ECG_NDIV = 128, ECG_DEC_RATE = 128, SR_ECG = 250sps, INA_MODE = low power, RESP_EN = 1, IDR_V = 32µAPk, CG_MODE = 0x2, CG_LPF_DUTY = 0x3

Note 8: M = 125, PLL_CLK = 4.096MHz, BIOZ_KDIV = 1, BIOZ_DAC_OS_R = 128, F_RESP = 32kHz, BIOZ_NDIV = 256, BIOZ_ADC_OS_R = 512, SR_RESP = 31.25sps, ECG_FDIV = 1, ECG_NDIV = 128, ECG_DEC_RATE = 128, SR_ECG = 250sps, INA_MODE = low power, RESP_EN = 1, IDR_V = 32µAPk, CG_MODE = 0x2, CG_LPF_DUTY = 0x3

FR_PPG = 128fps, PPG1_PWRDN = 0, PPG2_PWRDN = 1, MEASx_TINT = 14.6µs, MEASx_PPG1_ADC_RGE = 32µA, MEASx_PD_SETLNG = 11.8µs, MEASx_LED_SETLNG = 11.7µs, MEAS1_EN = 1, MEAS2_EN = 1, MEASx_DRVA_PA = MEASx_DRVB_PA = 25mA

Note 9: Guaranteed by design and characterization. Not tested in production.

Note 10: Electrode tissue interface impedance mismatch such that one electrode has < 10Ω source impedance and the other has an impedance of 51kΩ || 47nF per IEC60601-2-47.

Note 11: This specification defines the accuracy of the internal calibration voltage source as measured through the ADC channel.

Note 12: Overall accuracy must include calibration resistor accuracy and the overall calibration accuracy. Calibration uses an external 32.768kHz, 2.5nsRMS jitter, ±5ppm TC oscillator with a 680Ω external calibration resistor. The calibration resistor and Cole impedance were measured to within 0.05% magnitude and 0.1° phase accuracy using a calibrated Zurich Instruments MFIA.

Note 13: a. BIOZ_DRV_MODE = 0x0, IDR_V = 160nA_{RMS}, F_BIOZ = 16Hz, SR_BIOZ = 16sps, BIOZ_GAIN = 10V/V, BIOZ_DL_{PF} = 0x4, BIOZ_AHPF = 42.4MΩ with external 47nF BIP and BIN capacitors. Effective signal band = DC to 4Hz.
 b. BIOZ_DRV_MODE = 0x0, IDR_V = 32µA_{RMS}, F_BIOZ = 32kHz, SR_BIOZ = 31.25sps, BIOZ_GAIN = 10V/V, BIOZ_DL_{PF} = 0x3, BIOZ_AHPF = 2kHz. Effective signal band = DC to 2.5Hz.
 c. BIOZ_DRV_MODE = 0x0, IDR_V = 1.28mA_{RMS}, F_BIOZ = 64kHz, SR_BIOZ = 250sps, BIOZ_GAIN = 10V/V, BIOZ_AHPF = 5kHz. Effective signal band = DC to 65Hz.
 d. RESP_EN = 1, RESP(CG_MAG_4x = 0, RESP(CG_MAG = 32µAPk, F_RESP = 32kHz, SR_RESP = 31.25sps, BIOZ_GAIN = 10V/V, BIOZ_DL_{PF} = 0x3, BIOZ_AHPF = 2kHz. Effective signal band = DC to 2.5Hz.

Note 14: BIOZ_GAIN = 10V/V, F_BIOZ = 65.5kHz, SR_BIOZ = 256sps, BioZ Lead Bias = 200MΩ, BIOZ_AHPF = 5kHz

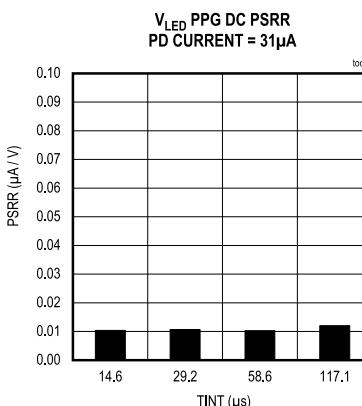
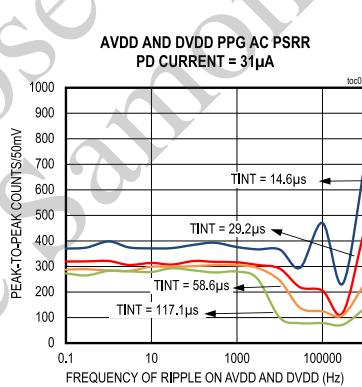
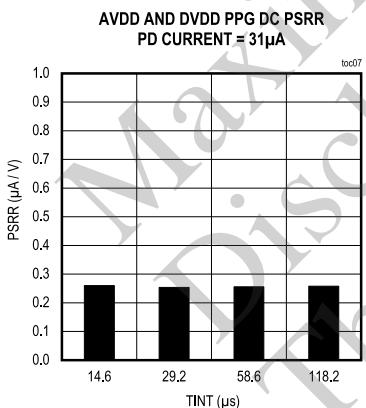
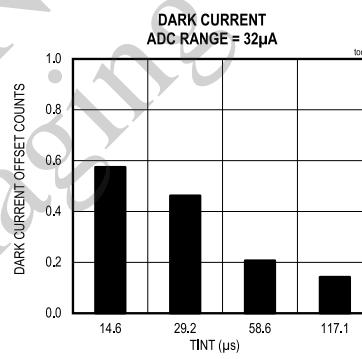
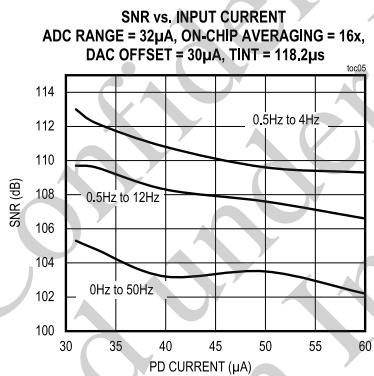
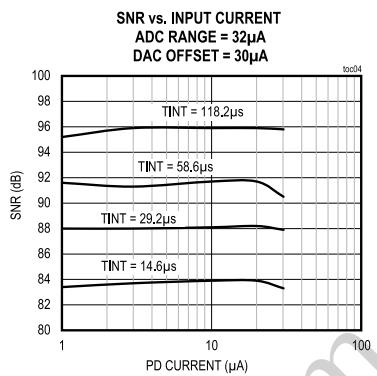
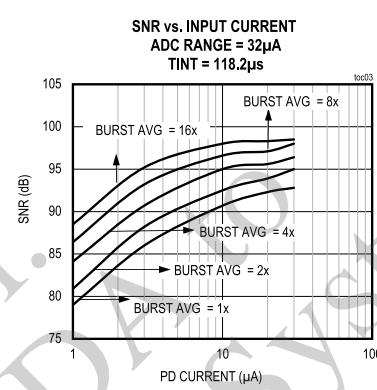
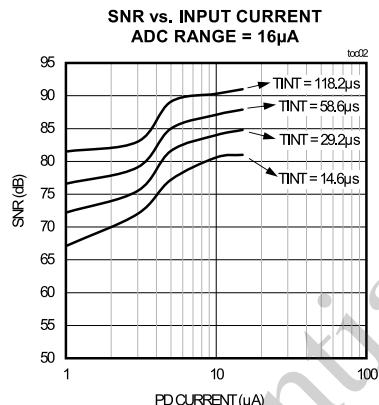
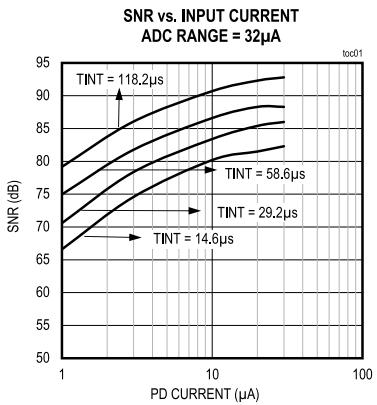
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Ultra-Low-Power, Clinical-Grade
 Vital-Sign AFE

Typical Operating Characteristics

($V_{DD_ANA} = V_{DD_DIG} = 1.8V$, $V_{LED} = 5.0V$, $GND = PGND = 0V$, $T_A = +25^{\circ}C$, unless otherwise noted.)

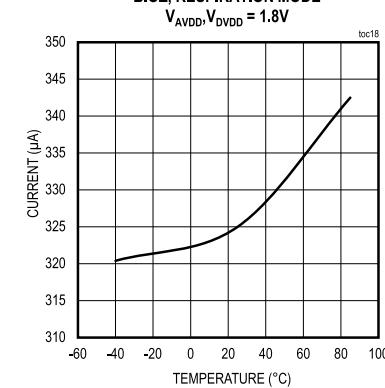
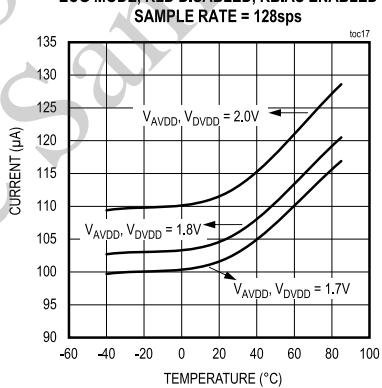
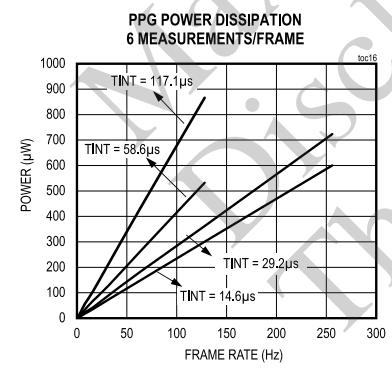
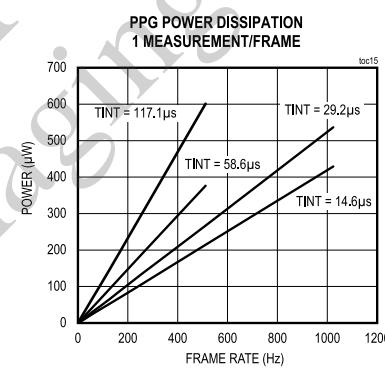
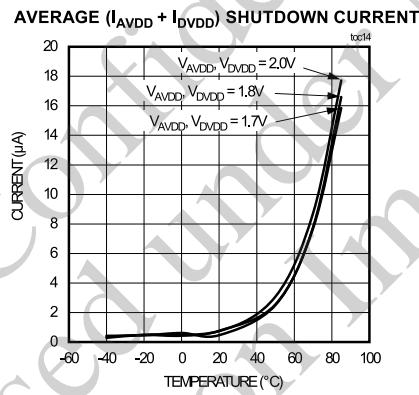
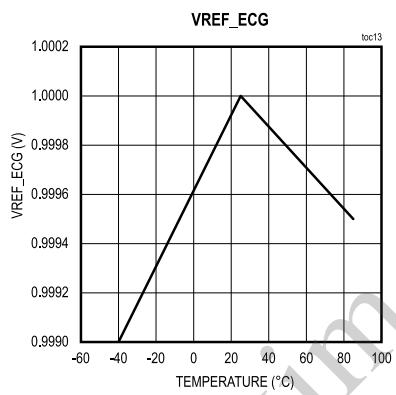
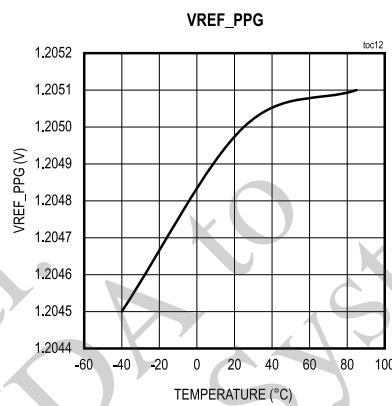
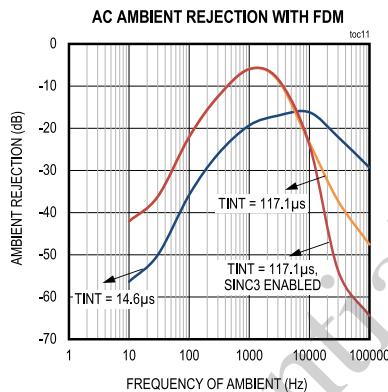
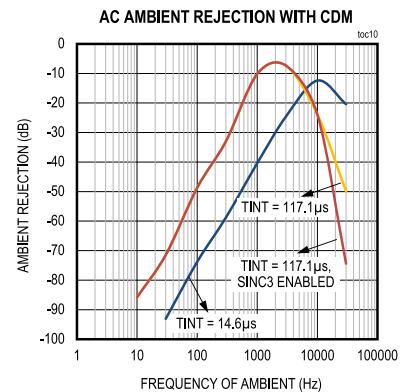


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Typical Operating Characteristics (continued)

($V_{DD_ANA} = V_{DD_DIG} = 1.8V$, $V_{LED} = 5.0V$, $GND = PGND = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)



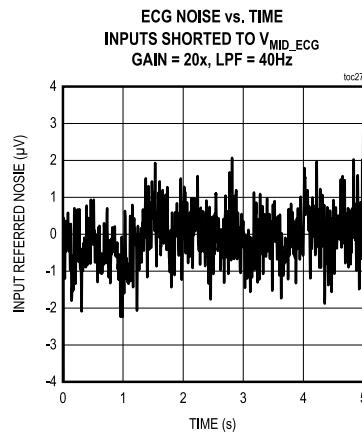
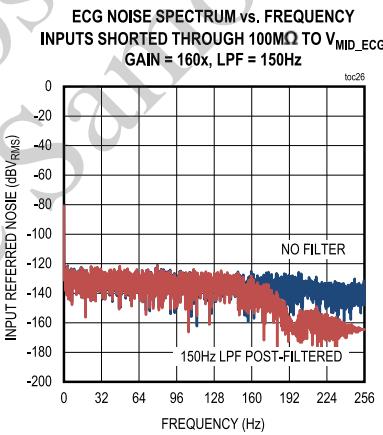
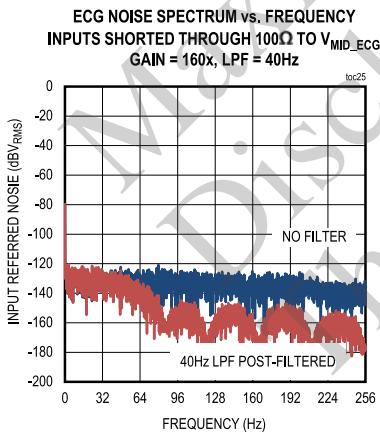
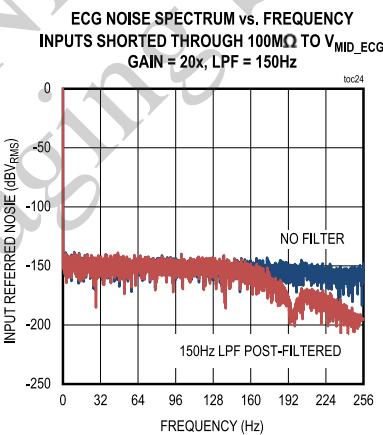
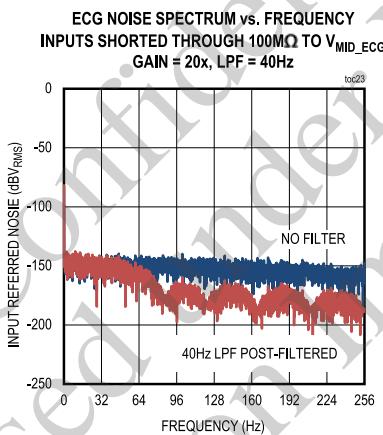
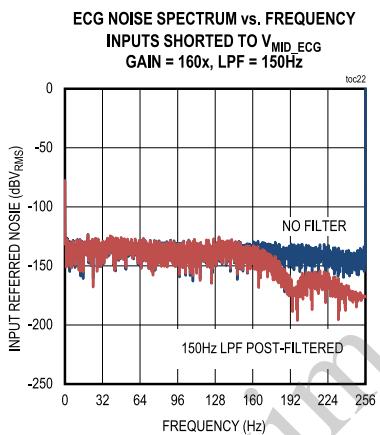
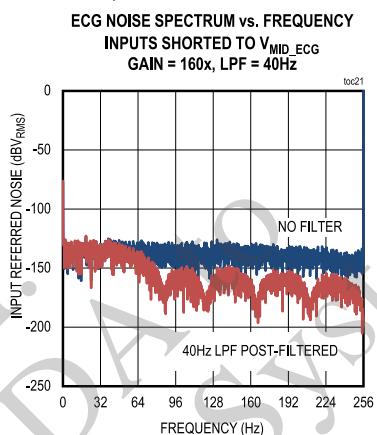
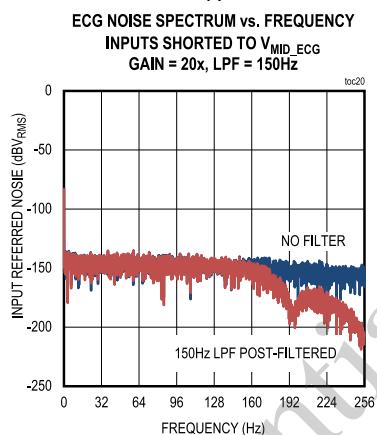
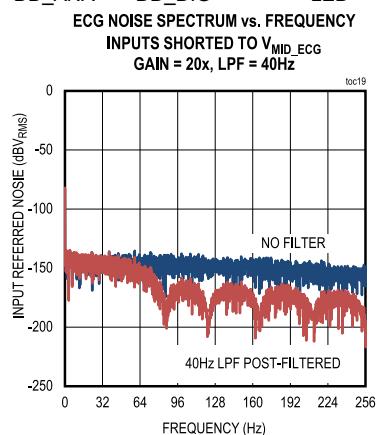
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Typical Operating Characteristics (continued)

($V_{DD_ANA} = V_{DD_DIG} = 1.8V$, $V_{LED} = 5.0V$, $GND = PGND = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)



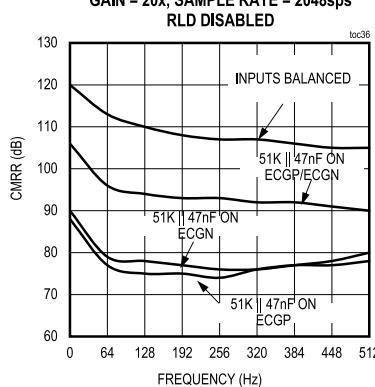
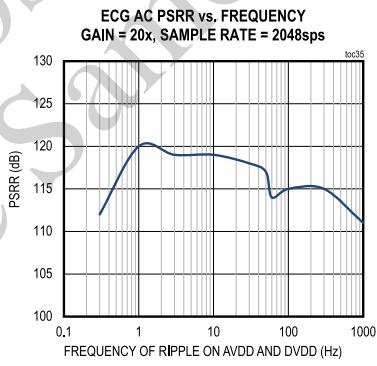
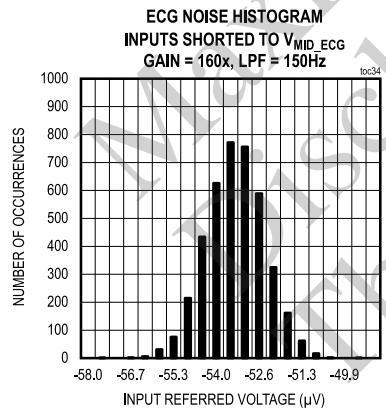
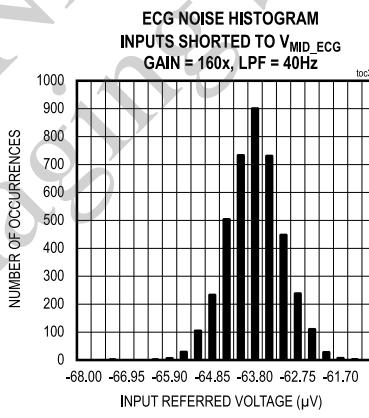
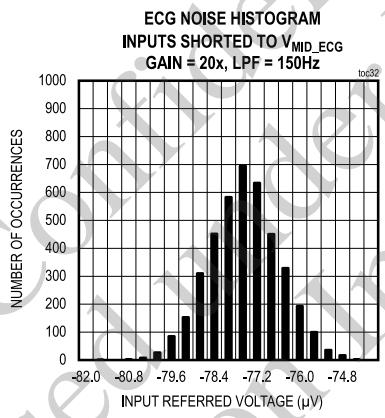
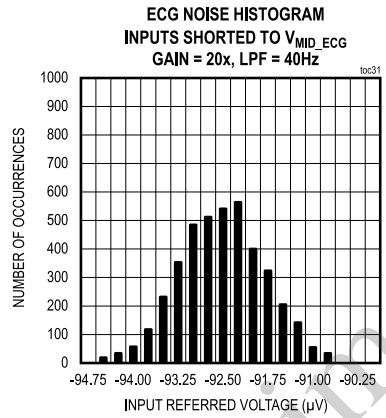
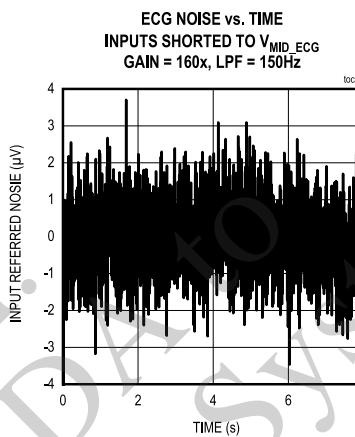
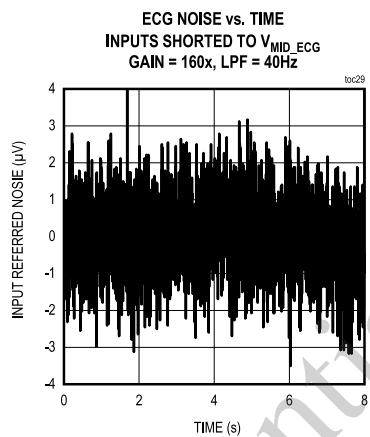
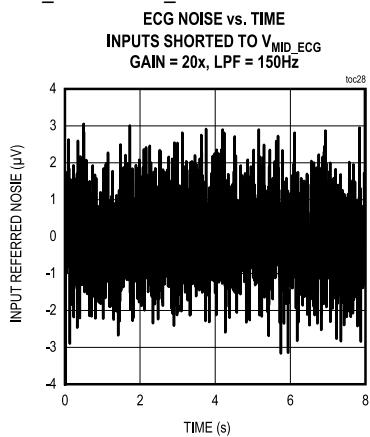
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Typical Operating Characteristics (continued)

($V_{DD_ANA} = V_{DD_DIG} = 1.8V$, $V_{LED} = 5.0V$, $GND = PGND = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)



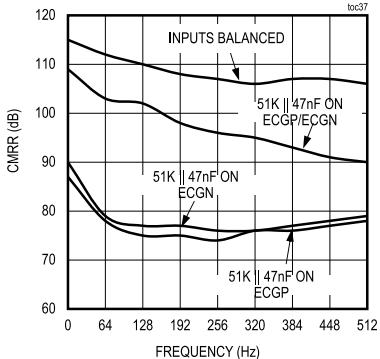
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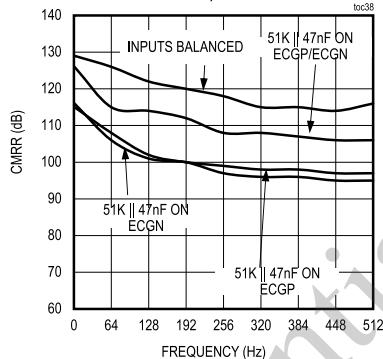
Typical Operating Characteristics (continued)

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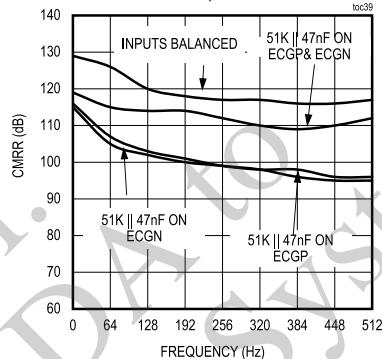
ECG CMRR vs. FREQUENCY
 GAIN = 160x, SAMPLE RATE = 2048sps
 RLD DISABLED



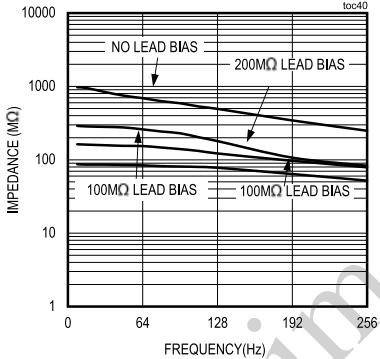
ECG CMRR vs. FREQUENCY
 GAIN = 20x, SAMPLE RATE = 2048sps
 RLD ENABLED, RLD GAIN = 98V/V



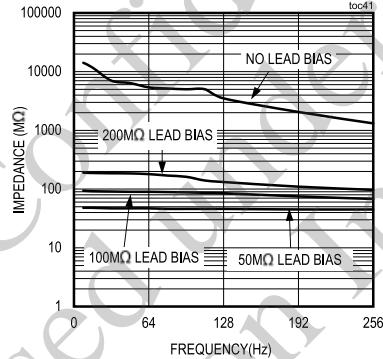
ECG CMRR vs. FREQUENCY
 GAIN = 160x, SAMPLE RATE = 2048sps
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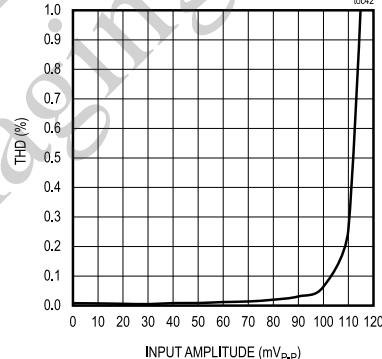
DIFFERENTIAL MODE
 INPUT IMPEDANCE vs. FREQUENCY



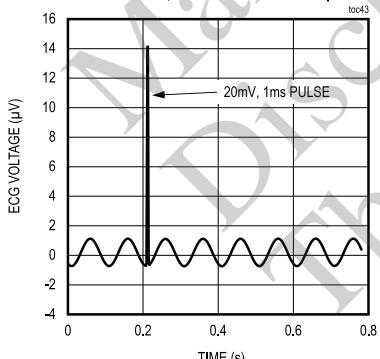
COMMON MODE
 INPUT IMPEDANCE vs. FREQUENCY



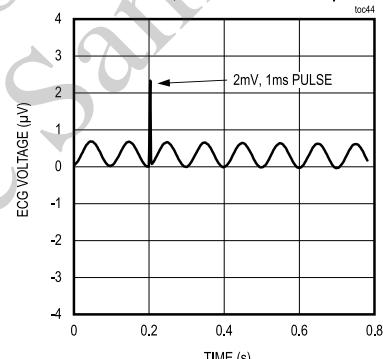
ECG THD vs. INPUT AMPLITUDE
 GAIN = 20x, INPUT FREQUENCY = 8Hz



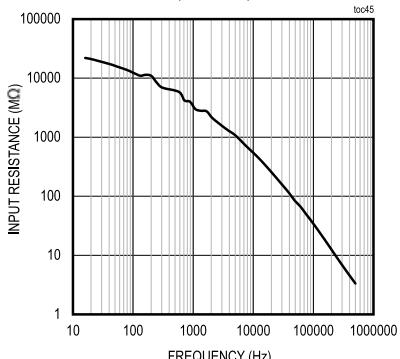
ECG PACEMAKER PULSE TOLERANCE
 GAIN = 20x, SAMPLE RATE = 512sps



ECG PACEMAKER PULSE TOLERANCE
 GAIN = 20x, SAMPLE RATE = 512sps



BIOZ CHANNEL DIFFERENTIAL INPUT RESISTANCE
 16Hz TO 500kHz, GAIN = 1, AHFP BYPASSED

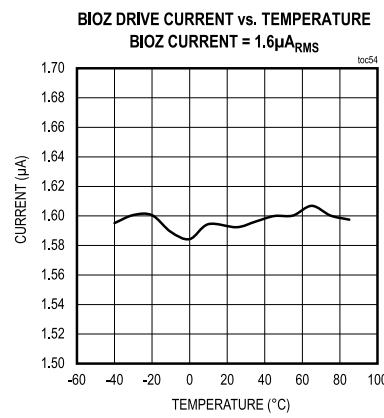
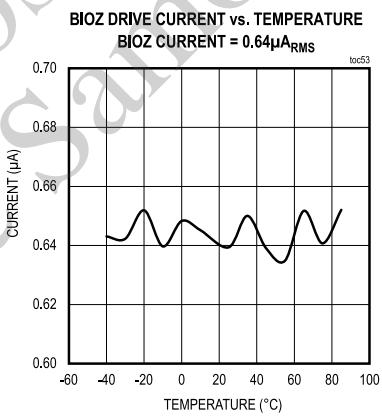
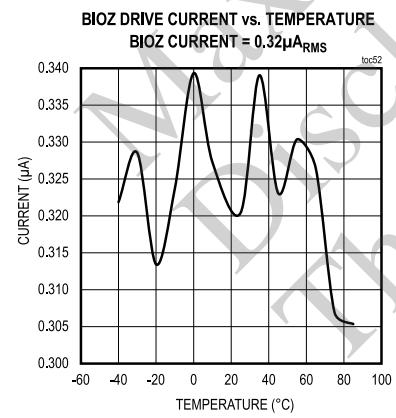
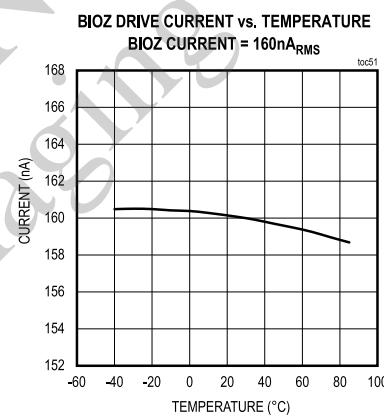
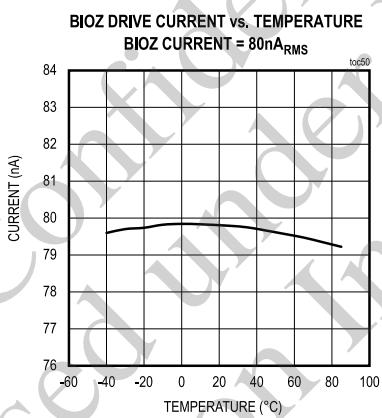
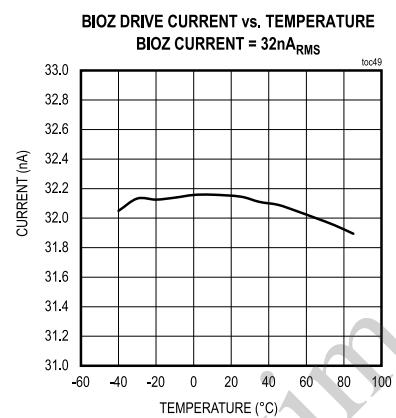
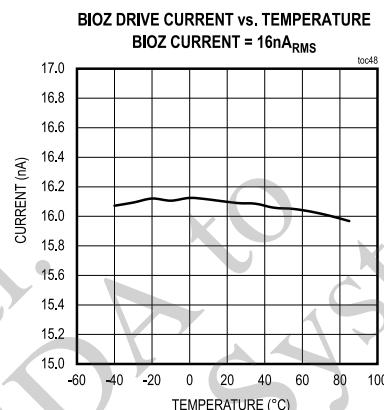
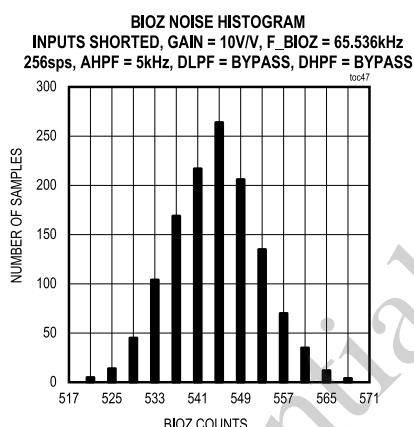
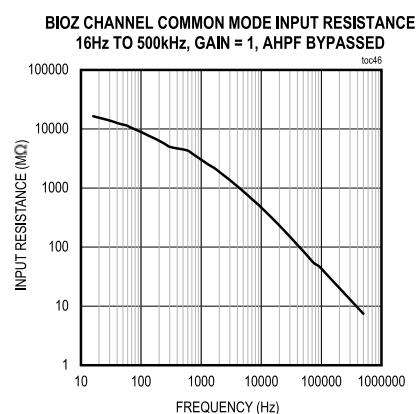


MAX86178

Ultra-Low-Power, Clinical-Grade
 Vital-Sign AFE

Typical Operating Characteristics (continued)

($V_{DD_ANA} = V_{DD_DIG} = 1.8V$, $V_{LED} = 5.0V$, $GND = PGND = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)



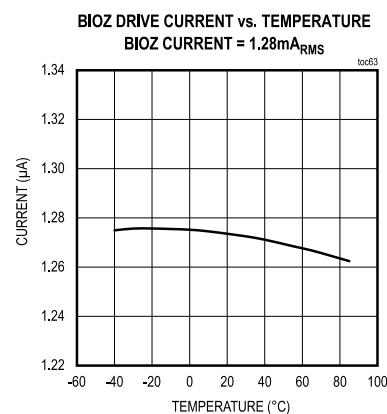
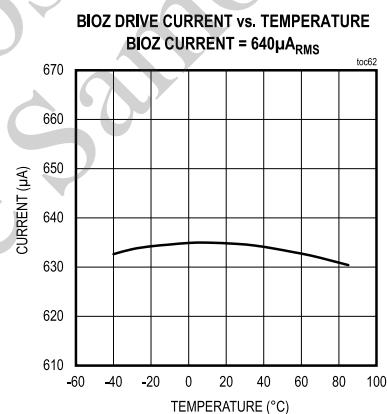
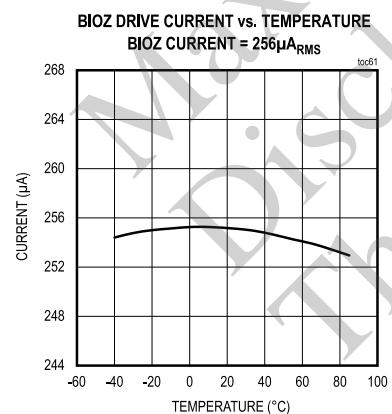
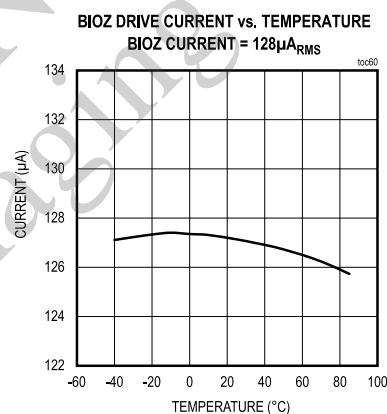
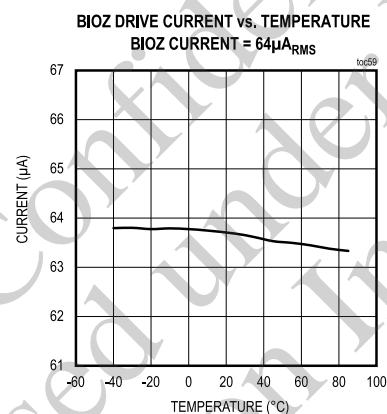
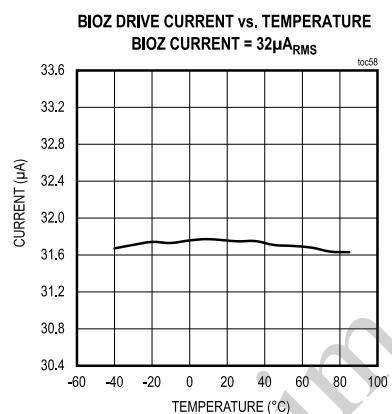
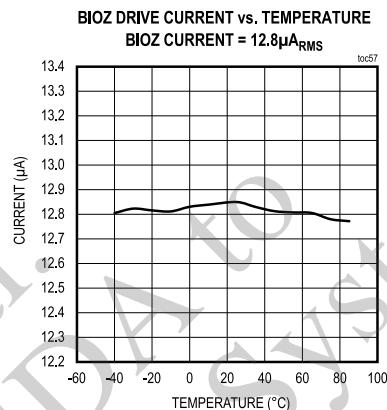
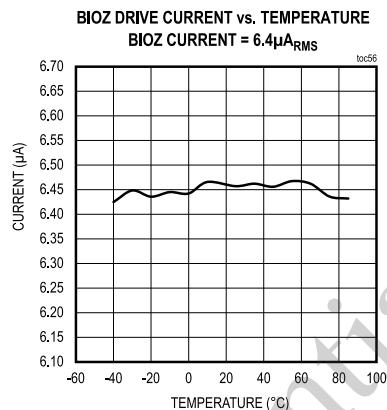
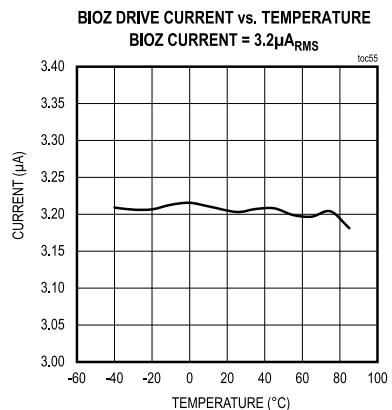
PRELIMINARY

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Ultra-Low-Power, Clinical-Grade
 Vital-Sign AFE

Typical Operating Characteristics (continued)

($V_{DD_ANA} = V_{DD_DIG} = 1.8V$, $V_{LED} = 5.0V$, GND = PGND = 0V, $T_A = +25^\circ C$, unless otherwise noted.)



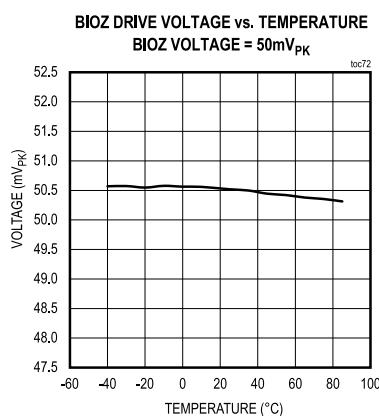
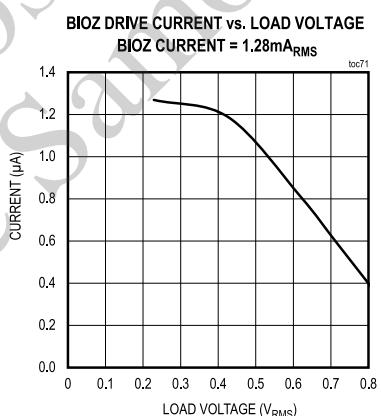
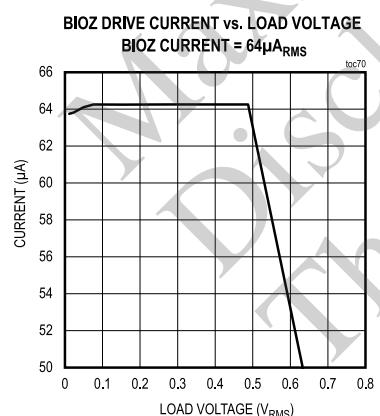
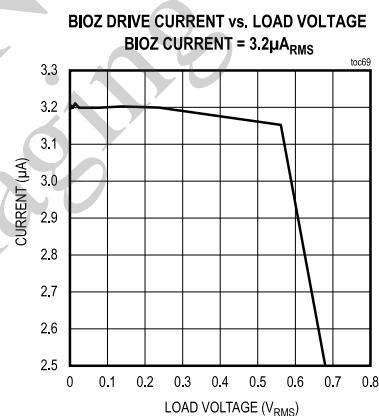
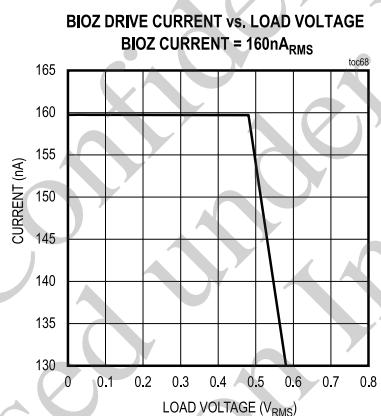
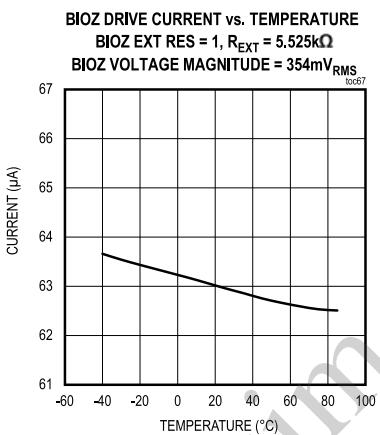
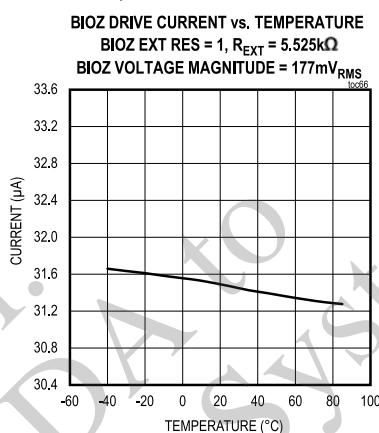
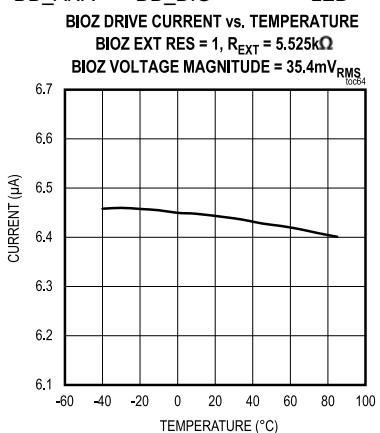
PRELIMINARY

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Ultra-Low-Power, Clinical-Grade Vital-Sign AFE

Typical Operating Characteristics (continued)

($V_{DD_ANA} = V_{DD_DIG} = 1.8\text{V}$, $V_{LED} = 5.0\text{V}$, $GND = PGND = 0\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

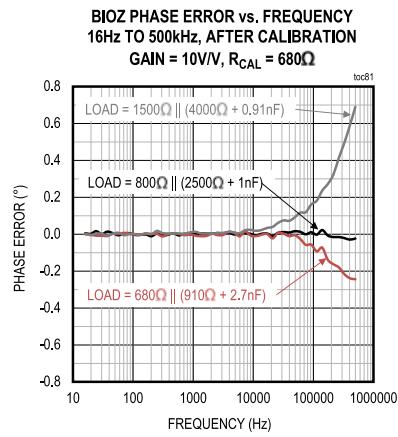
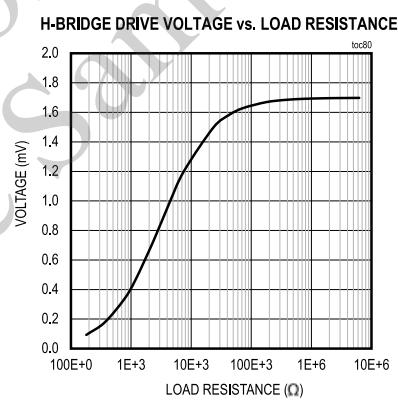
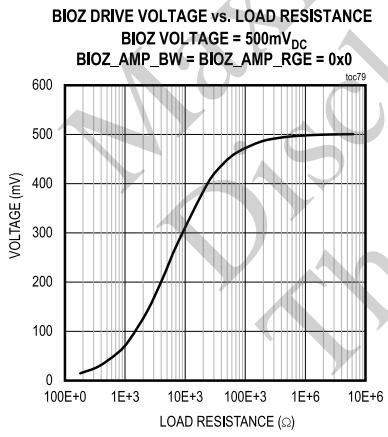
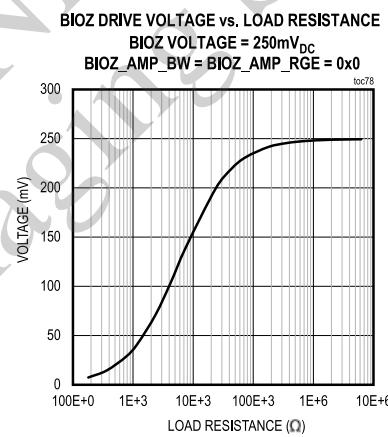
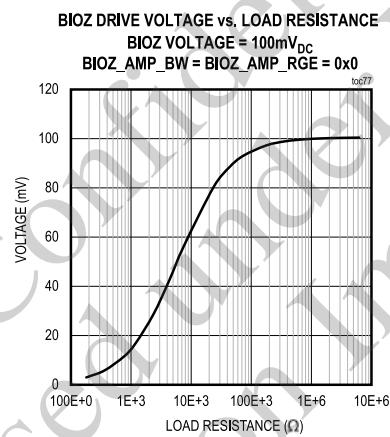
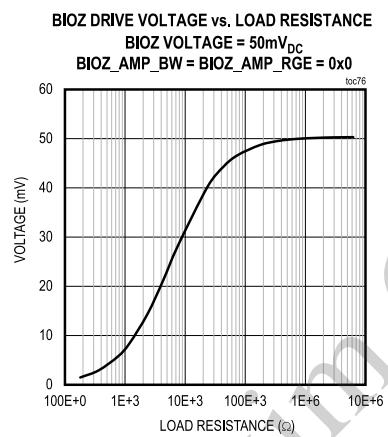
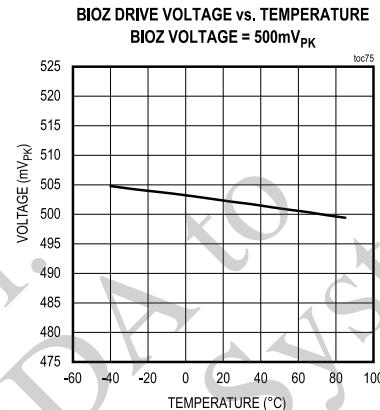
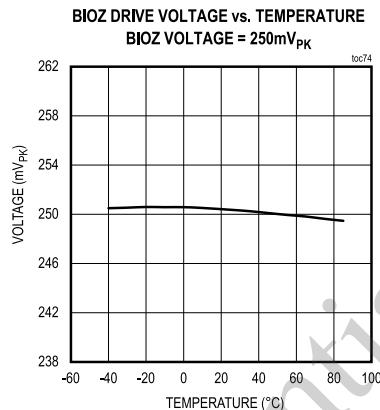
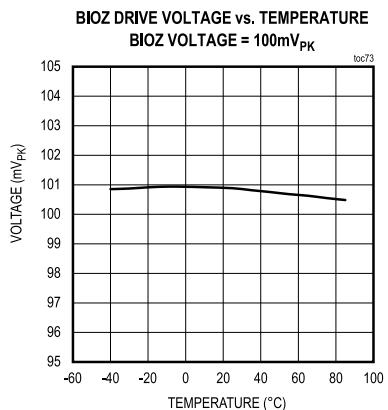


MAX86178

Ultra-Low-Power, Clinical-Grade
 Vital-Sign AFE

Typical Operating Characteristics (continued)

($V_{DD_ANA} = V_{DD_DIG} = 1.8V$, $V_{LED} = 5.0V$, $GND = PGND = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)



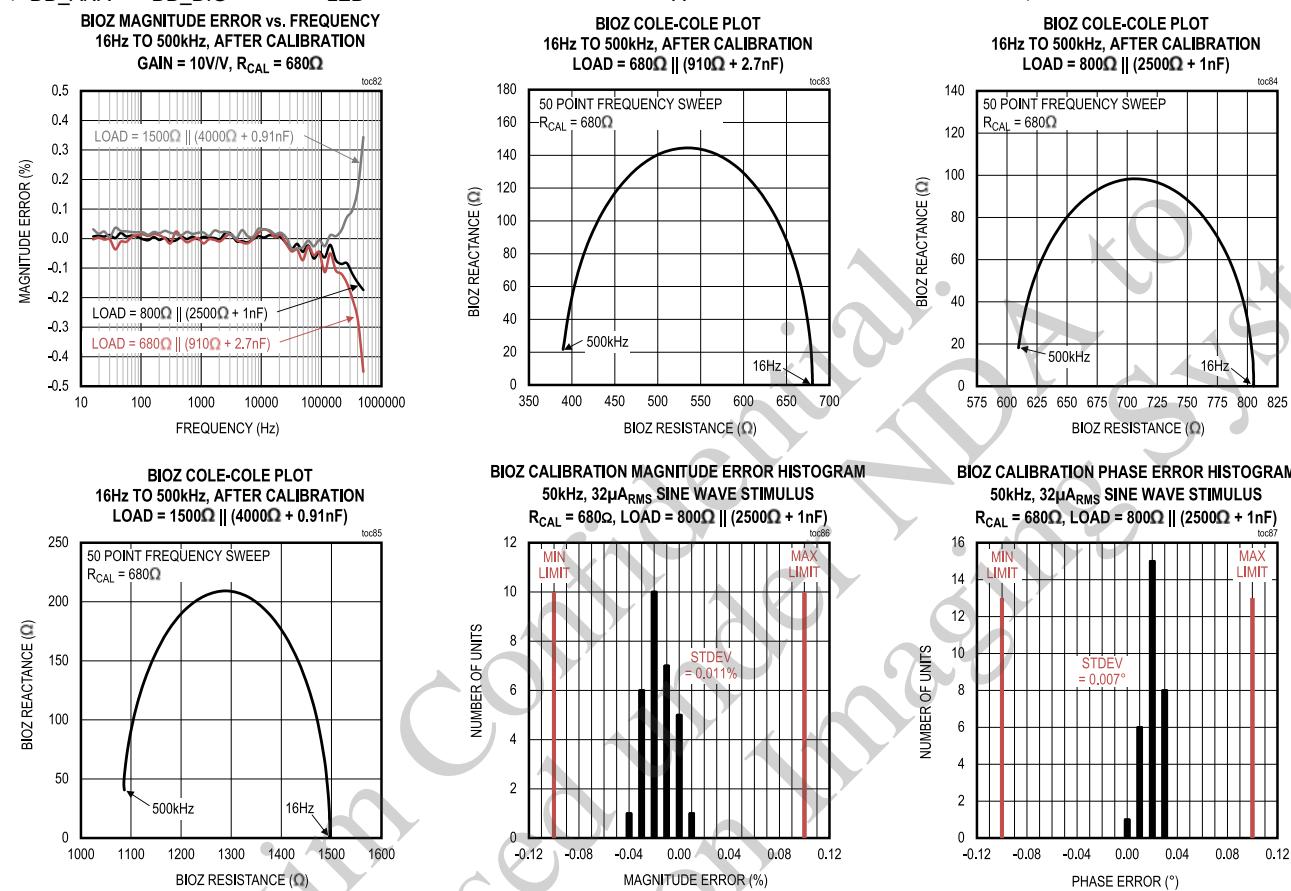
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Ultra-Low-Power, Clinical-Grade
 Vital-Sign AFE

Typical Operating Characteristics (continued)

($V_{DD_ANA} = V_{DD_DIG} = 1.8V$, $V_{LED} = 5.0V$, GND = PGND = 0V, $T_A = +25^\circ C$, unless otherwise noted.)



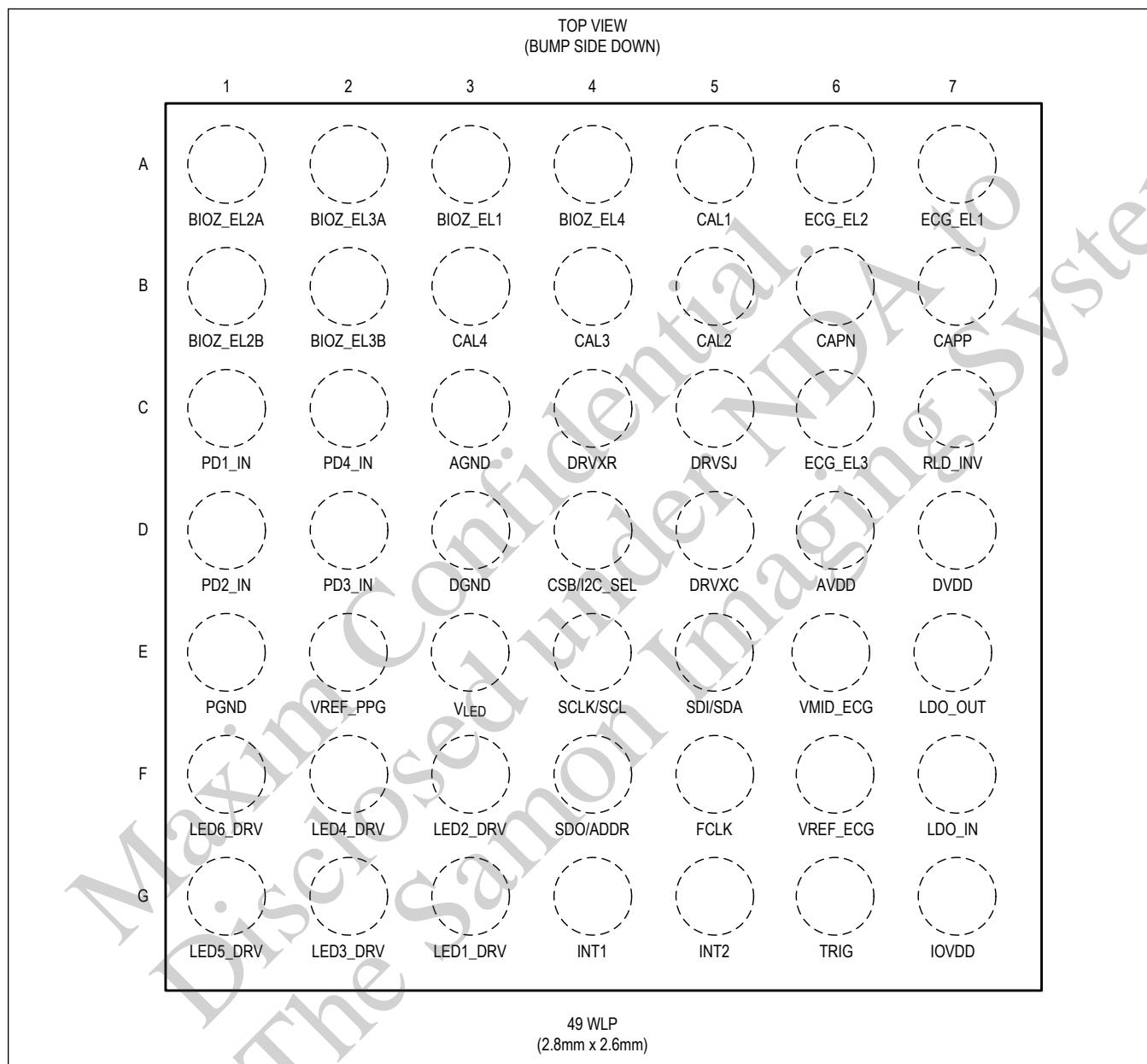
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MAX86178

Ultra-Low-Power, Clinical-Grade
 Vital-Sign AFE

Pin Configuration

MAX86178 WLP



Pin Description

PIN	NAME	FUNCTION
POWER		
D6	AVDD	Analog Core Supply Voltage. Bypass to AGND with a 0.1µF and a 10µF X5R 0603 capacitor or equivalent effective capacitance. Connect to an externally regulated supply or LDO_OUT if LDO_IN ≥ 2.3V

MAX86178**Ultra-Low-Power, Clinical-Grade
Vital-Sign AFE****Pin Description (continued)**

PIN	NAME	FUNCTION
D7	DVDD	Digital Core Supply Voltage. Bypass to DGND with a 0.1µF and a 10µF X5R 0603 capacitor or equivalent effective capacitance. Connect to an externally regulated supply or LDO_OUT if LDO_IN ≥ 2.3V.
C3	AGND	Analog Power and Reference Ground. Connect to the PCB ground plane.
D3	DGND	Digital Ground for both Digital Core and I/O Pad Drivers. Recommended to connect to the AGND plane.
E1	PGND	LED Power Return. Connect to PCB ground.
E3	V _{LED}	V _{LED} Power Supply Input. In a configuration with more than one LED supply, connect V _{LED} to the highest LED supply voltage. Bypass with a 10µF X5R 16V 0603 capacitor or minimum equivalent effective capacitance to PGND.
F7	LDO_IN	LDO Input. Connect to ground when not in use.
E7	LDO_OUT	LDO Output. Connect to AVDD, DVDD, and IOVDD only. Bypass to AGND. Not for external use.
G7	IOVDD	Digital Input Output Supply Voltage. Bypass to DGND
PPG		
C1	PD1_IN	Photodiode 1 Cathode Input. This is connected to either PPG1 or PPG2 depending on the MEASx_PD1_SEL (x = 1 to 6) setting.
D1	PD2_IN	Photodiode 2 Cathode Input. This is connected to either PPG1 or PPG2 depending on the MEASx_PD2_SEL (x = 1 to 6) setting.
D2	PD3_IN	Photodiode 3 Cathode Input. This is connected to either PPG1 or PPG2 depending on the MEASx_PD3_SEL (x = 1 to 6) setting.
C2	PD4_IN	Photodiode 4 Cathode Input. This is connected to either PPG1 or PPG2 depending on the MEASx_PD4_SEL (x = 1 to 6) setting.
G3	LED1_DRV	LED Output 1. Driven when MEASx_DRV _y = 0 (x = 1 to 6, y = A, B). Connect the LED cathode to LED1_DRV and its anode to the V _{LED} supply.
F3	LED2_DRV	LED Output 2. Driven when MEASx_DRV _y = 1 (x = 1 to 6, y = A, B). Connect the LED cathode to LED2_DRV and its anode to the V _{LED} supply.
G2	LED3_DRV	LED Output 3. Driven when MEASx_DRV _y = 2 (x = 1 to 6, y = A, B). Connect the LED cathode to LED3_DRV and its anode to the V _{LED} supply.
F2	LED4_DRV	LED Output 4. Driven when MEASx_DRV _y = 3 (x = 1 to 6, y = A, B). Connect the LED cathode to LED4_DRV and its anode to the V _{LED} supply.
G1	LED5_DRV	LED Output 5. Driven when MEASx_DRV _y = 4(x = 1 to 6, y = A, B). Connect the LED cathode to LED5_DRV and its anode to the V _{LED} supply.
F1	LED6_DRV	LED Output 6. Driven when MEASx_DRV _y = 5 (x = 1 to 6, y = A, B). Connect the LED cathode to LED6_DRV and its anode to the V _{LED} supply.
ECG		
A7	ECG_EL1	ECG Electrode 1 Connection. Configured as an ECG positive input, ECG negative input, or ECG right leg drive output based on the ECG_MUX_SEL[1:0](0x82) register setting.
A6	ECG_EL2	ECG Electrode 2 Connection. Configured as an ECG positive input, ECG negative input, or ECG right leg drive output based on the ECG_MUX_SEL[1:0](0x82) register setting.
C6	ECG_EL3	ECG Electrode 3 Connection. Configured as an ECG positive input, ECG negative input, or ECG right leg drive output based on the ECG_MUX_SEL[1:0](0x82) register setting.
B7	CAPP	Analog High-Pass Filter Input. Connect a 1µF X7R capacitor (C _{HPF}) between CAPP and CAPN to form a 0.5Hz high-pass response in the ECG channel. For more options of CHPF and corner frequencies, see Table 12 .

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Ultra-Low-Power, Clinical-Grade
Vital-Sign AFE**Pin Description (continued)**

PIN	NAME	FUNCTION
B6	CAPN	Analog High-Pass Filter Input. Connect a $1\mu\text{F}$ X7R capacitor (C_{HPF}) between CAPP and CAPN to form a 0.5Hz high-pass response in the ECG channel. For more options of C_{HPF} and corner frequencies, see Table 12 .
C7	RLD_INV	Inverting Input of RLD Amplifier. Connect a gain-setting resistor between RLD_INV and the ECG_ELx pin assigned to RLD, or leave disconnected to use internal gain settings.
BIOZ		
BIOZ / ELECTRODE CONNECTIONS		
A1	BIOZ_EL2A	BIOZ Electrode 2A Connection. BIOZ_EL2A or BIOZ_EL2B are normally connected to the BIOZ receive channel BIP input, but can be switched to connect to the DRVP current generator output under program control. Two BIOZ_EL2 inputs are provided so that one can use the device for both GSR/EDA applications that require an external AC-coupling capacitor and BIA/BIS applications that use the internal AHPF, and thus, do not require the use of an external AC-coupling capacitor.
B1	BIOZ_EL2B	BIOZ Electrode 2B Connection. See the description for BIOZ_EL2A.
A2	BIOZ_EL3A	BIOZ Electrode 3A Connection. BIOZ_EL3A or BIOZ_EL3B are normally connected to the receive channel BIN input, but can be switched to connect to the DRVN current generator output under program control. Two BIOZ_EL3 inputs are provided so that one can use the device for both GSR/EDA applications that require an external AC-coupling capacitor and BIA/BIS applications that use the internal AHPF and thus do not require the use of an external AC-coupling capacitor.
B2	BIOZ_EL3B	BIOZ Electrode 3B Connection. See the description for BIOZ_EL3A.
A3	BIOZ_EL1	BIOZ Electrode 1 Connection. BIOZ_EL1 is normally connected to the DRVP current generator output, but can be switched to the receive channel BIP input under program control.
A4	BIOZ_EL4	BIOZ Electrode 4 Connection. BIOZ_EL4 is normally connected to the DRVN current generator output, but can be switched to the receive channel BIN input under program control.
BIOZ / CALIBRATION SUPPORT		
A5	CAL1	Calibration Port 1. Connects the internal DRVP node to an external reference resistor when calibration is enabled.
B5	CAL2	Calibration Port 2. Connects the internal BIP node to an external reference resistor when calibration is enabled.
B4	CAL3	Calibration Port 3. Connects the internal BIN node to an external reference resistor when calibration is enabled.
B3	CAL4	Calibration Port 4. Connects the internal DRVN node to an external reference resistor when calibration is enabled.
BIOZ / REFERENCE		
C5	DRV SJ	Drive Amplifier Summing Junction. Virtual ground in sine-wave current mode.
C4	DRV XR	Drive Amplifier External Resistor. Connect a precision resistor between DRVXR and DRVXC if setting the BioZ drive current externally. Leave unconnected if using internal current settings.
D5	DRV XC	Drive Amplifier External Capacitor. Connect a 47nF capacitor between DRVXC and DRVSJ to AC couple the VDRV and IDR amplifiers in sine-wave current drive applications. Otherwise, short DRVXC to DRVSJ.
REFERENCE		
E6	VMID_ECG	ECG Common Mode Reference Output. Bypass to AGND with a $10\mu\text{F}$ X5R ceramic capacitor.
E2	VREF_PPG	PPG ADC Reference Buffer Output. Bypass to AGND with a $1\mu\text{F}$ X5R ceramic capacitor.
F6	VREF_ECG	ECG ADC Reference Buffer Output. Bypass to AGND with a $10\mu\text{F}$ X5R ceramic capacitor.
CONTROL INTERFACE		
E4	SCLK/SCL	SPI Clock in SPI Mode or I ² C Clock in I ² C Mode
E5	SDI/SDA	SPI Data Input in SPI Mode or I ² C Data Input and Output in I ² C Mode

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Pin Description (continued)

PIN	NAME	FUNCTION
F4	SDO/ADDR	SPI Data Output in SPI Mode or I ² C Address Select in I ² C Mode. Do not leave unconnected.
D4	CSB/ I ² C_SEL	Active-Low Chip Select Input in SPI Mode. Pull high or connect to IOVDD to select I ² C Mode. Do not leave unconnected.
G4	INT1	Interrupt 1 Output. INT1 is a programmable active-high or active-low status output. It can be used to interrupt an external device. When not used, it can be left unconnected.
G5	INT2	Interrupt 2 Output. INT2 is a programmable active-high or active-low status output. It can be used to interrupt an external device. When not used, it can be left unconnected.
G6	TRIG	Configurable Synchronization Trigger Input/Output. PPG frame trigger input, PLL sync input/output, ECG sync output, or LED pulse sync output. When not used, connect to DGND.
F5	FCLK	External Clock Input. Connect to a 32.0kHz or 32.768kHz external clock source (optional). When not used, it can be left unconnected.

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MAX86178**Ultra-Low-Power, Clinical-Grade
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The MAX86178 is a complete, integrated data acquisition systems, ideal for various applications including optical pulse oximetry, heart-rate detection, ECG, respiration, bioimpedance analysis/bioimpedance spectroscopy (BIA/BIS), and numerous other applications. It is designed for the demanding requirements of medical, mobile and wearable devices and requires minimal external hardware components for integration.

The PPG data acquisition system in the MAX86178 supports up to 6 LEDs and 4 photodiode inputs and includes two high-resolution optical-readout signal processing channels with robust ambient light cancellation and high-current LED-driver DACs to form a complete dual-optical readout signal chain.

The ECG channel in the MAX86178 has high input impedance, low noise, high CMRR, programmable gain, right-leg drive, lead-on and lead-off detection, and a high-resolution analog-to-digital converter.

The BioZ transmit channel has an independent current stimulus circuit for providing injected body currents. The stimulus current generation circuit can be supplied in a four-electrode (tetrapolar) manner as well as a two-electrode (bipolar) manner. This injected current is programmable and available over a wide frequency range (16Hz to 806kHz) and a wide range of stimulus current magnitudes (16nA_{RMS}, up to 1.28mA_{RMS} max). These ranges support GSR (galvanic-skin response) and electrodermal activity (EDA) measurements, BIA/BIS applications, and impedance cardiography (ICG) measurements such as cardiac output and stroke volume, or for impedance plethysmography (IPG) measurements. The transmit channel also includes an independent high-impedance, low-noise current-source driver for measuring respiration simultaneously with ECG.

The BioZ receive channel also has high input impedance, low noise, high CMRR, programmable gain, various low-pass and high-pass filter options, a high resolution analog to digital converters, and I and Q measurement capability to provide resistance and reactance measurements for BIA/BIS applications.

The BioZ channel also includes DC lead-off detection, DRVN lead-off detection, ultra-low-power lead-on detection during standby mode, and extensive calibration features and programmable resistive loads for built-in self-test. Soft power-up sequencing ensures that no large transients are injected into the electrodes.

The MAX86178 provides a calibration port for a four-wire external precision reference resistance to use during calibration. This calibration is required when using the MAX86178 for bioimpedance measurements needing absolute accuracy such as BIA/BIS or AED body-impedance. The four-wire calibration port can also be used to support multiple calibration resistances. Alternatively, there are trimmed load resistors internal to the device that can be used for calibration, but they are not as accurate as using an external reference resistor.

The MAX86178 is fully adjustable through software registers and the digital output data is stored in a 256-word FIFO. The FIFO allows the MAX86178 to be connected to a microcontroller or processor on a shared I²C or SPI bus. Both operate in fully autonomous mode for low-power battery applications.

The MAX86178 operates on a 1.8V main supply voltage or directly from a battery when using the internal LDO regulator, plus an additional 2.7V to 5.5V LED driver power supply. Both have flexible timing and shutdown configurations as well as control of individual blocks so that an optimized measurement can be made with minimum power consumption and a high level of accuracy.

Timing Subsystem

The MAX86178 timing subsystem is shown in [Figure 1](#).

[Figure 1](#) shows all the registers bits and formulas needed for setting the PPG frame rate, ECG and BioZ sample rates, as well as the stimulus frequencies for BioZ, respiration and ECG AC lead-off detect.

The sample rates for the three data paths, PPG, ECG and BIOZ are all referenced to a common clock called REF_CLK, which is sourced either from an external oscillator on the FCLK or from the internal slow oscillator clock INT_FCLK depending on the REF_CLK_SEL[6](0x1D) setting. A separate 10MHz oscillator provides PPG_ADC_CLK, which is the clock for the PPG ADC.

The MAX86178 timing system offers a great deal of flexibility. However, certain considerations must be taken into account when configuring the timing system. The following sections describe these considerations in detail.

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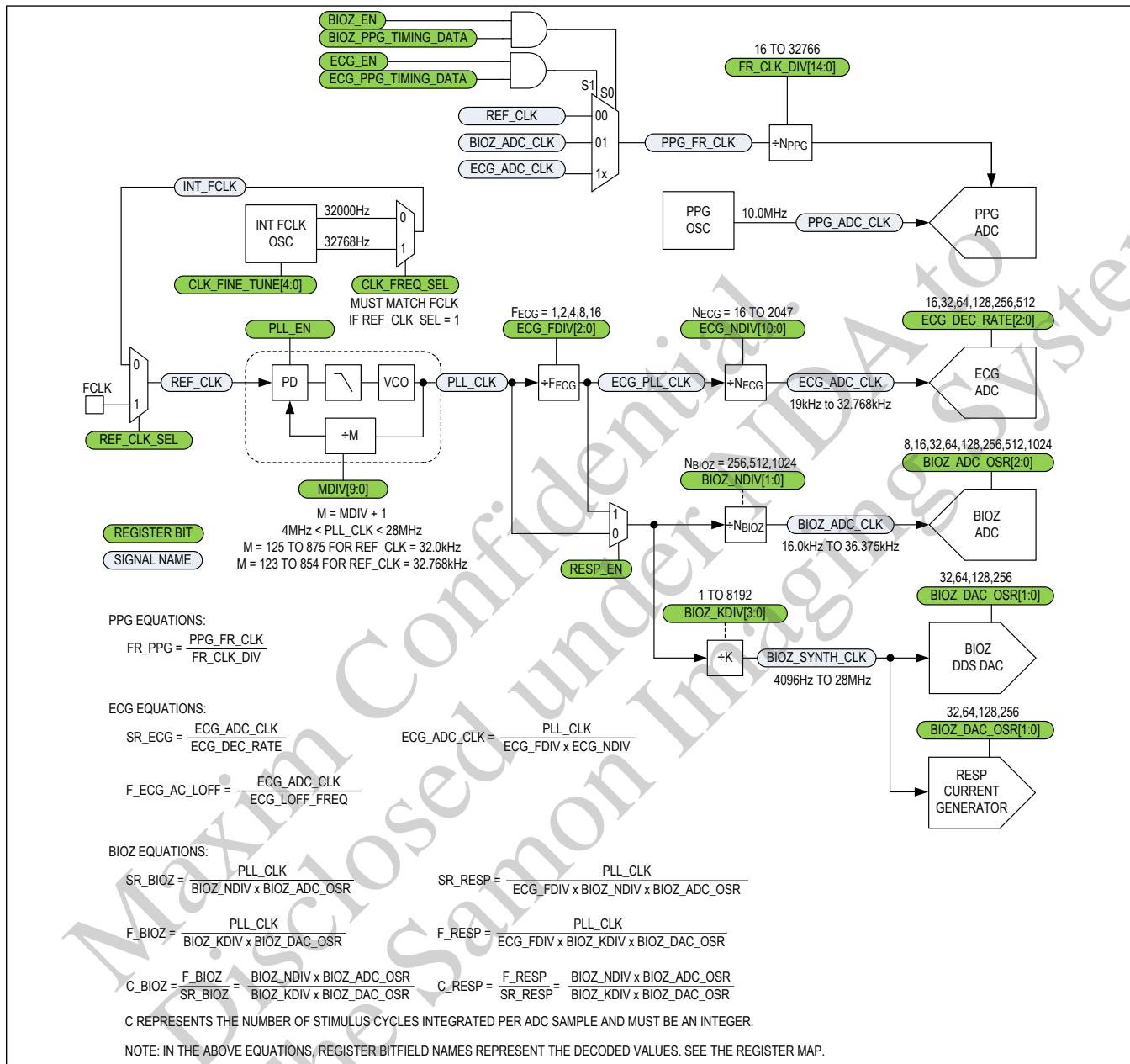


Figure 1. Timing Subsystem

Clock Sources

The MAX86178 timing system incorporates two internal slow oscillators, 32.0kHz and 32.768kHz, and the user can select the oscillator with the desired frequency by setting CLK_FREQ_SEL[5](0x1D). If REF_CLK_SEL[6](0x1D) = 0, the internal slow oscillator selected by CLK_FREQ_SEL provides the reference clock to the PLL circuit used as the time base for the ECG and BioZ channels and generates the clock for the PPG frame rate (PPG_FR_CLK). If REF_CLK_SEL = 1, the oscillator on the FCLK (either 32.0kHz or 32.768kHz) becomes the source of REF_CLK. Even when using the external oscillator on FCLK, the CLK_FREQ_SEL must be set according to the frequency of the external clock source.

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It is recommended to use a low-jitter external oscillator with < 347ppm of frequency accuracy to meet IEC60601-2-47 timing accuracy compliance. The FCLK source must be an active-drive clock, not only a crystal.

The two internal slow oscillators, 32.0kHz and 32.768kHz in MAX86178 are factory trimmed and exhibit a drift with temperature (primary cause of drift) of less than $\pm 1\%$ over the temperature range of 0°C to +50°C. If this level of stability is inadequate, then the MAX86178 offers a fine adjust register CLK_FINE_TUNE[4:0](0x1D), which can be used in combination with a highly stable crystal based real-time clock (RTC) oscillator in the host microcontroller to trim out the drift of the on-chip slow oscillator. By counting the time between the MAX86178 generated interrupts using the microcontroller based RTC, it is possible to compute the error in the slow oscillator frequency and trim it to within $\pm 0.0625\%$ (typ) of the microcontroller based RTC. Using this approach, it is possible to achieve accuracy near that of a crystal oscillator since the phase noise of the MAX86178 slow oscillator is low and the drift is primarily due to temperature.

The MAX86178 also has a 10MHz on-chip fast oscillator, which is the clock source for PPG ADC and is factory trimmed to better than 1% accuracy at room temperature and 2% accuracy over the entire operating temperature range.

PLL and PLL Synchronization

The MAX86178 timing subsystem shown in [Figure 1](#) allows the use of an internal PLL synchronized to either an internal or external clock source that is used by the ECG and BioZ channels.

The PLL generates an output clock (PLL_CLK) that operates over a 4MHz to 28MHz frequency range. The frequency of PLL_CLK is selected by the frequency of REF_CLK and the M divider value, which is set in MDIV[9:0](0x18, 0x19), where $M = MDIV + 1$.

The 10-bit MDIV register field must be set such that the PLL output frequency (PLL_CLK) is between 4MHz and 28MHz. For a reference clock of 32.768kHz, this would mean a valid MDIV range is 122 to 853 ($M = 123$ to 854). For a reference clock of 32.0kHz, this would mean a valid MDIV range of 124 to 874 ($M = 125$ to 875).

Soft-reset using RESET[0](0x11) is not allowed when PLL is enabled (PLL_EN[0](0x18) = 1). If the ECG and BioZ reference is not enabled before PLL_EN is set to 1, it automatically turns on, but can take up to 6ms to settle.

Sequence of Operation when PLL is used

When enabling or disabling PLL, the proper sequence of operations must be followed. This section describes the recommended sequence of operations for various scenarios when PLL is used.

Enabling and Disabling the PLL

The following sequence is recommended when enabling and disabling the PLL.

- Disable ECG, PPG and BioZ, if enabled.
- Enable PLL by setting PLL_EN to 1.
- Wait for PLL to lock using either the FREQ_LOCK[3](0x02) or PHASE_LOCK[2](0x02) status bits.
- Enable ECG, PPG, BioZ as needed.
- Disable ECG, PPG, and BioZ when data collection is done.
- Disable PLL by setting PLL_EN to 0.

Entering and Exiting Shutdown

The following sequence is recommended when putting the device into a shutdown state and to exit the shutdown state.

- Disable ECG, PPG, and BioZ if enabled.
- Disable PLL by setting PLL_EN to 0 if enabled.
- Set SHDN to 1, to enter shutdown mode.
- ...
- Set SHDN to 0 to enter normal mode.
- Enable PLL by setting PLL_EN to 1.
- Enable ECG, PPG, and BioZ as needed.
- ...

Soft-Reset Sequence

The following sequence is recommended when resetting the device using the RESET bit.

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- Disable PLL by setting PLL_EN to 0 if enabled.
- Set RESET = 1 to reset all registers.
- Enable PLL by setting PLL_EN to 1.
- ...

PLL Synchronization

The MAX86178 provides a PLL synchronization feature for use with multiple MAX86176, MAX30005, MAX86178, or Maxim bioimpedance AFEs in a system. This allows the PLLs of the multiple AFEs to remain synchronized and output synchronized samples. PLL synchronization uses either the TRIG pin or the broadcast feature. Both options are discussed as following.

PLL Synchronization Using the TRIG Pin

When the TRIG pin is used for PLL synchronization, one AFE is set up to act as a master and initiates the PLL and timing subsystem synchronization process, while the other(s) act as slave(s). Alternatively, all the AFEs together act as slaves and the microcontroller acts as the master of this process. In either case, all AFEs should use the same external reference clock for the PLLs and all the PLLs must be enabled and locked before generating a timing system reset pulse. The timing when using the MAX86178 in a master configuration is shown in [Figure 2](#). When acting as a master, TRIG_FCFG[7:5](0x13) is set to 0x2 and TIMING_SYS_RESET[7](0x10) is set to 1. TIMING_SYS_RESET is a self clearing bit and gets reset to 0 on the second rising edge of FCLK after it is asserted. Once it is cleared, the MAX86178 sends out a timing system reset pulse on the TRIG output after an internal time delay. On the first FCLK rising edge after the TRIG pin is pulled high by the timing system reset pulse, the ECG N-divider, ECG F-divider, and the BioZ N-divider of the master (if the AFE is the master) restart their counts at 0.

The timing when using the MAX86178 in a slave configuration is shown in [Figure 3](#). When acting as a slave, TRIG_FCFG[7:5] (0x13) is set to 0x1. In this mode, MAX86178 receives a timing system reset pulse on the TRIG pin. After the TRIG input is pulled high, the timing system reset signal is latched by the slave on the first falling edge of FCLK as shown in [Figure 3](#). On the first FCLK rising edge after the timing system reset pulse is latched on the TRIG input, the ECG N-divider, ECG F-divider, and the BioZ N-divider of the slave AFE device(s) restart their count at 0. Since the FCLK input to multiple devices use the same clock, PLLs of all the devices in the system are synchronized automatically.

This is the recommended sequence for synchronizing PLLs on multiple devices using the TRIG pin:

- Disable BioZ by setting ECG_BIOZ_BG_EN[2](0xA0) to 0 and BIOZ_EN[1:0](0xA0) to 0x0 if enabled.
- Disable ECG by settling ECG_EN[0](0x80) to 0 if enabled.
- Disable PPG by setting MEASx_EN (x = 1 to 6) (0x20) to 0 if enabled.
- Reset the part and flush the FIFO by setting SHDN[1](0x11) to 1.
- Then set SHDN = 0 on all the parts .
- Wait for 6ms.
- Program the configuration registers for BioZ, ECG, PPG as needed.
 - For synchronizing multiple devices, the PLLs should be configured such that the PPG frame rate, ECG sample rate, and BioZ sample rate match across all devices.
 - Set ECG_PPG_TIMING_DATA = 1, BIOZ_PPG_TIMING_DATA = 1, ECG_BIOZ_TIMING_DATA = 1, on all the parts (optional).
 - The broadcast feature can be used to program the common registers.
- Set TRIG_FCFG to 0x2 on the master device, and set TRIG_FCFG to 0x1 on all the slave devices.
- Program FIFO_A_FULL[7:0](0x0D) as desired, and A_FULL_EN1[7](0xC0) = 1 on the master device.
- Enable PLL by setting PLL_EN[0](0x18) to 1 on all the parts (using the broadcast feature or separately).
- Wait for PLL to lock on all the devices.
- Enable BioZ by setting ECG_BIOZ_BG_EN to 1, and BIOZ_EN to 0x1 or 0x2 as needed.
- Enable ECG by setting ECG_EN to 1 if needed.
- Enable PPG by setting MEASx_EN (x = 1 to 6) to 1 if needed.
- Set TIMING_SYS_RESET to 1 on the master device. All the devices reset the ECG N-divider, ECG F-divider and the BioZ N-divider, and restart the state machines within the current clock cycle.
 - Note: If both ECG_PPG_TIMING_DATA = 0 and BIOZ_PPG_TIMING_DATA = 0, PPG does not use the PLL, and its state machine does not restart.
- Disable BioZ, ECG, and PPG when data collection is done.

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- Disable PLL by setting PLL_EN to 0.

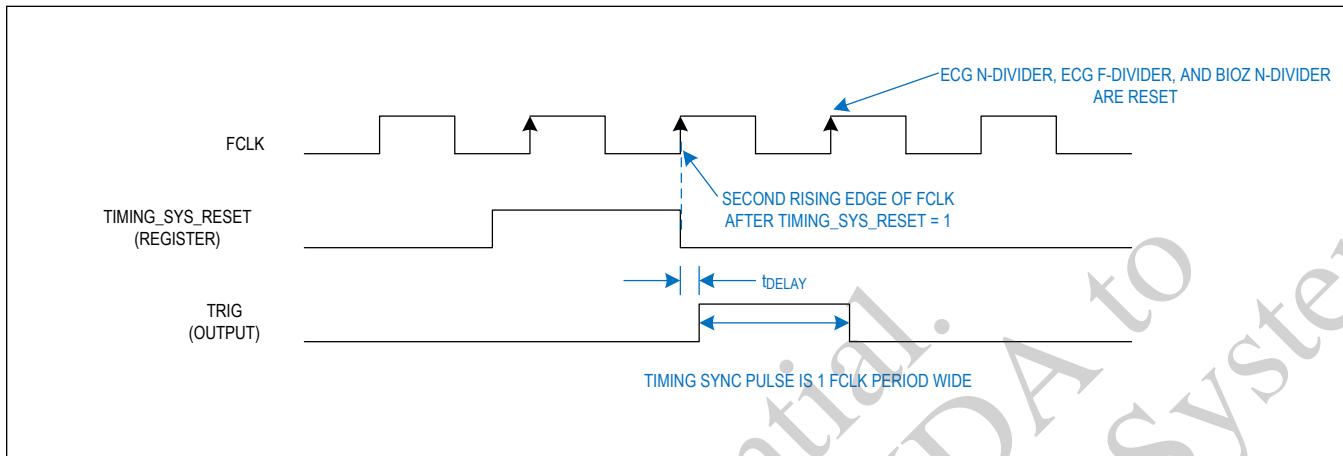


Figure 2. Timing System Synchronization with MAX86178 as a Master

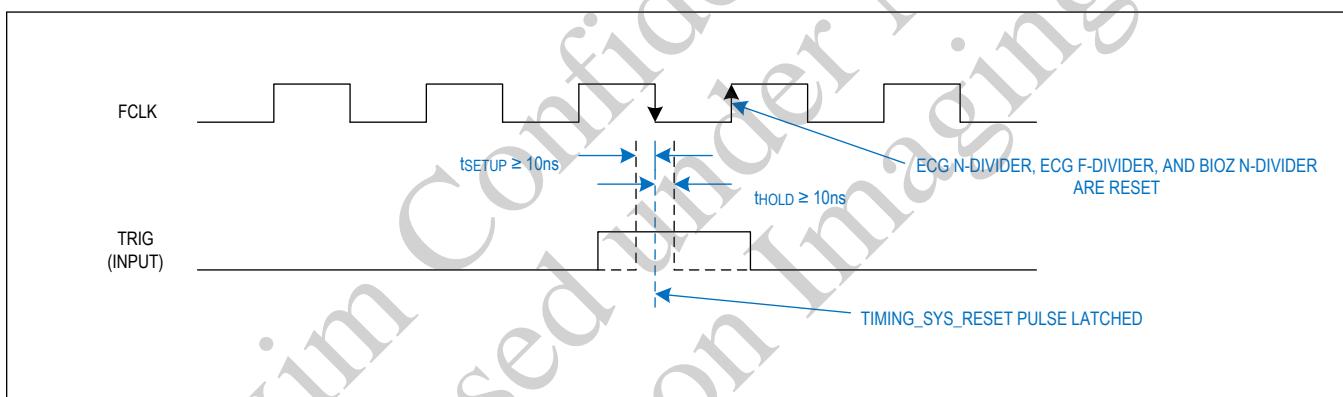


Figure 3. Timing System Synchronization with MAX86178 as a Slave

PLL Synchronization Using the Broadcast Command

PLLs on multiple AFEs can be synchronized using the broadcast feature if the TIMING_SYS_RESET[7](0x10) bit is at the same address in all the devices, and if all the PLLs use the same external reference clock for their PLLs.

Using the I²C Serial Interface:

Set I₂C_BCAST_EN to 1, and I₂C_BCAST_ADDR to the upper 7 bits of the broadcast address chosen for the system on all the AFEs whose PLLs need to be synchronized. Using this address as the Slave Address, write 1 to the TIMING_SYS_RESET bit.

Using the SPI Serial Interface:

Write 1 to the TIMING_SYS_RESET bits of all the AFEs in a single transaction by asserting their CSB inputs at the same time.

The internal timing reset pulse resets the ECG N-divider, ECG F-divider and the BioZ N-divider in all the AFEs at the same time on the third rising edge of the FCLK after TIMING_SYS_RESET bit is set to 1; thus, synchronizing all the PLLs.

This is the recommended sequence for synchronizing PLLs on multiple MAX86178 devices using the broadcast feature:

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- Disable BioZ by setting ECG_BIOZ_BG_EN[2](0xA0) to 0 and BIOZ_EN[1:0](0xA0) to 0x0 if enabled.
- Disable ECG by setting ECG_EN[0](0x80) to 0 if enabled.
- Disable PPG by setting MEASx_EN (x = 1 to 6) to 0.
- Reset the part and flush the FIFO by setting SHDN[1](0x11) to 1.
- Then set SHDN = 0 on all the parts.
- Wait for 6ms.
- Program the configuration registers for BioZ, ECG, and PPG as needed.
 - For synchronizing multiple devices, the PPG frame rate, ECG sample rate, and BioZ sample rate should be the same on all the parts.
 - Set ECG_PPG_TIMING_DATA = 1, BIOZ_PPG_TIMING_DATA = 1, and ECG_BIOZ_TIMING_DATA = 1 on all the parts (optional).
 - The broadcast feature can be used to program the common registers.
- Program FIFO_A_FULL[7:0](0x0D) as desired, and A_FULL_EN1[7](0xC0) = 1 on one of the parts, which becomes the primary part (others parts are secondary parts).
- Enable PLL by setting PLL_EN[0](0x18) to 1 on all the devices (using the broadcast feature or separately).
- Wait for PLL to lock on all devices.
- Enable BioZ by setting ECG_BIOZ_BG_EN to 1 and BIOZ_EN[1:0] to 0x1 or 0x2 as needed using broadcast feature.
- Enable ECG by setting ECG_EN to 1 as needed, using the broadcast feature.
- Enable PPG by setting MEASx_EN (x = 1 to 6) to 1 as needed using the broadcast feature
- Using the broadcast feature, set TIMING_SYS_RESET to 1 on all the devices.
 - All the devices reset the ECG N-divider, ECG F-divider and the BIOZ N-divider, and restart the state machines within the current clock cycle.

Note: If ECG_PPG_TIMING_DATA = 0 and BIOZ_PPG_TIMING_DATA = 0, PPG does not use the PLL, and its state machine does not restart.

- Disable BioZ, ECG, and PPG when data collection is done.

Note: TIMING_SYS_RESET can be set to 1 before or after enabling BioZ, ECG, and PPG.

- Disable PLL by setting PLL_EN to 0.

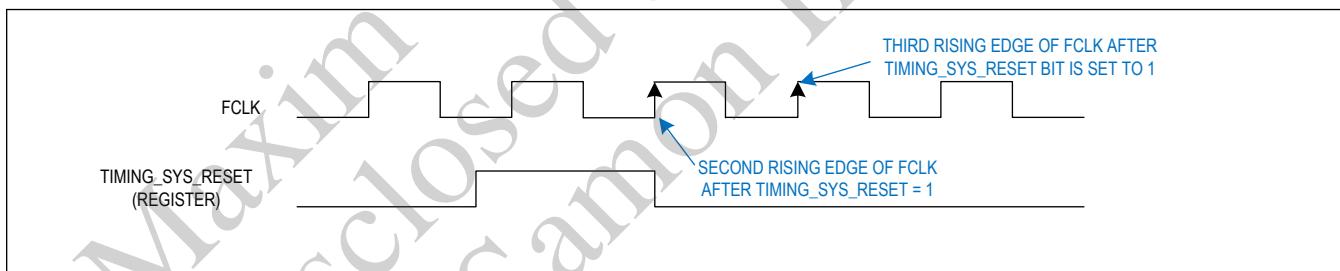


Figure 4. Timing System Synchronization for MAX86178 Using the Broadcast Feature

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PPG Frame Rate

The PPG frame rate (FR_PPG) is set by this equation, and some example frame rates are shown in [Table 1](#).

$$FR_{PPG} = \frac{PPG_FR_CLK}{FR_CLK_DIV[14:0]}$$

The PPG frame rate clock (PPG_FR_CLK) has several sources to allow for synchronized sampling with ECG or BioZ channels.

1. By default, the reference clock (as selected by REF_CLK_SEL[6](0x1D)) provides the PPG_FR_CLK.
2. When both ECG and ECG to PPG timing data are enabled (ECG_EN[0](0x80) = 1 and ECG_PPG_TIMING_DATA[5](0x11) = 1), ECG_ADC_CLK is selected as the PPG_FR_CLK to allow ECG samples and PPG frames to be synchronized.
3. When both BioZ and BioZ to PPG timing data are enabled (BIOZ_EN[1:0](0xA0) = 1 and

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BIOZ_PPG_TIMING_DATA[4](0x11) = 1), BIOZ_ADC_CLK is selected as the PPG_FR_CLK to allow BioZ samples and PPG frames to be synchronized.

- In case all of the above (ECG_EN, ECG_PPG_TIMING_DATA, BIOZ_EN, and BIOZ_PPG_TIMING_DATA) are enabled, PPG_FR_CLK is sourced from ECG_ADC_CLK.

Table 1. PPG Frame Rate Examples

PPG_FR_CLK (kHz)	FR_CLK_DIV[14:0](0x28, 0x29)	FR_PPG (fps)
32.768	16	2048
32.768	256	128
32.868	32766	1.000
32.0	16	2000
32.0	256	125
32.0	32766	0.977

The FR_CLK_DIV should be programmed so that it is greater than the product of $t_{MEASUREMENT}$ and PPG_FR_CLK where $t_{MEASUREMENT}$ is the time to complete all the enabled measurement conversions selected in the MEASx_EN ($x = 1$ to 6) in PPG Configuration 1 (0x20) registers and is calculated as follows.

- $t_{MEASUREMENT} = t_{INIT1} + t_{MEAS1} + t_{MEAS2} + t_{MEAS3} + \dots + t_{MEAS6}$
- $t_{INIT1} = 10 \times t_{FRAME}$
- $t_{MEASx} = [t_{INIT} + MEASx_TINT \times (2 \times MEASx_AVER + 1) + 2 \times MEASx_AVER \times MEASx_PD_SETLNG] \times MEASx_EN$ when using CDM or SINC3 filter.
- $t_{MEASx} = [t_{INIT} + 2 \times MEASx_TINT + MEASx_PD_SETLNG] \times MEASx_EN$ when using FDM and SINC3 is disabled.

where

t_{FRAME} = Frame clock period, 1/PPG_FR_CLK

t_{INIT} = $4 \times t_{FRAME}$

MEASx_TINT = Integration time defined in each measurement

MEASx_AVER = Measurement average for each measurement

MEASx_PD_SETLNG = Photodiode settling time defined in each measurement

MEASx_EN = 1 for each enabled measurement.

For details on all these parameters, refer to the Register Map.

If $t_{MEASUREMENT}$ calculated as above results in a frame period longer than t_{FRAME} , then a timing error occurs and INVALID_PPG_CFG[7](0x01) is set to 1.

If FR_CLK_DIV[14:0] < 0x0010, it is automatically overwritten to 0x0010, which is the period for the smallest frame period. Note that FR_CLK_DIV[14:0] = 0x7FFF is reserved.

The PPG frame rate when using external oscillator depends on the frequency on FCLK and FR_CLK_DIV[14:0]. PPG measurement and frame timing is driven by the on-chip fast oscillator (PPG OSC provides timing for the PPG channel) and remains the same whether using internal or external reference clock.

If PPG configuration registers (0x28 to 0x5F) are modified during measurement, any active frame is aborted and a new frame is started immediately following each register write. This feature prevents corrupted frames from being pushed to the FIFO, but results in a discontinuity in the frame rate because the frame clock divider is reset. If this behavior is not desired, an external frame trigger on the TRIG pin (with PPG_SYNC_MODE[5](0x21) = 1) should be used to maintain consistent frame timing. To avoid dropped frames, register writes should be performed after the completion of a frame and before the start of the next frame.

PPG Synchronization Modes

The MAX86178 supports two synchronization modes for PPG frame rate. The two synchronization modes are internal frame sync and external frame sync, and are controlled by PPG_SYNC_MODE[5](0x21) as shown in [Table 2](#).

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Table 2. Frame Triggers in Synchronization Modes

PPG_SYNC_MODE	PPG FRAME RATE
0	PPG_FR_CLK / FR_CLK_DIV
1	External pulse on TRIG

Internal frame sync mode is the free running mode of operation for PPG. It is also the default mode. In this mode, the MAX86178 uses the PPG_FR_CLK as a frame rate clock, and FR_CLK_DIV[14:0](0x28, 0x29) as the internal user programmable divider to set the time between subsequent frames or the PPG frame rate. External frame sync mode is a one-shot mode of operation for PPG. Setting TRIG_FCFG[7:5](0x13) to 0x0 and PPG_SYNC_MODE[5](0x21) to 1 enables the TRIG input to trigger a PPG frame. On either the falling edge (TRIG_ICFG[4](0x13) = 0) or the rising edge (TRIG_ICFG[4](0x13) = 1) of the TRIG input, a frame cycle begins. A frame cycle includes a power-up cycle and execution of each enabled measurement from MEAS1 to MEAS6.

ECG Sample Rate and AC Lead-Off Frequency

The ECG sample rate depends on the state of the following:

- CLK_FREQ_SEL[5](0x1D) defines the frequency of the reference clock
- REF_CLK_SEL[6](0x1D) selects the reference clock for input to PLL
- MDIV[9:0](0x18, 0x19) is the M divider
- ECG_FDIV[3:0](0x1B) is the ECG F divider
- ECG_NDIV[10:0] (0x1B, 0x1C) is the ECG N divider
- ECG_DEC_RATE[3:1](0x80) sets the decimation factor for ECG ADC

The ECG sample rate is calculated as follows.

- $\text{SR_ECG} = \frac{\text{ECG_ADC_CLK}}{\text{ECG_DEC_RATE}}$
- $\text{ECG_ADC_CLK} = \frac{\text{PLL_CLK}}{\text{ECG_FDIV} \times \text{ECG_NDIV}}$ (must be between 19.0kHz and 32.768kHz)
- $\text{PLL_CLK} = \text{REF_CLK} \times M$ (must be between 4.0MHz and 28MHz)

REF_CLK is either 32.0kHz or 32.768kHz depending on the state of the CLK_FREQ_SEL and REF_CLK_SEL bits, and M = MDIV + 1.

The AC lead-off stimulus frequency is calculated as follows:

- $F_{\text{ECG_AC_LOFF}} = \frac{Q \times \text{ECGADC_CLK}}{\text{ECG_LOFF_FREQ}}$
- $Q = \text{ROUNDUP}\left(\frac{\text{ECG_NDIV}}{\text{ROUND}\left(\frac{\text{ECG_NDIV}}{16}\right)}\right)$

Table 3 shows some common ECG sample rates optimized for minimum supply-current consumption. To minimize supply-current consumption for continuous ECG monitoring, PLL_CLK should be set to the lowest frequency possible between 4MHz and 28MHz. ECG_FDIV should be set to the highest value possible while maintaining ECG_ADC_CLK between 19kHz and 32.768kHz.

Table 3. Common ECG Sample Rates

SR_ECG (sps)	REF_CLK (kHz)	M = MDIV + 1	PLL_CLK (MHz)	ECG_FDIV	ECG_NDIV	ECG_ADC_CLK (kHz)	ECG_DEC_RATE
125	32.768	125	4.096	8	16	32.0	256
128	32.768	128	4.194	8	16	32.768	256
200	32.768	200	6.554	16	16	25.4	128
250	32.768	125	4.096	8	16	32.0	128
256	32.768	128	4.194	8	16	32.768	128
300	32.768	150	4.915	16	16	19.2	64

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Table 3. Common ECG Sample Rates (continued)

SR_ECG (sps)	REF_CLK (kHz)	M = MDIV + 1	PLL_CLK (MHz)	ECG_FDIV	ECG_NDIV	ECG_ADC_CLK (kHz)	ECG_DEC_RATE
360	32.768	180	5.898	16	16	23.04	64
500	32.768	125	4.096	8	16	32.0	64
512	32.768	128	4.194	8	16	32.768	64
1000	32.768	125	4.096	8	16	32.0	32
1024	32.768	128	4.194	8	16	32.768	32
2000	32.768	125	4.096	8	16	32.0	16
2048	32.768	128	4.194	8	16	32.768	16

BioZ Sample Rate and Stimulus Frequency

To make a BioZ measurement, the parameters listed below must be set, and then either I or Q measurements enabled by BIOZ_EN[1:0](0xA0).

The BioZ sample rate and stimulus frequencies depend on the state of the following fields:

- MDIV[9:0](0x18, 0x19)
- BIOZ_NDIV[7:6](0x1A)
- BIOZ_KDIV[3:0](0x1A)
- BIOZ_ADC_OS[5:3](0xA0)
- BIOZ_DAC_OS[7:6](0xA0)
- CLK_FREQ_SEL[5](0x1D)
- REF_CLK_SEL[6](0x1D)

The BioZ sample rate is calculated as follows.

- $SR_{BIOZ} = \frac{PLL_CLK}{BIOZ_NDIV \times BIOZ_ADC_OSR}$
- $BIOZ_ADC_CLK = \frac{PLL_CLK}{BIOZ_NDIV}$ (must be between 16.0kHz and 36.375kHz)
- $PLL_CLK = M \times REF_CLK$ (must be between 4MHz and 28MHz)

REF_CLK is either 32.0kHz or 32.768kHz depending on the state of the CLK_FREQ_SEL and REF_CLK_SEL bits, and M = MDIV + 1.

The BioZ stimulus frequency is set by the following equation.

- $F_{BIOZ} = \frac{PLL_CLK}{BIOZ_KDIV \times BIOZ_DAC_OSR}$
- $BIOZ_SYNTH_CLK = \frac{PLL_CLK}{BIOZ_KDIV}$ (must be between 4096Hz and 28MHz)

The ratio of F_{BIOZ} to SR_{BIOZ} must be an integer value or 0.5, so that each BioZ sample is integrated over a given number of stimulus half-cycles. This ratio, C_BIOZ, is calculated by the following equation.

- $C_{BIOZ} = \frac{F_{BIOZ}}{SR_{BIOZ}} = \frac{BIOZ_NDIV \times BIOZ_ADC_OSR}{BIOZ_KDIV \times BIOZ_DAC_OSR}$

The procedure for setting the BioZ timing parameters is as follows:

First decide the target stimulus frequency (F_{BIOZ}) for the BioZ measurement.

If $F_{BIOZ} < 54,668\text{Hz}$

1. Set BIOZ_DAC_OS[5:0] = 256.
2. Set BIOZ_KDIV to get PLL_CLK in range (see Note below [Table 6](#)).
3. Calculate MDIV + 1 = ROUND(PLL_CLK / REF_CLK).
4. Set BIOZ_NDIV to get BIOZ_ADC_CLK in range.
5. Set BIOZ_ADC_OS[5:3] so that C is an integer or 0.5.

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If $F_{BIOZ} > 54,668\text{Hz}$

1. Set $BIOZ_KDIV = 1$.
2. Set $BIOZ_DAC_OSR$ to get PLL_CLK in range.
3. Calculate $MDIV + 1 = \text{ROUND}(PLL_CLK / REF_CLK)$.
4. Set $BIOZ_NDIV$ to get $BIOZ_ADC_CLK$ in range.
5. Set $BIOZ_ADC_OSR$ so that C is an integer or 0.5.

Examples are shown in [Table 4](#) and [Table 5](#)

Table 4. Example Calculations of BioZ Configuration Parameters for $F_{BIOZ} < 54688\text{Hz}$

STEP	APPLICATION	EX1	EX2	EX3	EX4	EX5
	EDA/GSR	X	X	X		
	BIA/BIS			X	X	X
	RESP					X
	ICG					
	CLK_REF	32,768	32,768	32,768	32,768	32,768
Target	F_{BIOZ}	8	100	1,000	10,000	40,000
Step 1	$BIOZ_DAC_OSR[2:0]$	256	256	256	256	256
Target	$BIOZ_SYNTH_CLK$	2,048	25,600	256,000	2,560,000	10,240,000
Step 2	$BIOZ_KDIV[3:0]$	8192	1024	64	8	2
Target	PLL_CLK	16,777,216	26,214,400	16,384,000	20,480,000	20,480,000
Step 3	$MDIV[9:0] + 1$	512	800	500	625	625
Step 4	$BIOZ_NDIV[3:0]$	1024	1024	512	1024	1024
Target	$BIOZ_ADC_CLK$	16,384	25,600	32,000	20,000	20,000
Step 5	$BIOZ_ADC_OSR[2:0]$	1024	512	128	128	128
	C	0.5	2	4	64	256
Actual	PLL_CLK	16,777,216	26,208,000	16,384,000	20,480,000	20,480,000
Actual	$BIOZ_ADC_CLK$	16,384	25,600	32,000	20,000	20,000
Actual	$BIOZ_SYNTH_CLK$	2,048	25,600	256,000	2,560,000	10,240,000
Actual	SR_{BIOZ}	16	50	250	156.25	156.25
Actual	F_{BIOZ}	8	100	1,000	10,000	40,000
Actual	Error	0.00%	0.00%	0.00%	0.00%	0.00%

Table 5. Example Calculations of BioZ Configuration Parameters for $F_{BIOZ} > 54688\text{Hz}$

STEP	APPLICATION	EX1	EX2	EX3	EX4	EX5
	EDA/GSR					
	BIA/BIS	X	X	X	X	X
	RESP	X	X	X		
	ICG	X	X	X		
	CLK_REF	32,768	32,768	32,768	32,768	32,768
Target	F_{BIOZ}	54688	100000	150,000	250,000	500,000

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Table 5. Example Calculations of BioZ Configuration Parameters for F_BIOZ > 54688Hz (continued)

STEP	APPLICATION	EX1	EX2	EX3	EX4	EX5
Step 1	BIOZ_KDIV[3:0]	1	1	1	1	1
Target	BIOZ_DAC_OSР[2:0]	256	256	128	64	32
Step 2	BIOZ_SYNTH_CLK	14000128	25600000	19200000	16000000	16000000
Target	PLL_CLK	14,000,128	25,600,000	19,200,000	16,000,000	16,000,000
Step 3	MDIV[9:0] + 1	427	781	586	488	488
Step 4	BIOZ_NDIV[3:0]	512	1024	1024	512	512
Target	BIOZ_ADC_CLK	27,344	25,000	18,750	31,250	31,250
Step 5	BIOZ_ADC_OSР[2:0]	128	128	128	256	256
	C	427	512	1024	2048	4096
Actual	PLL_CLK	13,991,936	25,591,808	19,202,048	15,990,784	15,990,784
Actual	BIOZ_ADC_CLK	27,328	24,992	18,752	31,232	31,232
Actual	BIOZ_SYNTH_CLK	13,991,936	25,591,808	19,202,048	15,990,784	15,990,784
Actual	SR_BIOZ	213.5	195.25	146.5	122.0	122
Actual	F_BIOZ	54,656	99,968	150,016	249,856	499,712
Actual	Error	-0.06%	-0.03%	0.01%	-0.06%	-0.06%

Some common stimulus frequencies are shown in [Table 6](#) for REF_CLK frequencies of 32.768kHz. In the BioZ receive channel, the demodulation is done at the same frequency as the stimulus.

Table 6. Common BioZ Stimulus Frequencies and Sample Rates with REF_CLK = 32.768kHz

REF_CLK (Hz)	M (MDIV + 1)	PLL_CLK (Hz)	BIOZ_KDIV	BIOZ_DAC_OSР	F_BIOZ (Hz)	BIOZ_NDIV	BIOZ_ADC_OSР	INTEGRATION CYCLES	SR_BIOZ (sps)
32768	790	25886720	1	32	808960	1024	128	4096	197.50
32768	706	23134208	1	32	722944	1024	128	4096	176.50
32768	634	20774912	1	32	649216	1024	128	4096	158.50
32768	568	18612224	1	32	581632	512	128	2048	284.00
32768	488	15990784	1	32	499712	512	128	2048	244.00
32768	458	15007744	1	32	468992	512	128	2048	229.00
32768	822	26935296	1	64	420864	1024	128	2048	205.50
32768	738	24182784	1	64	377856	1024	128	2048	184.50
32768	662	21692416	1	64	338944	1024	128	2048	165.50
32768	594	19464192	1	64	304128	1024	128	2048	148.50
32768	533	17465344	1	64	272896	512	128	1024	266.50
32768	488	15990784	1	64	249856	512	128	1024	244.00
32768	479	15695872	1	64	245248	512	128	1024	239.50
32768	430	14090240	1	64	220160	512	128	1024	215.00
32768	781	25591808	1	128	199936	1024	128	1024	195.25
32768	691	22642688	1	128	176896	1024	128	1024	172.75

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REF_CLK (Hz)	M (MDIV + 1)	PLL_CLK (Hz)	BIOZ_KDIV	BIOZ_DAC_OSRR	F_BIOZ (Hz)	BIOZ_NDIV	BIOZ_ADC_OSRR	INTEGRATION CYCLES	SR_BIOZ (sps)
32768	621	20348928	1	128	158976	1024	128	1024	155.25
32768	559	18317312	1	128	143104	512	128	512	279.50
32768	512	16777216	1	128	131072	512	128	512	256.00
32768	449	14712832	1	128	114944	512	128	512	224.50
32768	781	25591808	1	256	99968	1024	128	512	195.25
32768	727	23822336	1	256	93056	1024	128	512	181.75
32768	648	21233664	1	256	82944	1024	128	512	162.00
32768	641	21004288	1	256	82048	1024	128	512	160.25
32768	586	19202048	1	256	75008	1024	128	512	146.50
32768	523	17137664	1	256	66944	512	128	256	261.50
32768	469	15368192	1	256	60032	512	128	256	234.50
32768	844	27656192	2	256	54016	1024	128	256	211.00
32768	781	25591808	2	256	49984	1024	128	256	195.25
32768	672	22020096	2	256	43008	1024	128	256	168.00
32768	641	21004288	2	256	41024	1024	128	256	160.25
32768	609	19955712	2	256	38976	1024	256	512	76.13
32768	547	17924096	2	256	35008	512	256	256	136.75
32768	484	15859712	2	256	30976	512	256	256	121.00
32768	438	14352384	2	256	28032	512	256	256	109.50
32768	781	25591808	4 (See Note)	256	24992	1024	256	256	97.63
32768	719	23560192	4 (See Note)	256	23008	1024	256	256	89.88
32768	625	20480000	4 (See Note)	256	20000	1024	256	256	78.13
32768	563	18448384	4 (See Note)	256	18016	512	256	128	140.75
32768	500	16384000	4 (See Note)	256	16000	512	256	128	125.00
32768	469	15368192	4 (See Note)	256	15008	512	256	128	117.25
32768	438	14352384	4 (See Note)	256	14016	512	256	128	109.50
32768	813	26640384	8	256	13008	1024	256	128	101.63
32768	750	24576000	8	256	12000	1024	256	128	93.75
32768	688	22544384	8	256	11008	1024	256	128	86.00
32768	625	20480000	8	256	10000	1024	256	128	78.13
32768	563	18448384	8	256	9008	1024	256	128	70.38
32768	500	16384000	8	256	8000	512	256	64	125.00

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REF_CLK (Hz)	M (MDIV + 1)	PLL_CLK (Hz)	BIOZ_KDIV	BIOZ_DAC_OSР	F_BIOZ (Hz)	BIOZ_NDIV	BIOZ_ADC_OSР	INTEGRATION CYCLES	SR_BIOZ (sps)
32768	438	14352384	8	256	7008	512	256	64	109.50
32768	750	24576000	16	256	6000	1024	256	64	93.75
32768	625	20480000	16	256	5000	1024	256	64	78.13
32768	500	16384000	16	256	4000	512	256	32	125.00
32768	500	16384000	32	256	2000	512	512	32	62.50
32768	500	16384000	64	256	1000	512	1024	32	31.25
32768	500	16384000	128	256	500	512	1024	16	31.25
32768	500	16384000	256	256	250	512	1024	8	31.25
32768	500	16384000	512	256	125	512	1024	4	31.25
32768	500	16384000	1024	256	63	512	1024	2	31.25
32768	500	16384000	2048	256	31	512	1024	1	31.25
32768	500	16384000	4096	256	16	1024	1024	1	15.63
32768	500	16384000	8192	256	8	1024	1024	0.5	15.63

Note: Setting BIOZ_KDIV = 4 results in a larger offset in the receive channel. If a calibration is applied to the measurement, this effect is negated by the offset measurement and subtraction. If no calibration is applied and accurate impedance is desired, it is recommended to avoid using this setting, and instead lowering MDIV by a factor of two to achieve the desired frequency with BIOZ_KDIV = 2.

Respiration Sample Rate and Stimulus Frequency

To enable respiration mode, set RESP_EN[0](0xB6). In this mode, the stimulus frequency and sample rate have slightly different control registers than other BioZ modes.

The respiration sample rate and stimulus frequencies depend on the state of the following fields:

- MDIV[9:0](0x18, 0x19)
- ECG_FDIV[3:0](0x1B)
- BIOZ_NDIV[7:6](0x1A)
- BIOZ_KDIV[3:0](0x1A)
- BIOZ_ADC_OSР[5:3](0xA0)
- BIOZ_DAC_OSР[7:6](0xA0)
- CLK_FREQ_SEL[5](0x1D)
- REF_CLK_SEL[6](0x1D)

The respiration sample rate is calculated as follows.

- SR_RESP = $\frac{\text{PLL_CLK}}{\text{ECG_FDIV} \times \text{BIOZ_NDIV} \times \text{BIOZ_ADC_OSР}}$
- BIOZ_ADC_CLK = $\frac{\text{PLL_CLK}}{\text{BIOZ_NDIV} \times \text{ECG_FDIV}}$ (must be between 16.0kHz and 36.375kHz)
- PLL_CLK = $M \times \text{REF_CLK}$ (must be between 4MHz and 28MHz)

REF_CLK is either 32.0kHz or 32.768kHz depending on the state of the CLK_FREQ_SEL and REF_CLK_SEL bits, and M = MDIV + 1.

The respiration stimulus frequency is calculated as follows.

- F_RESP = $\frac{\text{PLL_CLK}}{\text{ECG_FDIV} \times \text{BIOZ_KDIV} \times \text{BIOZ_DAC_OSР}}$

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- $\text{BIOZ_SYNTH_CLK} = \frac{\text{PLL_CLK}}{\text{BIOZ_KDIV} \times \text{ECG_FDIV}}$ (must be between 4096Hz and 28MHz)

The ratio of F_RESP to SR_RESP must be an integer value or 0.5, so that each respiration sample is integrated over a given number of stimulus half-cycles. This ratio (C_RESP) is calculated by the following equation.

$$\bullet \quad C_{\text{RESP}} = \frac{F_{\text{RESP}}}{SR_{\text{RESP}}} = \frac{\text{BIOZ_NDIV} \times \text{BIOZ_ADC_OSR}}{\text{BIOZ_KDIV} \times \text{BIOZ_DAC_OSR}}$$

Table 7 shows some common combinations of ECG sample rates and respiration sample rates since the two features are commonly used together. To minimize supply current consumption for continuous ECG and respiration monitoring, PLL_CLK should be set to the lowest frequency between 4MHz and 28MHz allowed by the BIOZ_ADC_CLK range (16.0kHz to 36.375kHz).

Table 7. Common ECG and Respiration Sample Rates

SR_ECG (sps)	REF_CLK (kHz)	M (MDIV + 1)	PLL_CLK (MHz)	ECG_FDIV	ECG_NDIV	ECG_ADC_CLK (kHz)	ECG_DEC_RATE	BIOZ_NDIV	BIOZ_ADC_CLK (kHz)	BIOZ_ADC_OSR	SR_RESP (sps)
128	32.768	128	4.194	1	128	32.768	256	256	16.384	512	32
125	32.768	125	4.096	1	128	32	256	256	16	512	31.25
200	32.768	200	6.554	1	256	25.6	128	256	25.6	1024	25
250	32.768	125	4.096	1	128	32	128	256	16	512	31.25
256	32.768	128	4.194	1	128	32.768	128	256	16.384	512	32
300	32.768	150	4.915	1	256	19.2	64	256	19.2	512	37.5
360	32.768	180	5.898	1	256	23.04	64	256	23.04	512	45
500	32.768	250	4.096	1	128	32	64	256	16	256	50
512	32.768	256	4.194	1	128	32.768	64	256	16.384	256	64

Note: Setting BIOZ_KDIV = 4 results in a larger offset in the receive channel. It is recommended to avoid this setting for respiration applications, and instead increase MDIV or FDIV by a factor of two to achieve the desired frequency with BIOZ_KDIV = 2 or 8.

Timing Data in the FIFO

The MAX86178 supports the timing reference of samples in the FIFO for the separate data paths (PPG, ECG, and BioZ) with respect to each other. Below are the details on ECG-to-PPG timing reference, BioZ-to-PPG timing reference, and ECG-to-BioZ timing reference.

ECG-to-PPG Timing Data

The timing reference of PPG samples with respect to the ECG samples in the FIFO is supported by setting ECG_PPG_TIMING_DATA[5](0x11) to 1. When this bit is set to 1, PPG timing data is saved in the FIFO at the start of the first measurement in a PPG frame. This timing data is the number of PPG frame clock (PPG_FR_CLK) cycles, starting from the time when the last ECG sample was saved in the FIFO until the first PPG measurement in a frame starts. The timing data is 10 bits wide and saturates at 0x3FF.

See the [FIFO Description](#) section for information on the tag used for ECG-to-PPG timing data. [Figure 5](#), [Figure 6](#), and [Figure 7](#) show some examples.

The timing of each measurement after the PPG Timing Data is saved in the FIFO is shown in [Figure 8](#).

Timing calculations for measurements with MEASx_SINC3 = 1 (SINC3 mode) or MEASx_filt_SEL = 0 (CDM mode) are:

$$t_1 = 64 \text{ fast clocks (10MHz)}$$

$$t_{2n} = \text{MEASx_TINT} \times (2 \times \text{MEASx_AVER} + 1) + \text{MEASx_PD_SETLNG} \times 2 \times \text{MEASx_AVER}$$

$$t_{3n} = \text{Roundup}((t_1 + t_{2n}) / t_{\text{FRAME}}) + 3 \times \text{PPG_FR_CLK} \text{ cycles}$$

Timing calculations for measurements with MEASx_SINC3 = 0 (POR) and MEASx_filt_SEL = 1 (FDM mode) are:

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$t_1 = 64$ fast clocks (10 MHz)

$t_{2n} = 2 \times \text{MEASx_TINT} + \text{MEASx_PD_SETLNG}$

$t_{3n} = \text{Roundup}((t_1 + t_{2n}) / t_{\text{FRAME}}) + 3 \times \text{PPG_FR_CLK}$ cycles

where,

t_{FRAME} = Frame Clock period (32.0kHz/32.768kHz)

MEASx_TINT = Integration time defined for each measurement ($x = 1$ to 6)

MEASx_AVER = Number of averages defined for each measurement ($x = 1$ to 6)

MEASx_PD_SETLNG = Photodiode settling time defined for each measurement ($x = 1$ to 6)

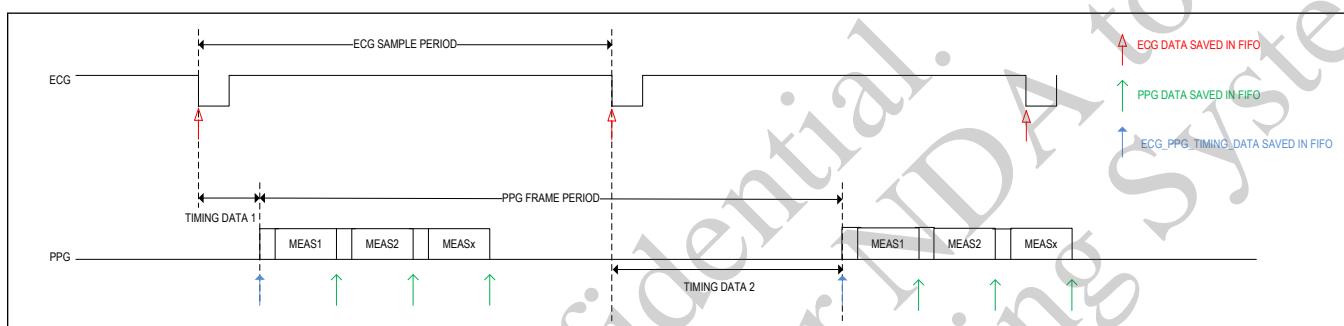


Figure 5. Example 1: ECG Sample Rate Faster than PPG Frame Rate

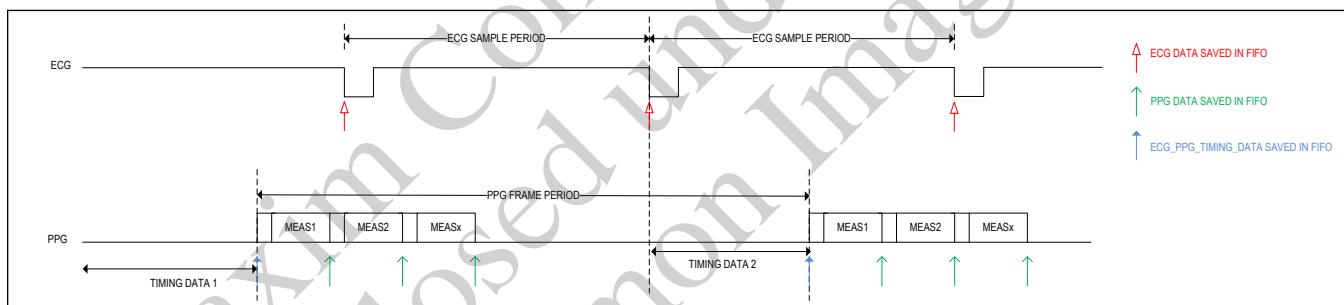


Figure 6. Example 2: ECG Sample Rate Faster than PPG Frame Rate

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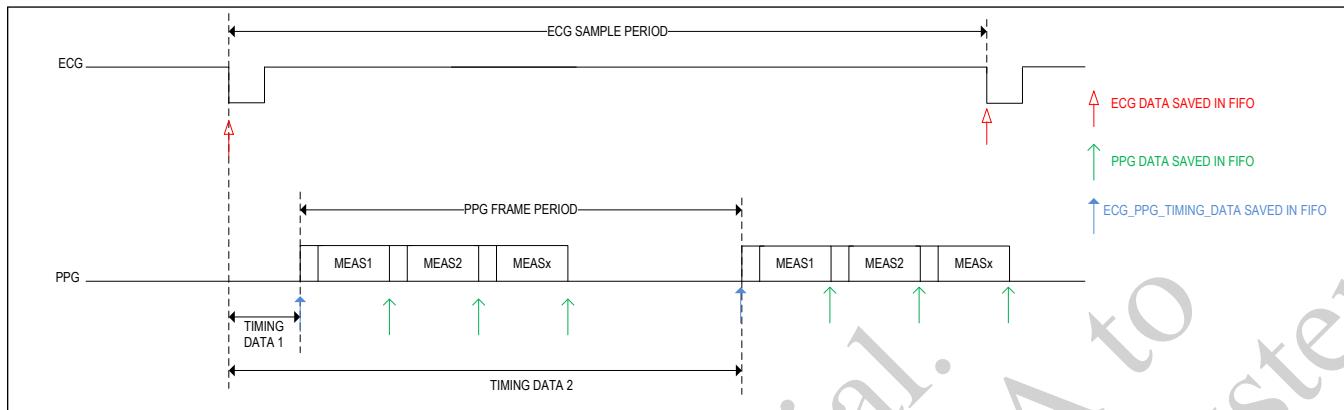


Figure 7. Example 3: ECG Sample Rate Slower than PPG Frame Rate

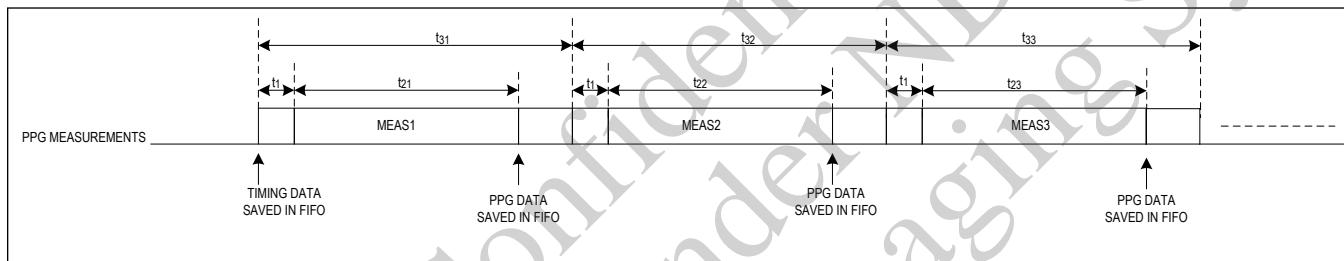


Figure 8. PPG Measurement Timing in a Frame

BioZ-to-PPG Timing Data

The timing reference of the PPG samples with respect to the BioZ samples in the FIFO is supported by setting BIOZ_PPG_TIMING_DATA[4](0x11) to 1. When this bit is set to 1, PPG timing data is saved in the FIFO at the start of the first measurement in a PPG frame. This timing data is the number of PPG frame clock (PPG_FR_CLK) cycles, starting from the time when the last BioZ sample was saved in the FIFO until the first PPG measurement in a frame starts. The timing data is 14 bits wide and saturates at 0x3FFF.

See the [FIFO Description](#) section for information on the tag used for BioZ-to-PPG timing data. [Figure 9](#), [Figure 10](#), and [Figure 11](#) show some examples.

The timing calculation for measurements is explained in the [ECG to PPG Timing Data](#) section.

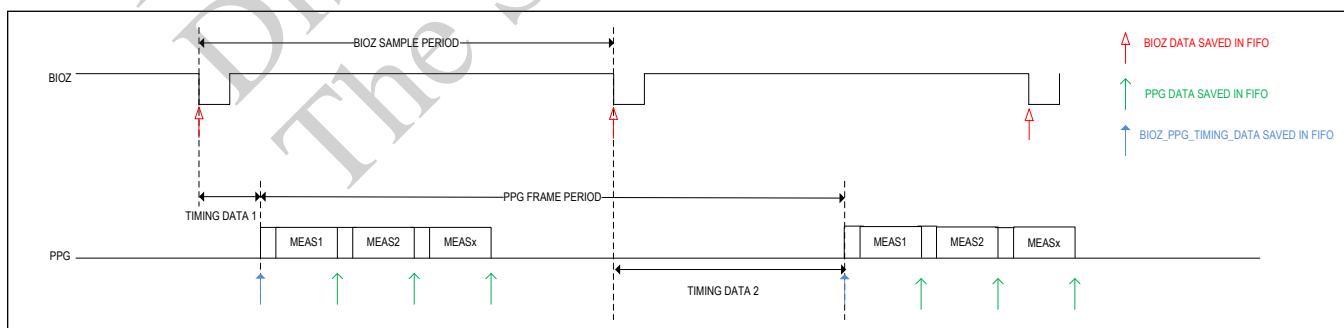


Figure 9. Example 1: BioZ Sample Rate Faster than PPG Frame Rate

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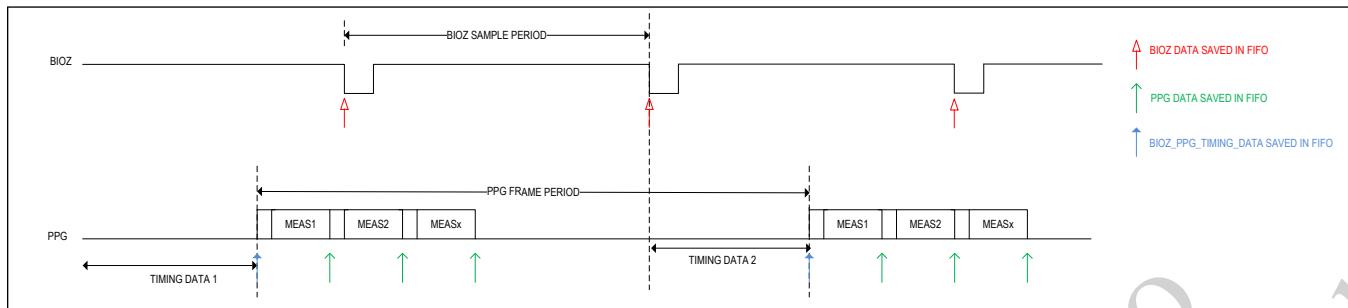


Figure 10. Example 2: BioZ Sample Rate Faster than PPG Frame Rate

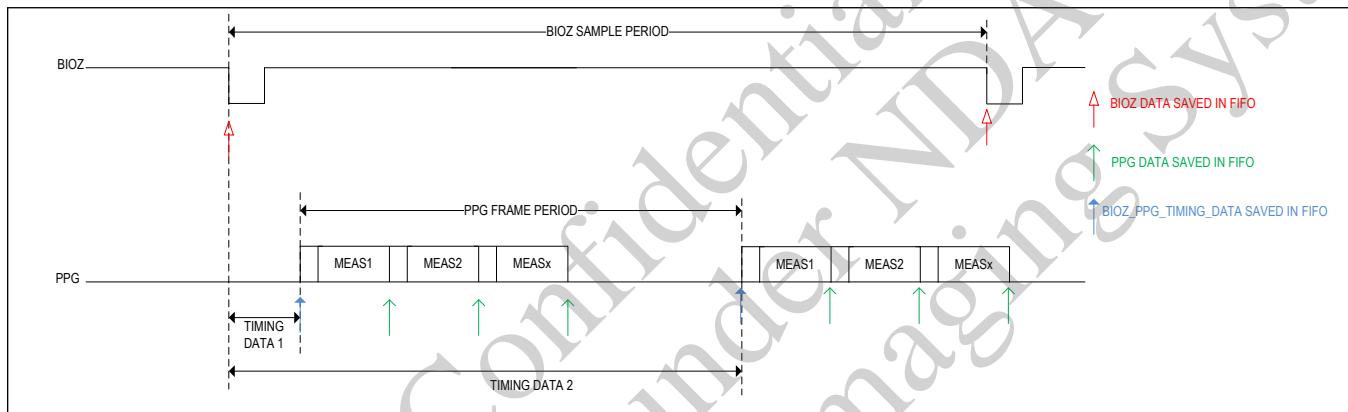


Figure 11. Example 3: BioZ Sample Rate Slower than PPG Frame Rate

ECG-to-BioZ Timing Data

The timing reference of BioZ samples with respect to ECG samples in the FIFO is supported by setting ECG_BIOZ_TIMING_DATA[3](0x11) to 1. When this bit is set to 1, BioZ timing data is saved in the FIFO when the BioZ data is ready to be saved in the FIFO. This timing data is the number of PLL reference clock (REF_CLK) cycles, starting from the time when the last ECG sample was saved to FIFO until the BioZ data is ready to be saved in the FIFO. The timing data is 10 bits wide and saturates at 0x3FF.

See the [FIFO Description](#) section for information on the tag used for ECG-to-BioZ timing data. [Figure 12](#), [Figure 13](#), and [Figure 14](#) show some examples.

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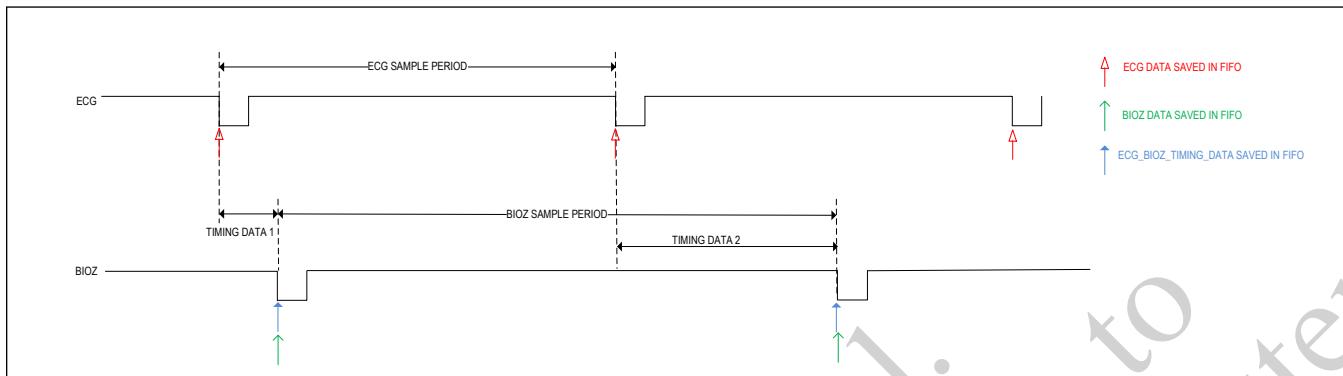


Figure 12. Example 1: ECG Sample Rate Faster than BioZ Sample Rate

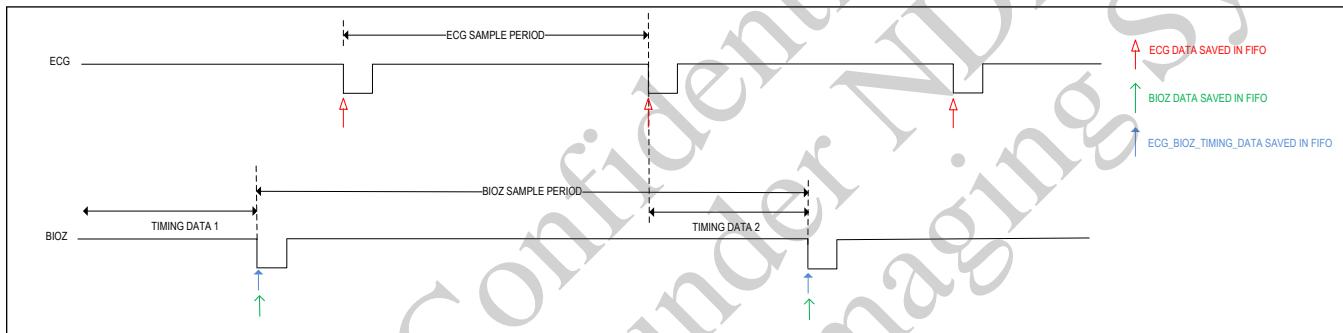


Figure 13. Example 2: ECG Sample Rate Faster than BioZ Sample Rate

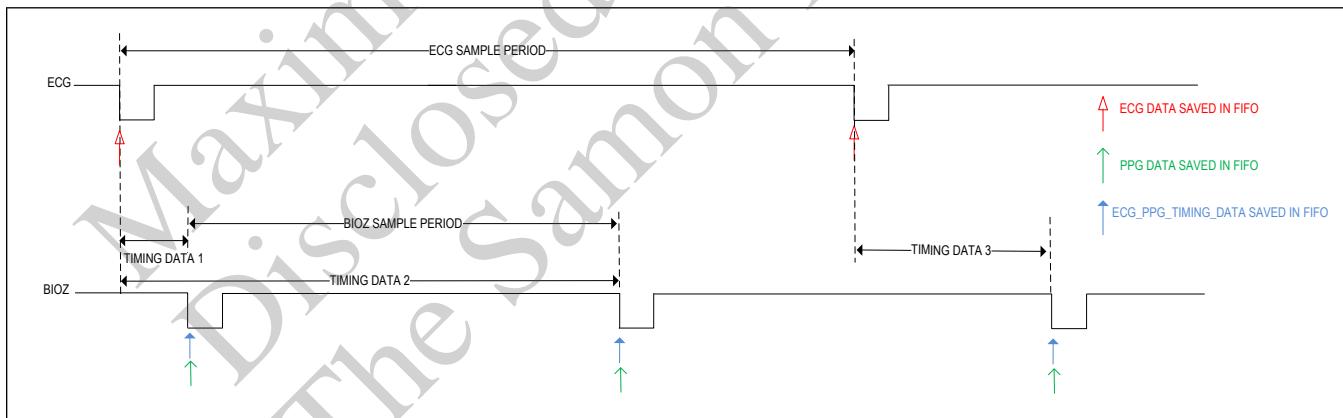


Figure 14. Example 3: ECG Sample Rate Slower than BioZ Sample Rate

PPG, ECG, and BioZ Signal Alignment

In order to temporally align the PPG, ECG, and BioZ analog signals with high precision, the latency of the ECG and BioZ signal chains need to be considered in addition to the digital sample alignment provided by the FIFO timing data. Because PPG samples are integrated over individual time windows, their timing is well defined by the timing subsystem with very little analog latency. However, the ECG and BioZ channels have multiple sources of latency between the analog

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signal entering the MAX86178 and digitized samples entering the FIFO. These include the analog HPF, INA, PGA, anti-aliasing filter, and the delta-sigma ADC with its low-pass decimation filter. This latency results in the digitized ECG and BioZ signals lagging behind the digitized PPG signal, as shown in [Figure 15](#). If precise signal alignment is needed, the relative latencies between each pair of channels should be characterized at the sample rates intended for the application.

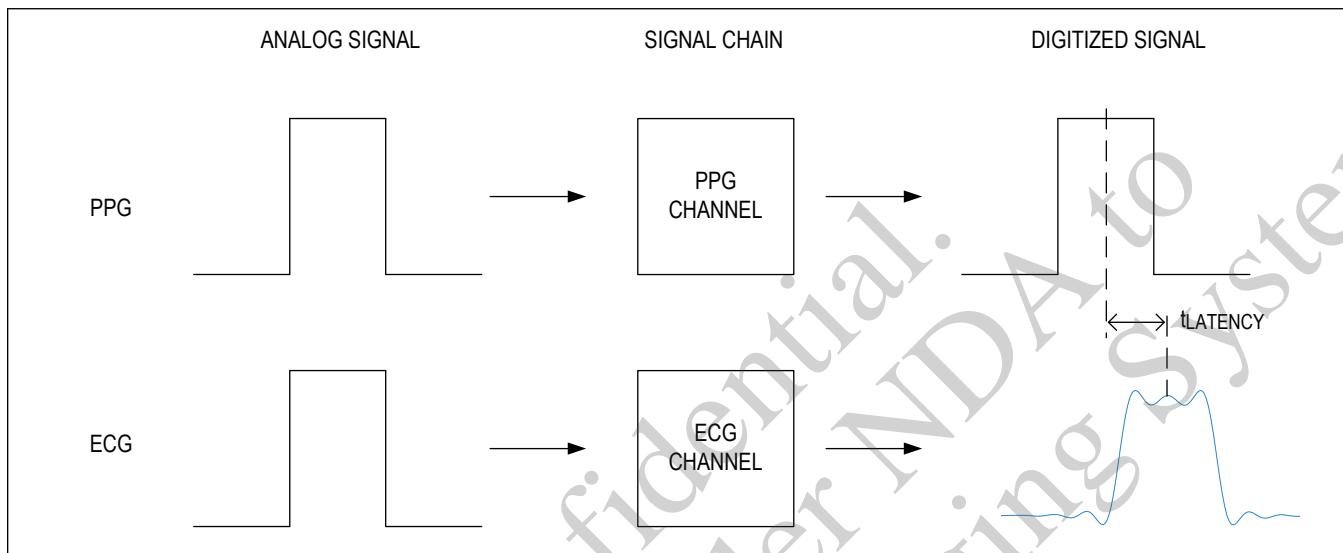


Figure 15. ECG and PPG Simultaneous Pulse Response

PPG

The PPG system in MAX86178 has two high-current LED drivers that support a total of 6 LED drive-output pins through two on-chip 6 x 1 multiplexers and control logic. Each driver has an 8-bit programmable DAC that can be programmed for a wide range of LED drive-current settings. The optical receiver has two high resolution readout channels that operate simultaneously and are connected to 4 PD input pins through on-chip control logic. Each individual channel has robust ambient-light cancellation in analog and digital domains. The PPG data from both ADCs in the two channels is stored in the 256-word FIFO, which can be analyzed and used in a number of different applications. The PPG system in MAX86178 can operate on a single supply voltage ranging between 3.1V and 5.5V that supplies V_{LED} to the LED driver as well as input to the on-chip LDO at LDO_IN. In this case, LDO_OUT is connected to AVDD and DVDD; thereby, providing +1.8V for the AFE. Alternatively, the AFE main supply at AVDD and DVDD can be connected to an external +1.8V without using on-chip LDO.

The PPG system in MAX86178 operates in a dynamic power-down mode, always powering down between frames to minimize power consumption. For more details on the power consumption at various sample rates, refer to the [Electrical Characteristics](#) table.

Keeping the voltage ripple on the V_{LED} as low as possible ensures the highest SNR is achieved. If a regulated supply is not available, the switching frequency on V_{LED} should be kept between 100kHz and 3MHz. By ensuring the switching frequency stays within the recommended range, along with a good load-transient response, high SNR can be maintained at the heaviest loads (high LED drive-current applications).

The MAX20345 or the smaller MAX20343 are recommended solutions for a buck-boost supplying V_{LED} . Both offer highly efficient buck-boost regulators with a very small load ripple, fast load-transient responses, and have load-pulse consistencies that provide more than 90dB SNR in a white card DC SNR test. Higher SNR is achieved by enabling the DAC offset in addition to utilizing the on-chip averaging and off-chip low-pass or band-pass filtering, allowing for 110dB SNR to be achieved.

The various blocks and features in the PPG system of MAX86178 are discussed in detail in the following sections.

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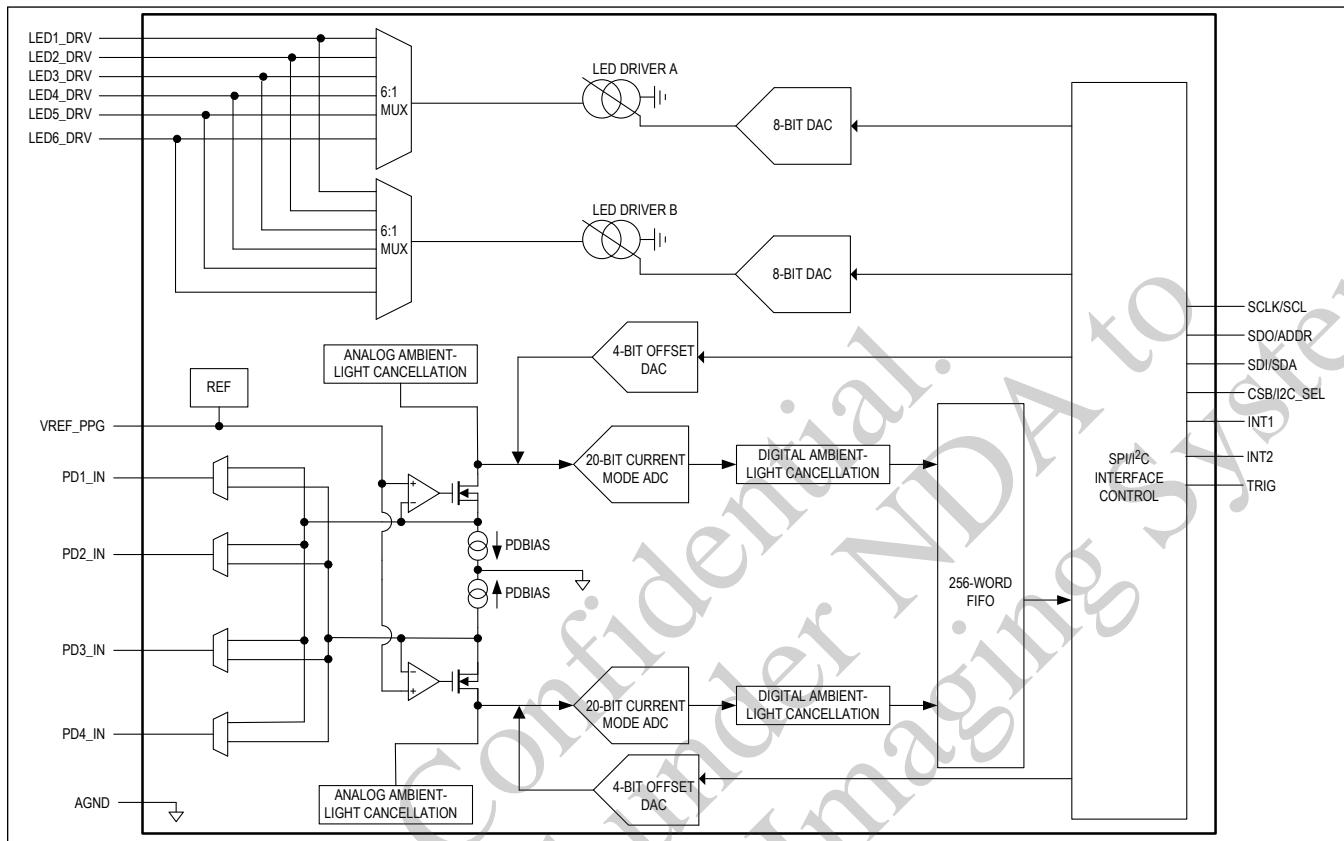


Figure 16. PPG Detailed Block Diagram

Optical Transmitter

The PPG block in MAX86178 has two independent precision LED current drivers that are connected to six LED-driver pins through two 6×1 muxes. Two LED-current DACs modulate LED pulses for a variety of optical measurements. The two LED-current DACs have 8-bit dynamic range with four programmable full-scale range settings of 32mA, 64mA, 96mA, and 128mA (typ). The configuration of the LED drivers can be uniquely set for each measurement. The MEASx_Selects registers (see the Register Map section) define how each LED driver is connected for that particular measurement. Thus, the configuration of the LED drivers can be uniquely set for each measurement and each measurement can drive one or both LED drivers.

Table 8. LED Driver and LED Mux Configuration

MEASx_DRV_A/MEASx_DRV_B	LEDn_DRV PIN CONNECTED TO LED DRIVER
0	LED1_DRV
1	LED2_DRV
2	LED3_DRV
3	LED4_DRV
4	LED5_DRV
5	LED6_DRV

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This configuration of LED driver and LED mux is highly flexible, allowing for not only any combination of the six LED-driver pins to be used at any one time, but also allows for any pin to sink up to 256mA by combining both drivers to generate a higher output current. [Figure 17](#) shows how the two LED drivers are connected to the six LED driver pins.

Both LED drivers are low-dropout current sources allowing for low-noise and power-supply independent LED currents to be sourced with minimal voltage overhead; thereby, minimizing LED power consumption. Four full-scale range settings are provided to allow for the optimization of LED driver noise, and dropout voltage on the LEDn_DRV pins. [Table 9](#) illustrates this trade-off.

Table 9. LED Driver Full-Scale Range Trade-Off

FULL-SCALE RANGE (mA)	RECOMMENDED MINIMUM V _{LEDn_DRV} (mV)	PEAK DC SNR (dB)
32	300	84
64	500	88
96	700	90
128	900	91

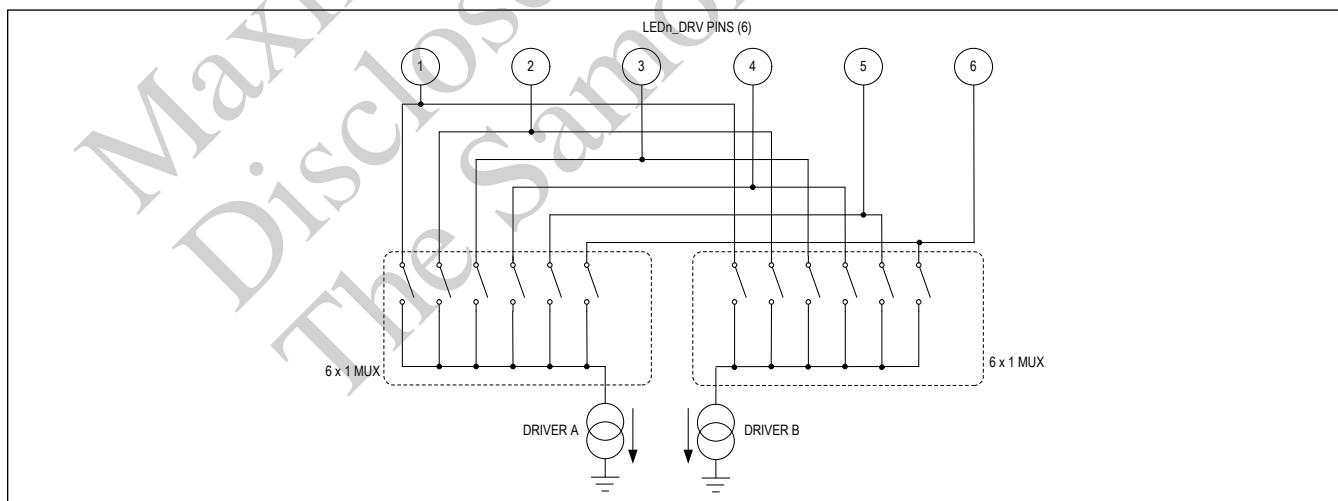
The LED on-time is the sum of the receiver integration time selected in MEASx_TINT, and the LED settling time selected in MEASx_LED_SETLNG. The duty cycle is set by the ratio of the LED on-time and the frame period. The average LED supply current is calculated as the product of the programmed LED current and the duty cycle.

The voltage on V_{LED} depends on the forward voltage (V_F) of the LEDs driven by the MAX86178. The AFE requires a minimum of 3.1V applied to the V_{LED} pin (see the [Electrical Characteristics](#) table). Additionally, the minimum required V_{LED} voltage in a system is determined by the sum of forward voltage (V_F) of each LED at maximum LED current and LED driver headroom voltage (V_{LEDn_DRV} as shown in [Table 9](#)).

The V_{LED} voltage must be above this minimum to avoid compression, and allow for enough headroom to supply the LED drive current as needed; otherwise, the I_{LED} can be reduced and become more sensitive to V_{LED} supply changes. The voltage on LEDn_DRV pins can be measured during an exposure to ensure the minimum headroom voltage is maintained during each LED exposure (LED on-time). The minimum V_{LED} can be simply calculated by using the formulas below:

$$V_{LED} \geq 3.1V \text{ and } V_{LED} \geq V_F + V_{LEDn_DRV}$$

where, V_F is a function of maximum LED current for the system.

**Figure 17. LED Drivers****PRELIMINARY**

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The optical path in the PPG block of MAX86178 is composed of a front-end photodiode biasing circuit with an analog ambient-light cancellation (ALC) sample and hold circuit that nulls the ambient-light photodiode current at the input of the ADC. This front-end biasing circuit is followed by a current integrating, continuous-time sigma-delta ADC with a proprietary discrete time filter. This discrete time filter uses multiple dark and exposure samples to generate an accurate 19-bit effective exposure output signal with excellent low- and high-frequency ambient-light rejection.

The MAX86178 PPG block incorporates dual signal paths and has four photodiode input pins. Each photodiode input is either connected to one of the two PPG signal paths or is left open by configuring MEASx_PDy_SEL ($x = 1$ to 6, $y = 1$ to 4) as needed, so that input to the two PPG ADCs is received simultaneously. For applications requiring only one optical signal path to be active (for example, lower power consumption), either one of the two channels is powered down by setting PPG1_PWRDN or PPG2_PWRDN (register 0x10) to 1. In this way, the MAX86178 is used in a single-channel configuration. By default, the MAX86178 PPG has dual-channel configuration.

Each signal path supports four full-scale range settings of 4 μ A, 8 μ A, 16 μ A, and 32 μ A set in the MEASx_PPGy_ADC_RGE ($x = 1$ to 6, $y = 1, 2$) field in each of the measurement configurations block. Also supported are four options for integration time, which effectively modulate the channel bandwidth, allowing for a trade-off between LED power consumption and PPG signal quality.

Each PPG signal path also incorporates a 4-bit offset DAC for extending the optical dynamic range by sourcing some of the exposure current to the offset DAC. The current offset to DAC is selected in the MEASx_PPGy_DACOFF ($x = 1$ to 6, $y = 1, 2$) register bit field. This feature is especially useful under certain conditions that occur when attempting to limit the exposure ADC counts, for example, when avoiding saturation while increasing the exposure-signal perfusion index. The optical paths also support multiple photodiode and LED settling time settings in order to support flexible multiparameter measurements for different types of photodiode/LED wavelength combinations.

Most significantly, each signal path supports up to six unique combinations of the above configurations as needed. This allows a single optical AFE to support multiple optical measurements in a compact, energy-efficient design.

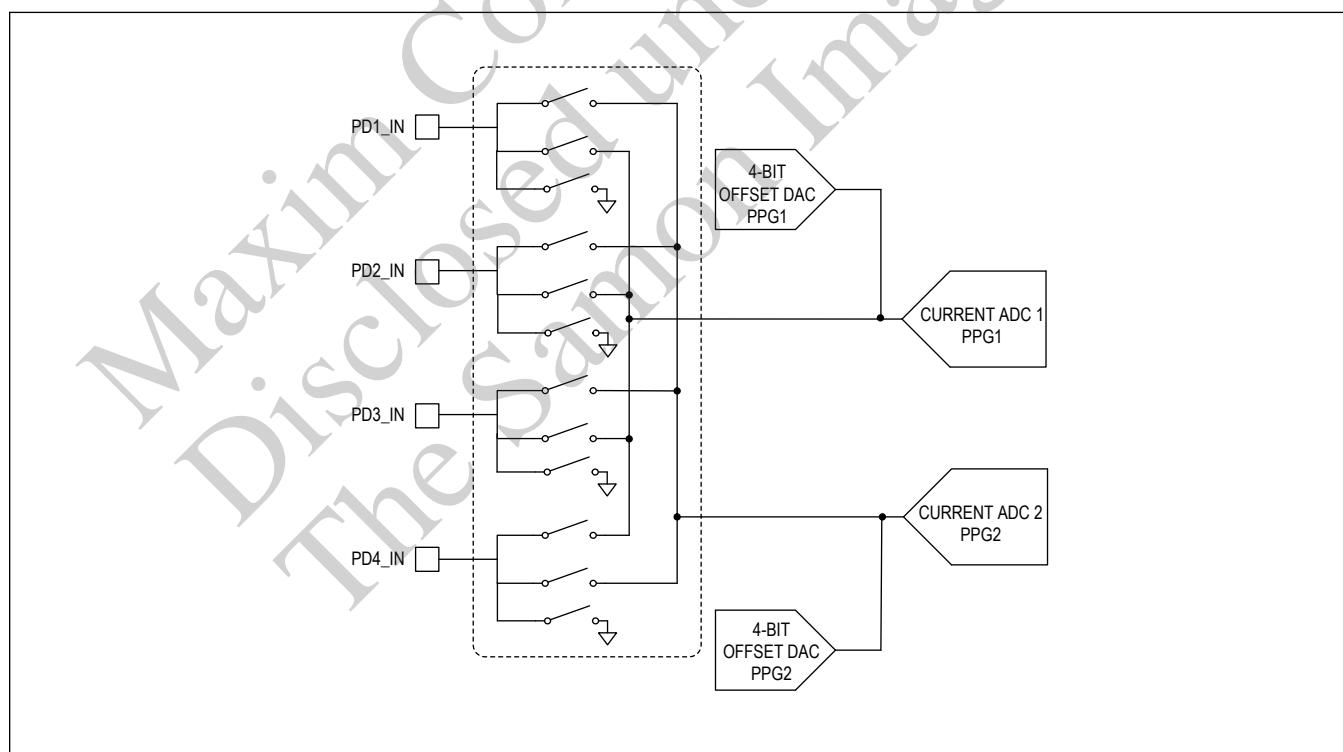


Figure 18. Optical Receive Channel

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There are three photodiode biasing options in MAX86178 PPG to support a large range of photodiode capacitance. Each photodiode input can have a separate bias setting; thereby, allowing for different photodiodes to be used. The PDm_BIAS (register 0x24) settings adjust the PDm_IN bias point impedance to ensure that each photodiode settles rapidly enough to support the sample timing.

Table 10. Recommended PD Bias Settings Based on the Photodiode Capacitance

PDm_BIAS (m = 1 to 4)	PHOTODIODE CAPACITANCE (pF)
0	Do not use
1	0 to 125
2	125 to 250
3	250 to 500

The PDm_BIAS impacts the dark current noise of the MAX86178. The relationship between PDm_BIAS and noise with increasing photodiode capacitance is shown in [Table 11](#). Because of the increased noise with a higher PDm_BIAS setting, the lowest recommended PDm_BIAS value should be used for any given photodiode capacitance.

Table 11. Dark Noise vs PD Bias Setting and Integration Time

PDm_BIAS	DARK NOISE (pA _{RMS}) MEASx_TINT = 14.6μs	DARK NOISE (pA _{RMS}) MEASx_TINT = 29.2μs	DARK NOISE (pA _{RMS}) MEASx_TINT = 58.6μs	DARK NOISE (pA _{RMS}) MEASx_TINT = 117.1μs
0x1	380	206	152	104
0x2	512	276	186	131
0x3	590	405	305	220

Measurement Configuration and Timing

A measurement is essentially one combination of LED (or LEDs) and PD (or PDs) that results in an optical measurement. The MAX86178 supports six individual measurements, each of which can be configured independently. Each measurement can be configured by the group of registers named PPG MEASx Setup (x = 1 to 6). These registers set up a number of parameters for each measurement independently as listed below.

- Connection of each of the two LED drivers to one of the six LED driver pins
- Connection of each of the four photodiode inputs to one of the two PPG channels
- Ambient measurement
- LED driver range
- LED drive current for each driver
- LED settling time
- PD settling time
- Number of burst averages
- Ambient rejection scheme (CDM or FDM)
- On-chip decimation filter selection (COI, COI2, or SINC3)
- ADC integration time
- ADC range for each channel
- DAC offset for each channel

In addition, the following parameters are set for all enabled measurements:

- PPG synchronization mode
- Dual-channel or single-channel mode
- Proximity mode
- Number of sample averages
- Bias setting for all PD inputs

A measurement can be configured to pulse one or two LED drivers sequentially at multiple wavelengths as is done in pulse-oximetry measurements or simultaneously to drive multiple LEDs such as is done with heart-rate measurements on the wrist. A measurement is also configurable to measure the direct ambient level. If the direct ambient is enabled in a measurement through MEASx_AMB (see the Register Map section), it must be the last measurement in the sequence

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of enabled measurements.

[Figure 19](#) represents one measurement with only one of the LED drivers active. No averaging is used. As seen in [Figure 19](#) only MEASx_DRVA is pulsing during the exposure time. In this mode, each driver pulse results in a single optical-sampled value for each PD input to be stored in the FIFO. For example, in a single-channel configuration, only one ADC data sample is stored in the FIFO for each driver pulse, but for a dual-channel configuration, two ADC data samples are stored in the FIFO for each driver pulse. This configuration can be used when heart rate is being measured with a single LED.

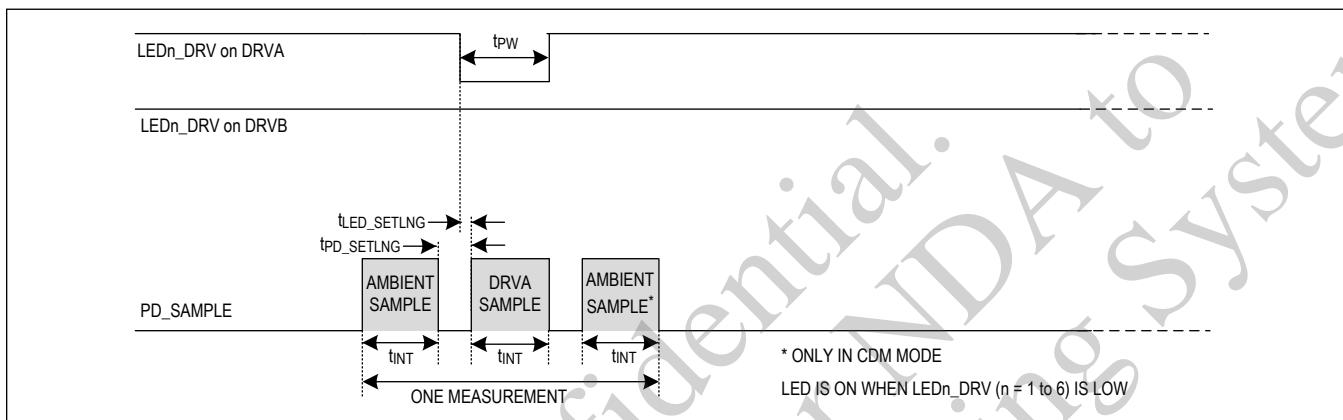


Figure 19. Measurement with One LED Driver

Frame

A frame is a combination of one (min) to six (max) measurements configured in MEASx_EN ($x = 1$ to 6). The frame rate defines how frequently a frame is repeated and is expressed in units of frames per second (fps). For details on the PPG frame-rate configuration, see the [PPG Frame Rate](#) section.

Any combination of measurements can be enabled, but measurements are done in a numerical order inside a frame. For example, it is valid to enable MEAS1, MEAS2, and MEAS5 while MEAS3 and MEAS4 are skipped. But if a measurement of direct ambient is configured, then this measurement must be configured as the last measurement in the frame.

[Figure 20](#) represents the timing diagram for one measurement in each frame. This measurement has only one LED driver pulsing. See [Figure 19](#) for details about what comprises M1.

[Figure 21](#) illustrates the timing for six measurements in each frame. Each measurement can be configured independently using the MEASx Selects Registers (see the Register Map section). Alternatively, all measurements share the configuration of M1 by setting MEAS1_CONFIG_SEL [0] (0x22) to 1. Each measurement is comprised of ambient (LED off) sample(s) as well as exposure (LED on) sample as shown in [Figure 19](#).

[Figure 22](#) illustrates the timing with burst averaging in each frame with MEAS3 configured to have an on-chip burst average of 2 (MEAS3_AVER[2:0](0x41) = 0x1). The result of MEAS3 in each frame is only one FIFO data pushed into FIFO. This FIFO data is the average of the two PD samples labeled F1M3a and F1M3b. The burst averaging factor is configured by MEASx_AVER ($x = 1$ to 6) and it is available only with CDM (MEASx_FILT_SEL = 0). The ambient (LED off) samples as well as the exposure samples in case of burst averaging are shown in [Figure 22](#). In this case, the maximum valid frame rate is limited by the burst averaging factor for enabled measurements.

[Figure 23](#) shows timing with sample averaging of 2 in each frame (SMP_AVE[6:4](0x22) = 0x1). Each individual measurement in frame 1 (F1) and frame 2 (F2) is averaged and the result is saved in FIFO as a single sample for each measurement. For example, the sample in FIFO for measurement 1 is $(F1M1 + F2M1) / 2$. Each enable measurement within every frame has its ambient sample(s) and exposure sample as detailed in [Figure 19](#). When using sample averaging, the data output rate is reduced by the frame rate / sample averaging factor. Therefore, sample averaging also limits the bandwidth of the PPG data and helps improve SNR of the AFE.

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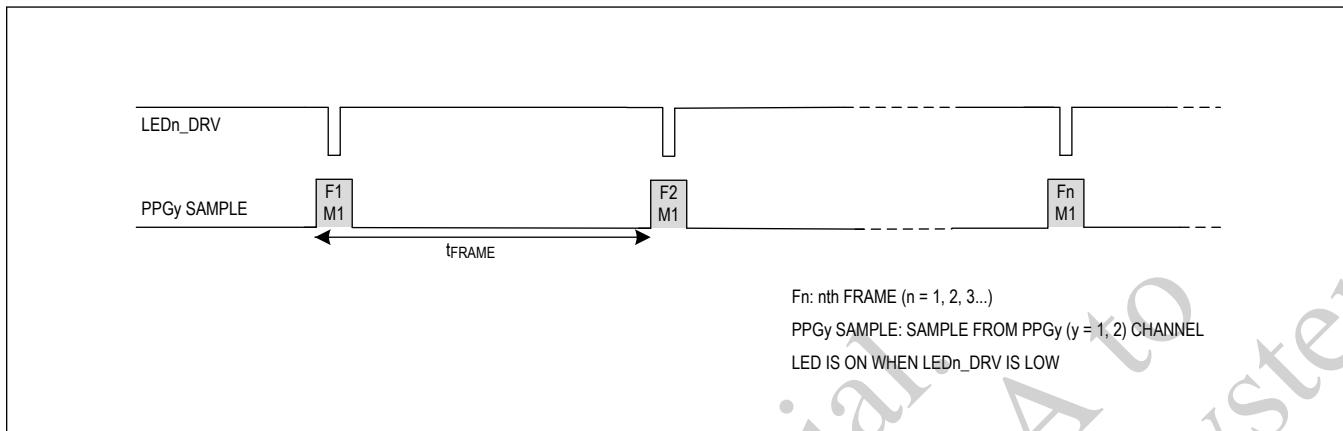


Figure 20. Frame with One Measurement

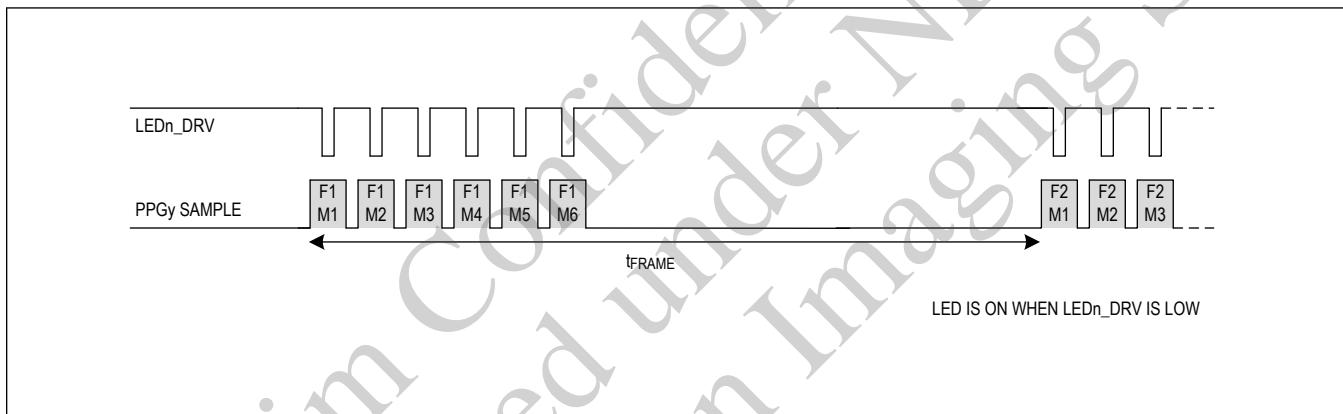


Figure 21. Frame with Six Measurements

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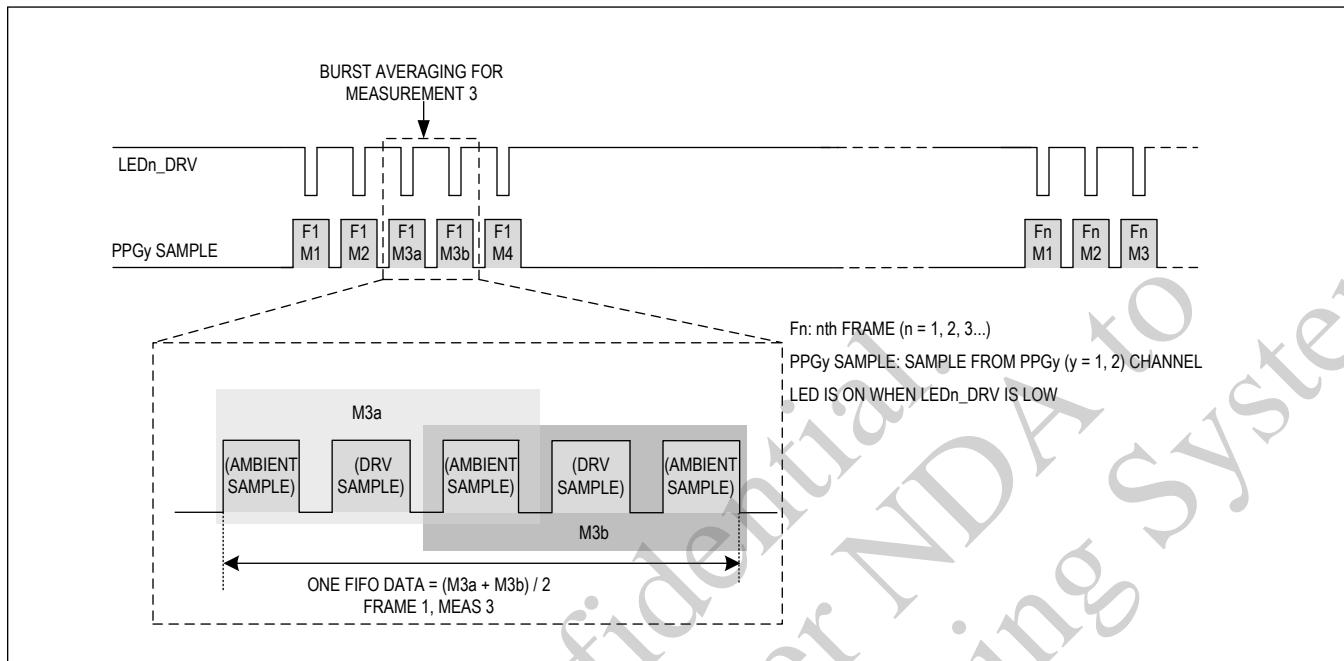


Figure 22. Frame with Burst Averaging

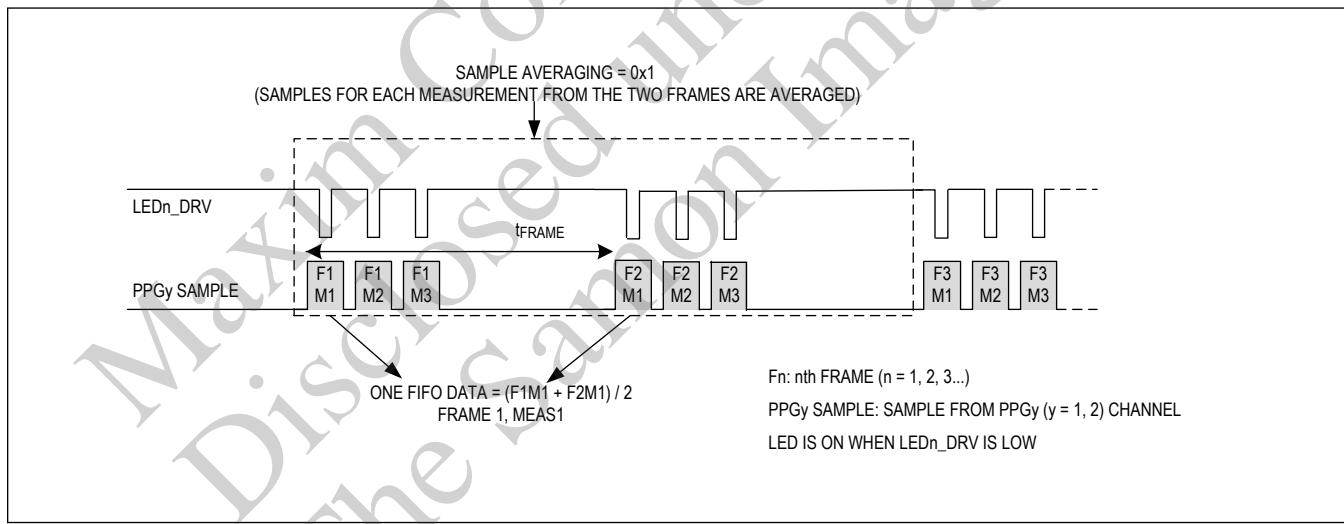


Figure 23. Frame with Sample Averaging

Ambient Rejection

The MAX86178 implements ambient-light cancellation in two steps, a coarse cancellation and a fine cancellation. Each PPG channel has its own dedicated ambient-light cancellation circuits. Also, each MEASx has its own ambient-light cancellation configuration. The coarse cancellation is in the analog domain. It is enabled by default and can be disabled by setting the ALC_DISABLE[4](0x22) to 1. The fine cancellation is a digital cancellation scheme and is configured as either central difference method (CDM) or forward difference method (FDM) using the MEASx_FILT_SEL bit.

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ALC is an analog sample and hold scheme, which cancels up to 200 μ A of DC photodiode current. Any drift or residual from ALC is cancelled by CDM/FDM cancellation.

One CDM sample is comprised of 3 ADC conversions, with 2 ambient and 1 exposure conversion. One FDM sample is comprised of 2 ADC conversions, with 1 ambient only and 1 exposure conversion.

The ambient and exposure samples are used for digital cancellation of any residual error (from ALC) or drift (in ambient signal). The final computed value is the effective exposure signal, which is stored in the FIFO.

See [Figure 24](#) for the timing diagram for CDM and [Figure 25](#) for the timing diagram for FDM.

The MAX86178 features various decimation filtering options for the delta-sigma PPG ADC. By default, the MAX86178 uses a second-order decimation filter (COI2). Alternatively, the user can select a third-order decimation filter (COI3). The second-order COI2 filter has a narrower noise-equivalent bandwidth as compared to the third-order COI3, and therefore, results in lower-noise performance. The selection for either COI2 or COI3 is done by programming MEASx_FILT2_SEL for each individual measurement. However, the second order decimation filter COI2 is available only with the longest integration time setting (MEASx_TINT = 0x3). Using COI2 instead of COI3 for the longest integration-time setting provides about 1 dB higher SNR for PPG results. Both the COI2 and COI3 filters have a non-symmetrical impulse response with no ripple in the pass band or the stop band. A third option is to use the SINC3 decimation filter for the delta-sigma PPG ADC, which is enabled for each measurement individually by setting MEASx_SINC3_SEL. This filter provides improved high-frequency roll-off, 60dB/dec roll-off for out of band frequencies, that significantly improves the high-frequency ambient-light rejection. In comparison, the COI2 and COI3 filters provide only about 20dB/dec roll-off at high frequencies but provide excellent quantization performance.

Ambient-light cancellation in low-frequency ambient light improves when using a burst average by setting MEASx_AVER $\geq 0x2$.

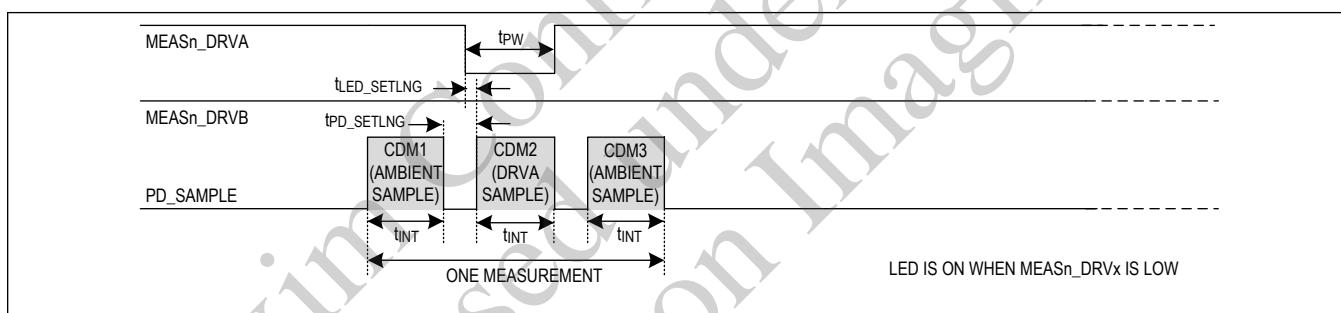


Figure 24. Central Difference Method (CDM)

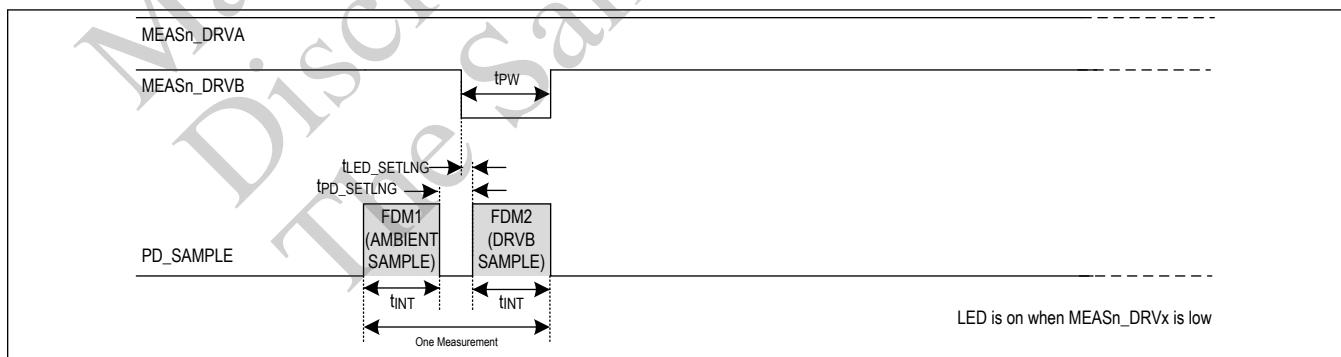


Figure 25. Forward Difference Method (FDM)

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MAX86178**Ultra-Low-Power, Clinical-Grade
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The MAX86178 includes a threshold-detect function that enables users to detect ADC counts higher than a specified range or lower than a specified range.

The threshold-detect function is used in proximity mode (see the [Automatic Proximity Detect Mode](#) section) to reduce energy consumption and extend battery life when the sensor is not in contact with skin. There are two separate instances of threshold-detect functions available in MAX86178, Threshold1 and Threshold2. Both are disabled by default.

The threshold-detect function is enabled by selecting a measurement in THRESHx_MEAS(x = 1, 2) in register 0x70. The threshold-detect function is set up for either PPG1 or PPG2 by configuring THRESHx_PPG_SEL (x = 1, 2) in register 0x71. In order to configure the threshold-detect function, both an upper limit and a lower limit must be set. These can be configured in the PPG Threshold Interrupts registers (0x72 to 0x75).

In addition, two features are available to make the threshold-detect function more adaptable for various system and application requirements. These are time hysteresis and level hysteresis and are configurable through the TIME_HYST[4:3] and LEVEL_HYST[2:0] in register 0x71. Time hysteresis sets the number of consecutive samples that must be outside the limits defined by THRESHOLDx_UPPER and THRESHOLDx_LOWER in order to assert the threshold interrupt. Level hysteresis defines the sample variation around THRESHOLDx_UPPER and THRESHOLDx_LOWER. This value is in ADC counts and is applied at $\pm 0.5 \times$ LEVEL_HYST around THREHSOLDx_UPPER as well as $\pm 0.5 \times$ LEVEL_HYST around THRESHOLDx_LOWER. Specifically, in order for a threshold interrupt to be asserted, a sample must either transition above the THRESHOLDx_UPPER + 0.5 x LEVEL_HYST and stay above THRESHOLDx_UPPER - 0.5 x LEVEL_HYST for the number of samples defined in TIME_HYST or transition below THRESHOLDx_LOWER - 0.5 x LEVEL_HYST and stay below THRESHOLDx_LOWER + 0.5 x LEVEL_HYST for the number of samples defined in TIME_HYST as shown in [Figure 26](#).

If a threshold-detect function instance is enabled, the corresponding THRESHx_HILO interrupt bit (register 0x00) is asserted and threshold mode is activated when the ADC counts of the assigned measurement on the specified PPG channel drop below the lower limit, or exceed the upper limit (in consideration with the LEVEL_HYST and TIME_HYST settings). The upper threshold check is disabled by setting THRESHx_UPPER (0x72, 0x74) to 0xFF. The PPG ADC reading, if negative, is clipped to 0x00000 before comparing with the threshold limits. Therefore, programming THRESHOLDx_LOWER to 0x00 effectively disables the lower threshold check.

The threshold-detect function enables low power consumption while in automatic proximity detect mode. Alternatively, the LED configuration during the threshold-detect active mode is determined by the firmware settings as needed for each application. The lower settings of the LED current, ADC integration time, and frame rate result in reducing power consumption during situations when there is no reflective returned signal.

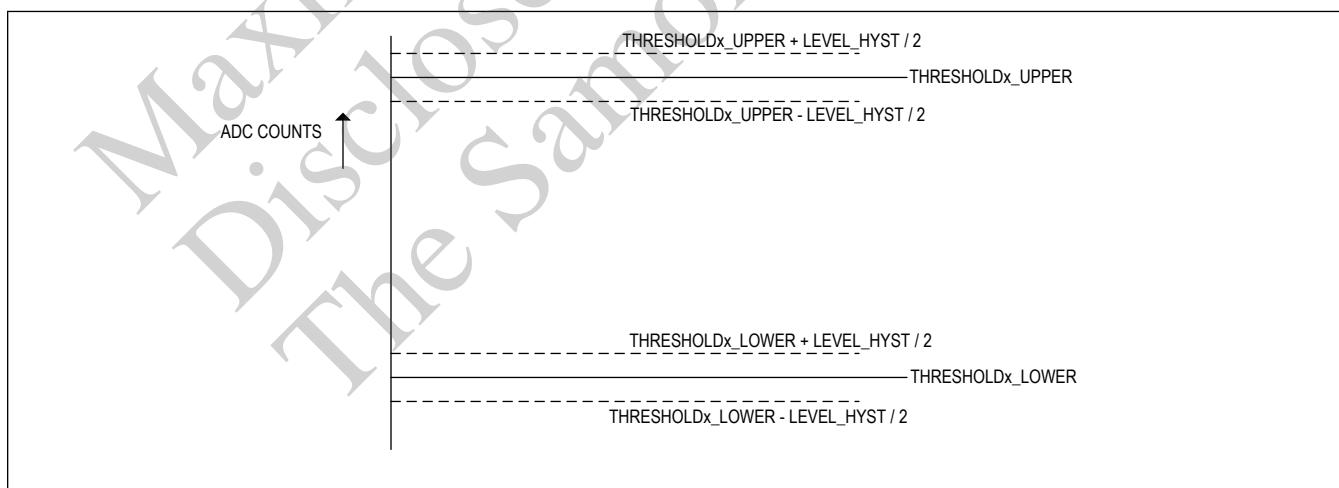


Figure 26. Threshold Limits with LEVEL_HYST

MAX86178**Ultra-Low-Power, Clinical-Grade
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The MAX86178 includes a proximity detect mode that switches the device automatically between proximity-detect mode (PROX mode) and normal mode. Using the threshold-detect function (see the [Threshold-Detect Function](#) section), the proximity mode significantly reduces energy consumption; thereby, extending battery life when the sensor is not in contact with skin.

When the PROX_AUTO[3](0x23) is set to 1, PROX mode is enabled. In this mode, PPG measurement 6 is reserved for proximity function and is automatically enabled even if MEAS6_EN[5](0x20) is programmed to 0. Threshold1 is used for proximity detect, but THRESH1_MEAS_SEL[3:0](0x70) is ignored. Instead, measurement 6 is considered for this threshold instance. The PROX mode is implemented on the PPG channel selected in THRESH1_PPG_SEL[6](0x71).

The device enters PROX mode when the measurement 6 ADC reading is below the threshold defined by THRESHOLD1_LOWER[7:0](0x73). Otherwise, it is in normal mode. THRESHOLD1_UPPER[7:0](0x72) is not used. The device switches between PROX mode and normal mode automatically. In PROX mode, the frame rate automatically changes to 8fps, and only measurement 6 is selected for ADC conversions. While in normal mode, measurement 6 and all the enabled measurements 1 to 5 are selected for ADC conversions, and the frame rate is configured by FR_CLK_DIV[14:0](0x28, 0x29). In order to reduce power consumption while in PROX mode, the MEAS6 LED drive current should be as low as possible. The LED current for MEAS6 is configured through MEAS6_DRVA_PA[7:0](0x5E) and MEAS6_DRVB_PA[7:0](0x5F).

If THRESH1_HILO interrupt is enabled using THRESH1_HILO_EN1[1](0xC0) or THRESH1_HILO_EN2[1](0xC5), an interrupt is asserted on the INT1 or INT2 pin, respectively, when the part switches from normal mode to PROX mode and also for each ADC conversion while in PROX mode. There is no interrupt when the part switches from PROX mode to normal mode.

In order to get an interrupt when switching from PROX mode to normal mode, a second threshold instance is enabled using THRESH2_HILO_EN1[2](0xC0) or THRESH2_HILO_EN2[2](0xC5). THRESHOLD2_UPPER[7:0](0x74) should be programmed to be equal to THRESHOLD1_LOWER[7:0](0x73), and THRESHOLD2_LOWER[7:0](0x75) should be zero. THRESH2_MEAS_SEL[7:4](0x70) should be programmed to select MEAS6. THRESH2_PPG_SEL[7](0x71) should be programmed the same as THRESH1_PPG_SEL[6](0x71). When configured this way, Threshold 2 generates an interrupt when switching from PROX mode to normal mode and does not generate an interrupt when the part switches from normal mode to PROX mode.

To reduce the number of interrupts, THRESH1_HILO interrupt should be enabled when the part is in normal mode, and THRESH2_HILO should be enabled when the part is in PROX mode. If interrupts are not needed for detecting switching between PROX and normal modes, Threshold 2 Interrupt registers need not be programmed.

False detection of PROX mode and normal mode can be avoided by configuring TIME_HYST[4:3] and LEVEL_HYST[2:0] in register 0x71 as desired.

See the [Threshold-Detect Function](#) section for more details on threshold interrupts.

ECG

The ECG channel is a complete signal chain with all of the critical features necessary to collect high-quality ECG data such as flexible gain, critical filtering, low noise, high input impedance, and multiple lead-biasing options. Additional features, such as fast recovery, AC and DC lead-off detection, ultra-low-power lead-on detection, and right leg drive, enable robust operation in demanding applications such as wrist-worn devices with dry electrodes. The analog-signal chain drives an 18-bit sigma-delta ADC with a wide range of user-selected output sample rates. The following sections describe each of these features in detail and provide the information needed to implement them.

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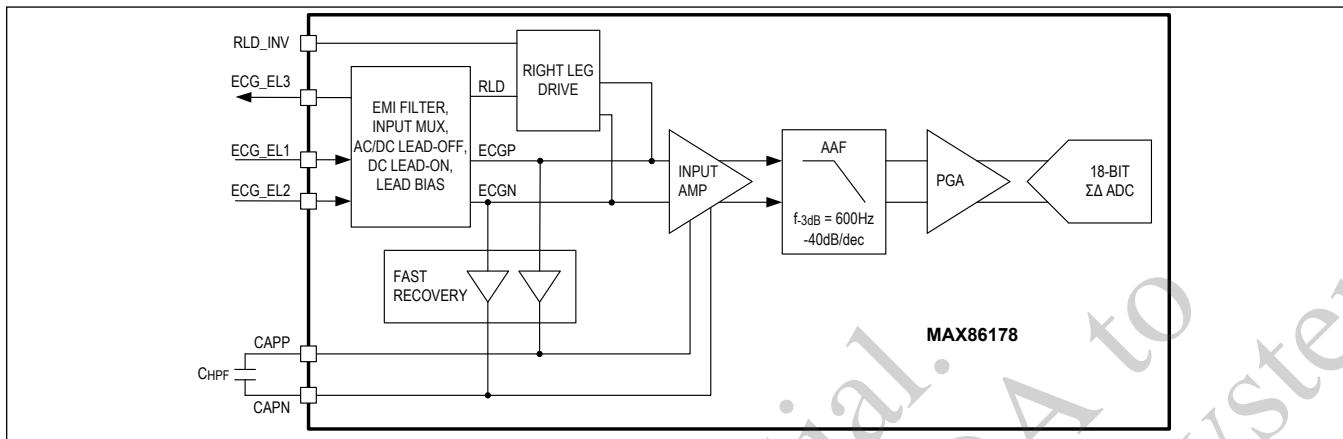


Figure 27. Simplified ECG Channel Signal Chain

Analog-Signal Chain and ADC

The ECG-signal chain shown in [Figure 27](#) consists of an input amplifier with high-pass filtering and fast recovery, an anti-aliasing filter (AAF), a programmable gain amplifier (PGA), and a delta-sigma ADC.

The input amplifier (INA) has a wide input range of 150mV to 1.35V to allow for large electrode offsets and changes in body bias, as well as offering programmable gain. The DC bias on ECGP and ECGN as well as low frequency signals below the corner frequency of the analog HPF are removed by the INA. The AC portion of the signal occupying frequencies above the corner frequency is amplified and passed to the PGA and ADC. This differential AC signal, as shown in [Figure 28](#) can be as large as 200mV_{P-P}. The AC signal is amplified further by the PGA and then passed to the ADC, which has a full-scale range of 2V_{P-P}. To avoid saturating the ADC, the combined gain of the INA and PGA should be chosen such that the AC input signal amplitude is less than $2V_{P-P} / (\text{INA gain} \times \text{PGA gain})$. The INA gain is set by ECG_INA_GAIN[1:0](0x81) and ECG_INA_RGE[3:2](0x81) and ranges from 2.5V/V to 60V/V. The PGA gain is set by ECG_PGA_GAIN[6:4](0x81) and ranges from 1V/V to 16V/V. Both gain settings are located in the ECG Configuration 2 (0x81) register.

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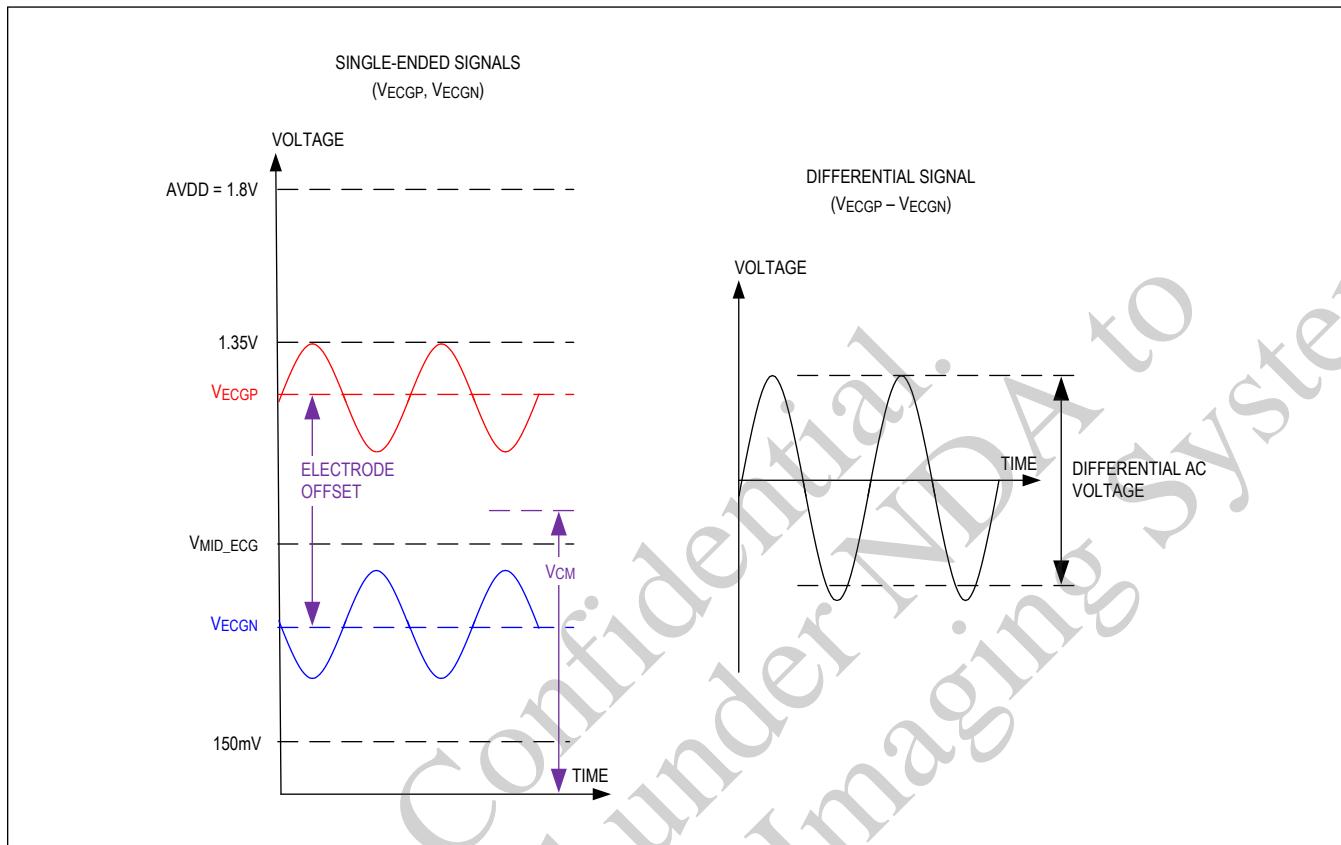


Figure 28. ECG Channel Input Ranges

The INA utilizes an external capacitor (C_{HPF}) connected between CAPP and CAPN to accomplish built-in high-pass filtering, as shown in [Figure 29](#). The INA buffers the voltage on ECGP and ECGN onto CAPP and CAPN through buffers with $200\text{k}\Omega$ each by default, for a combined resistance of $400\text{k}\Omega$ (R_{HPF}) to form a low-pass filtered voltage across C_{HPF} . The INA then subtracts the voltage on C_{HPF} from the input voltage and outputs the amplified difference. The end result is a high-pass filter with the corner frequency set by the value of C_{HPF} . To guarantee that the corner frequency is lower than the desired value across the operating temperature range, the minimum value of R_{HPF} ($240\text{k}\Omega$ min) and the minimum capacitor tolerance of C_{HPF} must be considered in the corner frequency calculation:

$$f_{-3dB} = 1 / (2 \times \pi \times R_{HPF} \times C_{HPF})$$

[Table 12](#) shows the minimum effective capacitance needed to guarantee common corner frequencies. The resistance of R_{HPF} can either be fixed at $400\text{k}\Omega$ (default) or vary with the input amplifier range (see ECG_IMP_HI[3](0x82)).

Table 12. ECG Analog HPF Corner Frequency Selection with $R_{HPF} = 400\text{k}\Omega$

HPF CORNER FREQUENCY (Hz)	MINIMUM EFFECTIVE CAPACITANCE (μF)	STANDARD 10% CAPACITOR VALUE (μF)
≤ 5	0.13	0.15
≤ 0.67	0.99	1.1
≤ 0.5	1.3	1.5
≤ 0.05	13	15

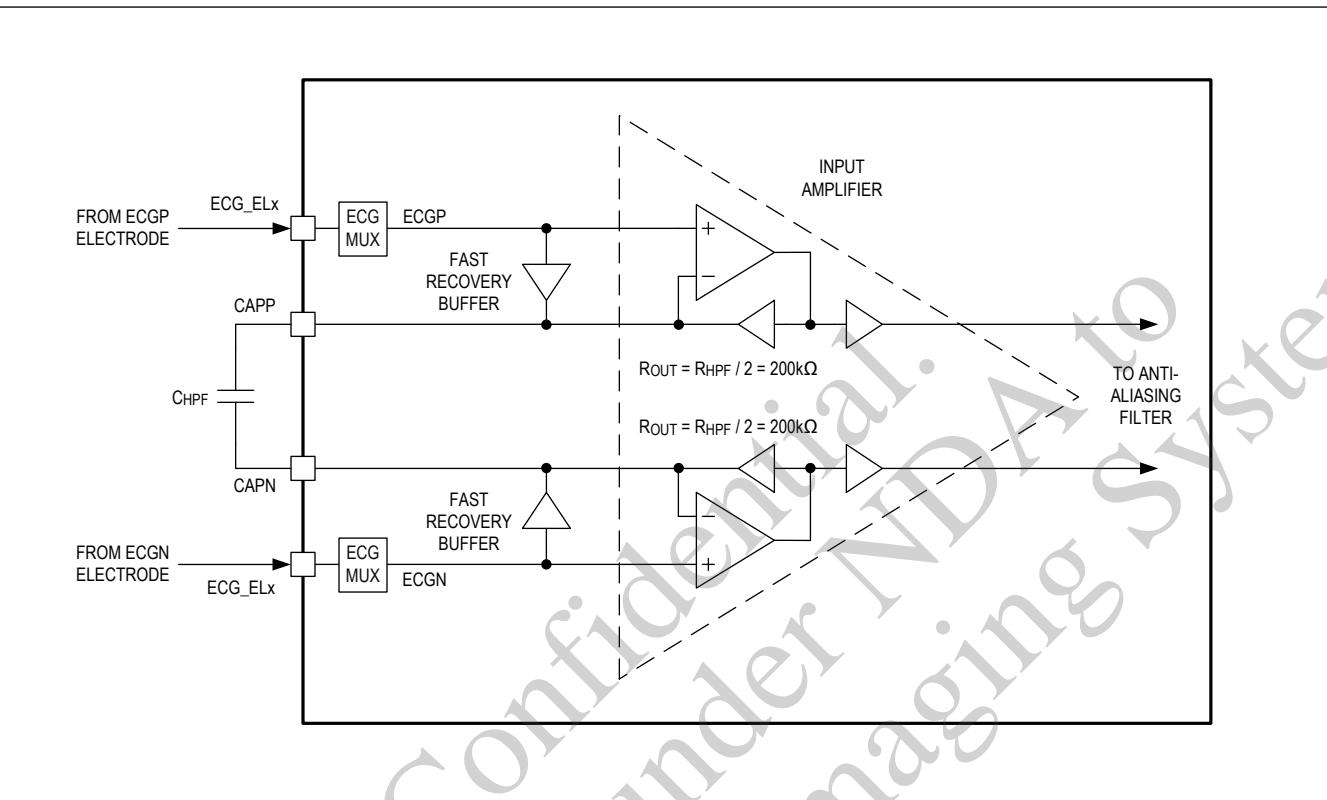
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Figure 29. Input Amplifier Detailed Block Diagram

Following the input amplifier is a 2-pole active anti-aliasing filter with a 600Hz corner frequency that provides 57dB of attenuation at half the modulator sampling rate (approximately 16kHz). Following the PGA is a delta-sigma ADC with an input sampling rate set by the ECG ADC sample clock (32.0kHz or 32.768kHz (see the [Timing Subsystem](#) section). This input sampling rate is divided by the value set by ECG_DEC_RATE[2:0](0x80) to set the ECG sample rate between 62.5sps and 2048sps. The decimation filter has a SINC3 CIC architecture, which ensures adequate attenuation above the Nyquist frequency of the digitized signal, but also reduces the bandwidth of the pass-band to approximately $0.26 \times SR_{ECG}$. At higher sample rates, the INA, PGA, and AAF also limit the ECH channel bandwidth. [Table 13](#) shows the -1dB and -3dB bandwidths at common sample rates (see [Table 3](#)).

Table 13. ECG Channel Bandwidth

SAMPLE RATE (sps)	-1dB BANDWIDTH (Hz)	-3dB BANDWIDTH (Hz)
128	19	33
200	30	52
204.8	31	53
250	38	65
256	38	66
500	74	128
512	76	131
1024	144	250
2048	246	432

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Fast Recovery Modes

The input amplifier (INA) has the ability to rapidly recover from an excessive overdrive event such as a defibrillation pulse, high-voltage external pacing, and electro-surgery interference, or a rapid change in electrode offset due to motion. These events create a large change in the differential offset between ECGP and ECGN, causing the input amplifier or ADC to saturate. The analog HPF would eventually converge and bring the offset voltage back into range, but this can take a long time. Fast recovery greatly speeds up this process by enabling strong buffers to rapidly charge C_{HPF}, effectively raising the HPF corner frequency momentarily. These buffers are shown in [Figure 29](#).

Fast recovery can be activated by three methods:

- Analog automatic mode:** An analog circuit detects if the INA is saturated, and briefly enables the fast recovery buffers.
- Digital automatic mode:** A digital function detects if the ADC counts are outside of a programmable threshold, and momentarily enables the fast recover buffers.
- Manual mode:** The fast recovery buffers are controlled manually by the host microcontroller.

Analog automatic mode is enabled by ECG_AUTO_REC[2](0x82) and monitors the INA for saturation, which occurs when the offset voltage changes rapidly. If the INA is saturated for more than approximately 2ms, the fast recovery buffers are enabled and remain active for approximately 32ms. After the buffers are disabled, there is a lockout period of approximately 96ms, after which saturation monitoring resumes. ECG samples taken while this mode is triggered are not marked with the fast recovery flag.

Digital automatic mode is enabled by setting EN_ECG_FAST_REC[7:6](0x83) to 0x2, and compares the ECG ADC counts to the symmetrical threshold set by ECG_FAST_REC_THRESHOLD[5:0](0x83). If the ADC counts are outside of the threshold for more than approximately 125ms, the fast recovery buffers are enabled and remain active for approximately 500ms. This behavior is shown in [Figure 30](#). ECG samples taken while this mode is triggered are marked with the fast recovery flag (see the [FIFO Description](#) section).

In manual mode, the fast recovery buffers are enabled by setting EC_ECG_FAST_REC to 0x1, and disabled by setting it to 0x0. This mode allows the host microcontroller to implement custom fast-recovery logic, such as modified time durations or rising and falling thresholds. For example, the host could monitor the ADC counts and activate fast recovery if the counts saturate (e.g., $> \pm 95\%$ FSR), and keep fast recovery enabled until the counts fall to within a certain threshold (e.g., $< \pm 10\%$ FSR). This logic scheme would allow for much shorter fast recovery times in response to minor disturbances. ECG samples taken while this mode is active are marked with the fast recovery flag (see the [FIFO Description](#) section).

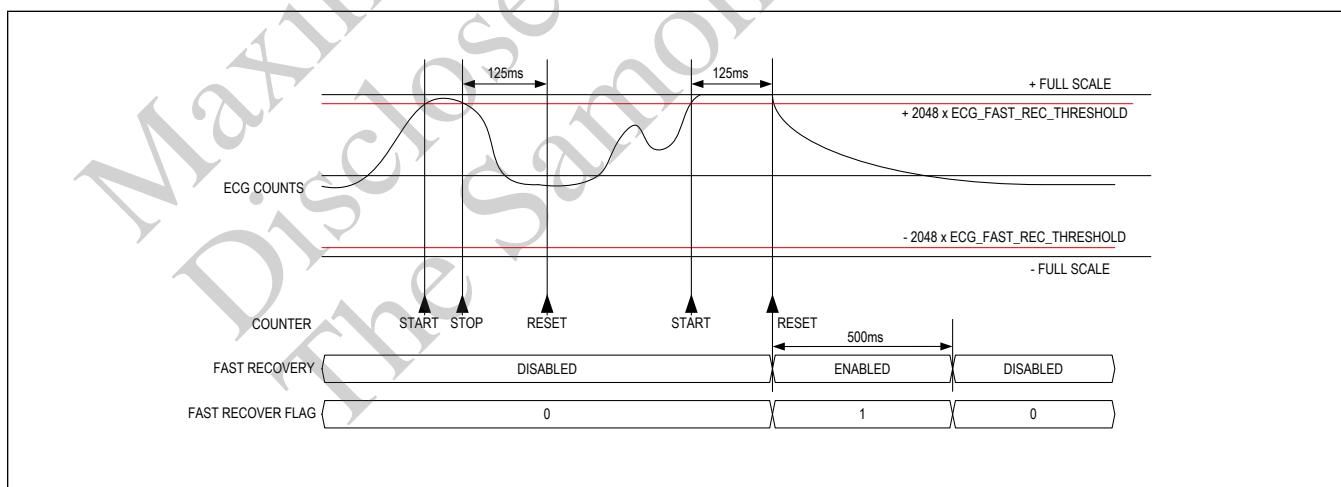


Figure 30. Digital Automatic Fast-Recovery Behavior

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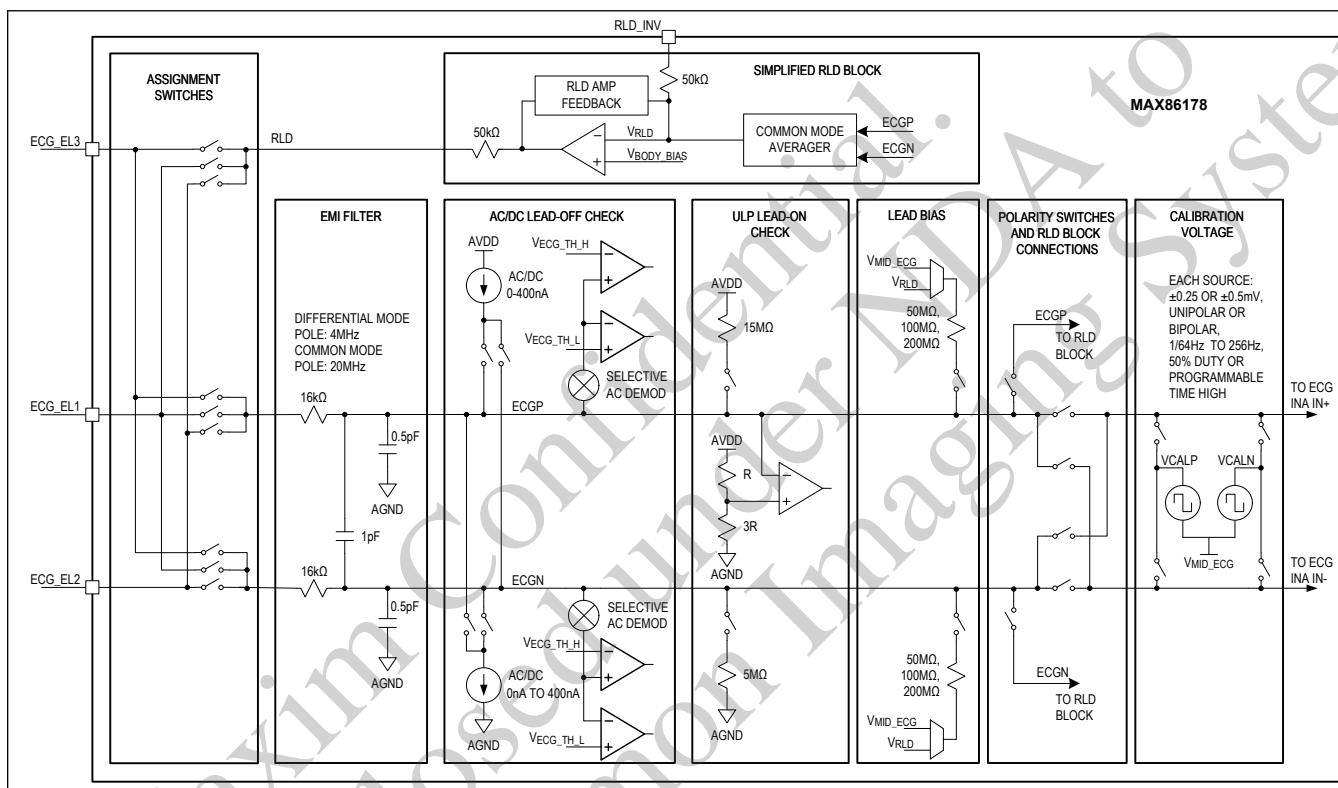
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Figure 31. ECG Channel Input MUX

ECG EMI Filtering

The EMI filter on the ECGP and ECGN inputs consists of 16kΩ resistors connected to ECGP and ECGN followed by a 1pF differential mode capacitor and 0.5pF common-mode capacitors. These form a single-pole, low-pass, differential-and common-mode filter with the differential-mode pole located at approximately 4MHz and the common-mode pole located at approximately 20MHz. Additional external EMI filters are not recommended for applications with dry electrodes in order to maintain high input impedance and common-mode rejection ratio, which helps mitigate the impact of electrode-impedance mismatch. With lower input impedance and CMRR, the electrode impedance mismatch translates into additional common-mode-to-differential-mode voltage conversions. Applications with wet electrodes can be used with external EMI filters with high precision components to minimize electrode impedance mismatch. In this case, the differential-mode pole can be set as low as the desired signal bandwidth, and the common-mode pole should be set at least a decade below the AM radio band (535kHz).

The ECG_ELx pins have ESD protection compliance with 2kV HBM. For IEC ESD compliance, external ESD diodes must be added (see [Typical Applications Circuits](#)).

MAX86178**Ultra-Low-Power, Clinical-Grade
Vital-Sign AFE****PRELIMINARY****ECG DC Lead-On Detection**

The MAX86178 features an ultra-low powered (ULP) lead-on detection circuit for the ECG electrodes. The ECG channel must be disabled (ECG_EN[0](0x80) = 0) when the ULP lead-on is enabled.

The ULP lead-on detect circuit operates by pulling ECGN low with a pulldown resistance of $5\text{M}\Omega$ (typ) and pulling ECGP high with a pullup resistance of $15\text{M}\Omega$ (typ). A low-power comparator determines if ECGP is pulled below $0.75 \times \text{AVDD}$ (typ), and asserts the ECG_LON[7](0x04) status bit if ECGP remains below the threshold for at least 128ms. This circuit is shown in [Figure 31](#).

There are several conditions that can pull ECGP below the threshold and trigger a lead-on status:

- The total impedance between ECGP and ECGN is below $40\text{M}\Omega$ (typ) due to both electrodes contacting the body.
- The total impedance between ECGP and AGND is below $45\text{M}\Omega$ (typ) due to the the ECGP electrode contacting a body that is coupled to AGND. For example, if the MAX86178 system is coupled to earth ground through a power or data cable, and the body is also coupled to earth ground, then a low-impedance path could pull the ECGP electrode low.
- The ECGP electrode is contacting the body and has a large half-cell potential. The half-cell potential can push the ECGP voltage below the threshold.

If the ECG_LON interrupt is enabled by ECG_LON_EN1[7](0xC4) or ECG_LON_EN2[7](0xC8), an interrupt is generated to alert the host microcontroller of the lead-on condition. This interrupt allows the microcontroller to sleep when the system is not in use, and only to wake up when the user touches the device electrodes. Upon receiving an interrupt and waking up, the microcontroller should read the ECG_LON status register to determine if a lead-on condition has occurred. Because of the bit clear-on-read behavior, the status register should be read a second time to determine if the lead-on condition persists.

ECG DC Lead-Off Detection

The MAX86178 features DC lead-off detection, which is enabled through the Lead Detect Configuration 1 (0x88) register. DC lead-off detection is used while ECG is active and cannot be used at the same time as AC lead-off detection.

A matching source and sink current is injected into the ECGP and ECGN electrodes. This current, when the electrodes are connected properly, flows through a first electrode-tissue interface, through the body and then through a second electrode-tissue interface. The electrode-tissue interface impedance is dependent on the type of electrode used (wet or dry), as well as the materials of the electrodes. The current flow develops a differential voltage across the two input pins. If one or both electrode-tissue interfaces have poor contact with the body, the current path has much higher impedance and the resulting voltage is large. If the electrodes are properly connected, then this voltage is small. DC lead-off detection can be used to evaluate the viability of both wet and dry electrode tissue interfaces.

The programmable stimulus current magnitudes are programmed using the Lead Detect Configuration 2 (0x89) register. The LOFF_IMAG[4:0] bits in the Lead Detect Configuration 2 register are used to set the nominal current between 0nA and $2.8\mu\text{A}$. More details on setting the DC lead-off current are available in the register description.

There is also a voltage threshold setting that sets the threshold of the comparators and is used to determine whether a DC lead-off condition is encountered. The threshold setting is programmable using the ECG_LOFF_THRESH bit within the Lead Detect Configuration 2 register (0x89). The voltage threshold is centered around VMID_ECG .

When using DC lead-off detection, there are two approaches available for alerting the microcontroller and user if the viability of the electrode tissue interfaces has been compromised: (1) dual comparators indicating if ECGP or ECGN voltages exceeds the programmable high threshold or programmable low threshold; and, (2) utility mode measurements can be used to digitize the voltage drop (the DC lead-off voltage) across the two electrodes and the body impedance (see the [Utility Mode Measurements](#) section).

The dual comparators can be used to generate a hardware interrupt using the Interrupt Enable 4 registers (0xC8, 0xC8) if the DC lead-off voltage exceeds the threshold (i.e., a minimum continuous violation) for 128ms before asserting the ECG_LOFF interrupt flags. See [Figure 32](#) diagram below. There are four bits in the Status 4 (0x03) register, which when asserted indicate a lead-off condition has been detected. ECG_LOFF_PH, ECG_LOFF_PL, ECG_LOFF_NH, and ECG_LOFF_NL all give detailed information of the lead-off condition that has been detected. More details are available in the register map.

When using DC lead-off detection, the BioZ channel ADC can be repurposed to measure a buffered copy of either the differential ($\text{V}_{\text{ECGP}} - \text{V}_{\text{ECGN}}$) voltage or a buffered copy of the ($\text{V}_{\text{CAPP}} - \text{V}_{\text{CAPN}}$) voltage by asserting the

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EN_UTIL_MODE bit in the BioZ Configuration 4 register at address 0xA3. Refer to the [Utility Mode Measurements](#) section for details.

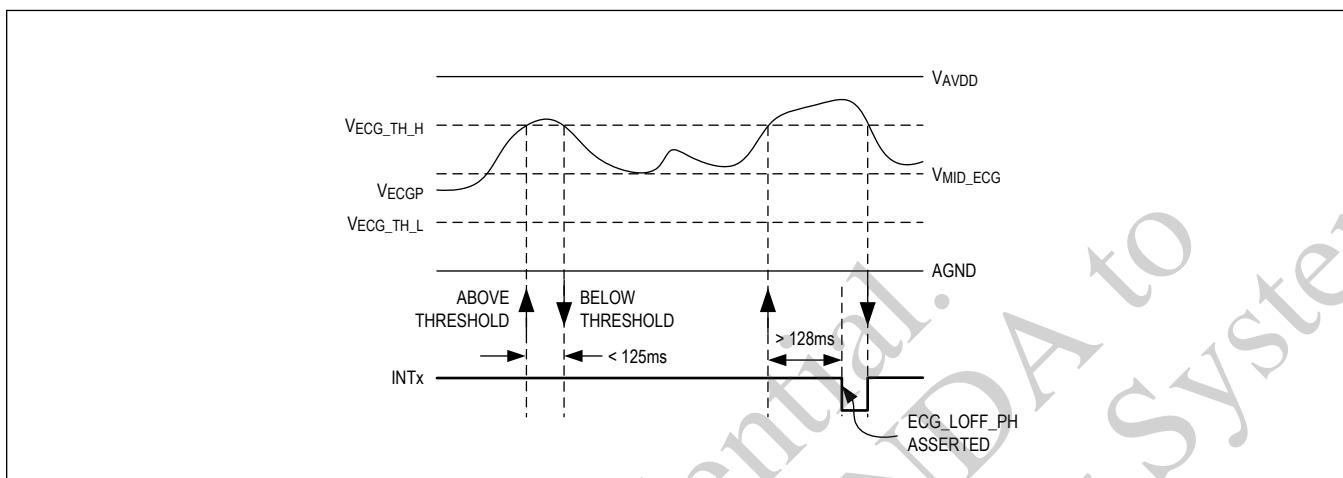


Figure 32. DC Lead-Off Detection Behavior

Table 14 shows calculated current and threshold settings to be used for a given contact impedance. For different contact impedances, the table can be calculated using Ohm's Law ($V = I \times R$), where I is the current generator setting and R is the contact impedance. Contact impedance is the body impedance in combination with the two electrode tissue interfaces. The table is meant for reference based on nominal current generator settings. For current generator accuracy refer to the electrical characteristics table. When using dry electrodes, it is recommended to use higher threshold values to accommodate larger electrode offset voltages.

Table 14. Recommended Lead-Off Current and Threshold Values

LOFF_IMAG CURRENT SETTING	CONTACT IMPEDANCE									
	10kΩ	100kΩ	200kΩ	1MΩ	2MΩ	10MΩ	20MΩ	40MΩ		
1.25nA	All Settings of V _{TH}									
20nA	All Settings of V _{TH}									
40nA	All Settings of V _{TH}									
120nA	All Settings of V _{TH}				V _{TH} > 450mV		Do Not Use			
280nA	All Setting of V _{TH}				Do Not Use					
400nA	All Settings of V _{TH}				Do Not Use					
1.2μA	All Settings of V _{TH}			V _{TH} > 450mV	Do Not Use					
2.8μA	All Settings of V _{TH}		Do Not Use							

ECG AC Lead-Off Detection

The MAX86178 offers ECG AC lead-off detection as an alternative to DC lead-off detection. Available frequencies and current stimulus magnitudes are described in the ECG Lead Detect Configuration 1 and 2 registers (0x88 and 0x89). If ECG_LOFF_MODE is set to 1, then AC lead-off is selected. This circuit operates much the same as the DC lead-off circuit, except a clock is applied to chop the DC output current into a square wave. The ECG_LOFF_IMAG[2:0] field is used for setting both the DC and AC lead-off current magnitudes. On the receive side, there is a small AC-to-DC converter that is switched on for AC mode. The rectified DC output is then compared to the same thresholds that are used for DC lead-off detection. The AC stimulus frequency is set by ECG_LOFF_FREQ[3:0]—details are available in the [ECG Sample Rate and AC Lead-Off Frequency](#) section.

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The MAX86178 includes a utility mode that repurposes the BioZ receive channel to measure ($V_{ECGP} - V_{ECGN}$), ($V_{ECGP} - V_{MID_ECG}$), ($V_{ECGN} - V_{MID_ECG}$), or ($V_{CAPP} - V_{CAPN}$). Utility mode measurements are used to determine the DC biases of the ECG inputs since the ECG channel only measures the high-pass-filtered differential-input voltage. The DC bias information can be used to determine if the inputs are within range, or to directly measure the DC lead-off voltage. Utility mode measurements and BioZ measurements cannot be performed simultaneously.

Utility mode is enabled by EN_UTIL_MODE[7](0xA3), and the measurement is selected by BIOZ_EN[1:0](0xA0). BIOZ_DM_DIS[2](0xA5) must be set to 1 to disable the demodulator, and BIP_ASSIGN[7:6](0xAC) and BIN_ASSIGN[5:4](0xAC) must each be set to 0x3 to connect the selected signal. The selected signal is applied to the inputs of the BioZ PGA as shown in [Figure 33](#). The PGA gain is set by BIOZ_GAIN[1:0](0xA5) and can be set to 1V/V, 2.5V/V, or 5V/V. The utility mode sample rate is equal to the BioZ sample rate, as discussed in the [BioZ Sample Rate and Stimulus Frequency](#) section. Utility mode samples are 20 bits, and marked with unique data tags in the FIFO (see the [FIFO Description](#) section). The input-referred voltage of the selected measurement can be calculated with the following equation.

$$V_{UTIL}(V) = ADC_COUNT \times V_{REF_ECG} / (2^{19} \times BIOZ_PGA_GAIN)$$

where,

ADC_COUNT = ADC counts in signed magnitude format

$V_{REF_ECG} = 1V$ (typ)

BIOZ_PGA_GAIN = PGA gain set by BIOZ_GAIN

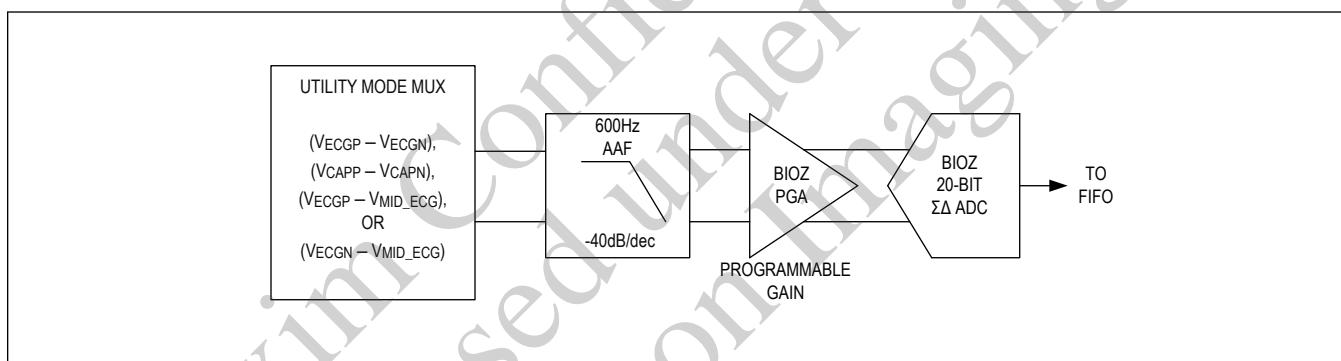


Figure 33. Utility Mode Signal Chain

ECG Calibration Voltage Sources

Calibration voltage sources are available to provide rectangular pulse-train signals for internal signal-chain validation. Each of the two sources, VCALP and VCALN, can be unipolar or bipolar with respect to V_{MID_ECG} , with amplitudes of $\pm 0.25mV$ or $\pm 0.5mV$. Each input can be connected to either of the two sources or V_{MID_ECG} for differential mode amplitudes between $0.25mV_{P-P}$ and $2.0mV_{P-P}$ or common-mode amplitudes between $0.25mV_{P-P}$ and $1mV_{P-P}$.

[Figure 34](#) illustrates the possible calibration waveforms. Frequency selections are available in 4x increments from 15.625mHz to 256Hz with pulse widths between 30.5 μs and 31.723ms or 50% duty cycle. When applying calibration voltage sources with the device connected to a subject, the series input switches must be disconnected so as not to drive signals into the subject. See registers ECG CAL Configuration 1/2/3 (0x84, 0x85, 0x86) to select a configuration.

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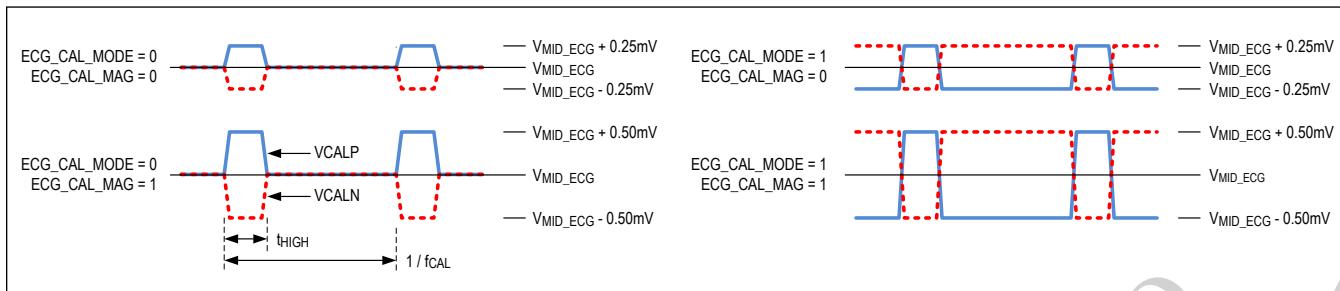
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Figure 34. Calibration Voltage Source Options

Converting Digitized ECG Samples to Voltage

Biopotential channel samples are recorded in 18-bit, left justified, 2's complement format. After converting to signed magnitude format, the biopotential channel differential input voltage, V_{ECG} (mV) = $(V_{ECGP} - V_{ECGN})$, is calculated by the following equation:

$$V_{ECG} (\text{mV}) = \text{ADC_COUNT} \times V_{REF_ECG} / (2^{17} \times \text{ECG_GAIN})$$

ADC_COUNT is the ADC counts in signed magnitude format, V_{REF_ECG} is 1000mV (typ, see the [Electrical Characteristics](#) section) and $\text{ECG_GAIN} = \text{ECG_INA_GAIN} \times \text{ECG_PGA_GAIN}$. ECG_INA_GAIN is programmable between 2.5V/V and 60V/V; and ECG_PGA_GAIN is programmable at 1V/V, 2V/V, 4V/V, 8V/V, or 16V/V. These two gains are set in the ECG Configuration 2 register (0x81).

ECG Noise Measurements

[Table 15](#), [Table 16](#), [Table 17](#), and [Table 18](#) show the typical noise performance of the biopotential channel of MAX86178 referred to the ECG inputs for the four INA range settings. Most applications use gains of 10V/V or higher, but lower gain ranges are included for an expanded AC differential-input range to accommodate large baseline wander. These lower gain settings exhibit higher input-referred noise compared to gains larger than 10V/V. The input-referred noise is given over three different bandwidths: 40Hz, 100Hz, and 150Hz. Note that this low-pass filtering is assumed to be done as a post-processed step by the microcontroller and its firmware, as there is no on-chip digital low-pass filtering. The filters used for the data in this table are 12-tap digital FIR filters with 20dB of stop-band attenuation. This filter design is optimized for low signal latency when displaying the ECG signal in real time. Higher-order digital filters are suitable for ECG recording systems where latency is not an issue and a better filter response is preferred. This data was taken at 512sps, with the RMS and P-P values measured over 1 a second window.

Table 15. Biopotential Channel Noise Performance with ECG_INA_RGE = 0x0

ECG_INA_RGE	PGA GAIN (V/V)	INA GAIN (V/V)	TOTAL GAIN (V/V)	BAND-WIDTH (Hz)	NOISE (μVRMS)	NOISE (μVP-P)	SNR (dB)	ENOB (bits)
0	1	10	10	40	1.04	5.52	96.6	15.8
				100	1.24	7.41	95.1	15.5
				150	1.32	8.13	94.6	15.4
	20	20	20	40	0.64	3.34	94.8	15.5
				100	0.94	5.95	91.5	14.9
				150	1.04	6.66	90.6	14.8
	40	40	40	40	0.74	4.09	87.5	14.2
				100	0.95	4.75	85.4	13.9
				150	1.03	5.65	84.7	13.8
	60	60	60	40	0.67	3.56	84.9	13.8
				100	0.88	4.65	82.6	13.4

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(continued)**

ECG_INA_RGE	PGA GAIN (V/V)	INA GAIN (V/V)	TOTAL GAIN (V/V)	BAND-WIDTH (Hz)	NOISE (μVRMS)	NOISE ($\mu\text{Vp-p}$)	SNR (dB)	ENOB (bits)
2	10	20	150	40	0.98	5.60	81.6	13.3
				40	0.88	4.17	92.1	15.0
				100	1.07	6.70	90.4	14.7
				150	1.14	6.87	89.8	14.6
	20	40	20	40	0.68	3.53	88.2	14.4
				100	0.89	5.36	85.9	14.0
				150	0.98	6.09	85.1	13.8
				40	0.71	3.68	81.8	13.3
	40	80	40	100	0.91	5.34	79.7	12.9
				150	1.01	6.53	78.9	12.8
				40	0.64	3.64	79.3	12.9
				100	0.85	4.50	76.8	12.5
	60	120	20	150	0.94	4.95	76.0	12.3
				40	0.75	4.03	87.4	14.2
				100	0.98	5.42	85.1	13.8
				150	1.09	6.34	84.2	13.7
			40	40	0.70	4.40	82.0	13.3
				100	0.87	4.79	80.1	13.0
				150	0.97	5.60	79.2	12.9
				40	0.68	4.29	76.3	12.4
	40	160	40	100	0.87	5.10	74.2	12.0
				150	0.96	5.53	73.3	11.9
				40	0.63	3.19	73.3	11.9
				100	0.82	4.40	71.1	11.5
	60	240	60	150	0.91	5.69	70.2	11.4
				40	0.78	3.69	81.1	13.2
				100	1.01	6.33	78.8	12.8
				150	1.11	6.17	78.0	12.7
			20	40	0.61	2.98	77.1	12.5
				100	0.86	4.84	74.2	12.0
				150	0.97	5.79	73.1	11.9
				40	0.68	3.90	70.2	11.4
	40	320	40	100	0.88	5.32	68.0	11.0
				150	0.95	5.99	67.3	10.9
				40	0.65	3.58	67.1	10.9
				100	0.86	4.78	64.6	10.4
	60	480	60	150	0.94	5.70	63.9	10.3
				40	0.78	4.66	75.1	12.2
				100	0.95	6.51	73.4	11.9

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**Table 15. Biopotential Channel Noise Performance with ECG_INA_RGE = 0x0
 (continued)**

ECG_INA_RGE	PGA GAIN (V/V)	INA GAIN (V/V)	TOTAL GAIN (V/V)	BAND-WIDTH (Hz)	NOISE (μVRMS)	NOISE ($\mu\text{V}_{\text{P-P}}$)	SNR (dB)	ENOB (bits)
	20	320	150	150	1.02	7.00	72.7	11.8
				40	0.58	3.00	71.6	11.6
				100	0.81	4.43	68.8	11.1
				150	0.88	5.12	68.0	11.0
	40	640	40	40	0.70	3.84	63.9	10.3
				100	0.83	5.04	62.4	10.1
				150	0.92	5.96	61.6	9.9
				40	0.74	3.85	60.0	9.7
	60	960	100	40	0.93	5.01	57.9	9.3
				150	1.02	6.08	57.2	9.2

Note: $\text{SNR} = 20\log\left(\frac{V_{\text{IN(RMS)}}}{V_{\text{N(RMS)}}}\right)$, $\text{ENOB} = (\text{SNR} - 1.76) / 6.02$

Note: $V_{\text{IN(P-P)}} = 2\text{V} / \text{TOTAL GAIN}$, which represents the largest signal that can be input into the ECG channel.

$$V_{\text{IN(RMS)}} = V_{\text{IN(P-P)}} / (2\sqrt{2}).$$

Table 16. Biopotential Channel Noise Performance with ECG_INA_RGE = 0x1

ECG_INA_RGE	PGA GAIN (V/V)	INA GAIN (V/V)	TOTAL GAIN (V/V)	BAND-WIDTH (Hz)	NOISE (μVRMS)	NOISE ($\mu\text{V}_{\text{P-P}}$)	SNR (dB)	ENOB (bits)	
1	7.5	7.5	40	40	1.13	5.55	98.5	16.1	
				100	1.39	7.49	96.6	15.8	
				150	1.48	8.24	96.1	15.7	
			15	40	0.94	5.21	94.0	15.3	
	15	15		100	1.15	7.20	92.3	15.0	
				150	1.21	8.19	91.8	15.0	
		30	40	0.79	3.79	89.5	14.6		
	30		30		100	1.01	5.48	87.4	14.2
					150	1.08	5.77	86.8	14.1
		45	40	0.78	4.35	86.1	14.0		
	45		45		100	0.97	5.71	84.2	13.7
					150	1.09	6.38	83.1	13.5
		7.5	40	0.96	5.38	93.8	15.3		
	2		15		100	1.23	6.72	91.7	14.9
					150	1.34	7.65	90.9	14.8
		15	40	0.86	4.91	88.7	14.4		
	30		30		100	1.09	6.88	86.7	14.1
					150	1.18	7.44	86.0	14.0
		60	40	0.80	4.68	83.4	13.6		
	45		90		100	1.02	6.35	81.3	13.2
					150	1.09	6.50	80.7	13.1

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(continued)**

ECG_INA_RGE	PGA GAIN (V/V)	INA GAIN (V/V)	TOTAL GAIN (V/V)	BAND-WIDTH (Hz)	NOISE (μVRMS)	NOISE ($\mu\text{Vp-p}$)	SNR (dB)	ENOB (bits)
4	7.5	30	100	100	0.94	5.76	78.5	12.7
				150	1.04	6.38	77.6	12.6
				40	0.91	5.14	88.3	14.4
	15	60	100	100	1.12	6.20	86.4	14.1
				150	1.21	7.55	85.8	14.0
				40	0.70	3.55	84.5	13.7
	30	120	100	100	0.93	4.90	82.0	13.3
				150	1.05	5.48	81.0	13.2
				40	0.75	4.09	77.9	12.6
	45	180	100	100	0.96	5.82	75.8	12.3
				150	1.06	5.85	74.9	12.1
				40	0.77	3.79	74.2	12.0
	8	60	100	100	0.95	5.98	72.4	11.7
				150	1.02	6.69	71.7	11.6
				40	0.82	4.40	83.1	13.5
	15	120	100	100	1.09	5.60	80.7	13.1
				150	1.18	7.05	80.0	13.0
				40	0.80	4.37	77.3	12.6
	30	240	100	100	1.05	5.98	75.0	12.2
				150	1.12	6.84	74.5	12.1
				40	0.79	3.94	71.4	11.6
	45	360	100	100	0.95	5.66	69.8	11.3
				150	1.06	6.27	68.9	11.1
				40	0.81	4.95	67.7	11.0
	16	120	100	100	1.02	6.92	65.7	10.6
				150	1.14	7.55	64.7	10.5
				40	0.81	3.96	77.2	12.5
	7.5	240	100	100	1.10	5.96	74.6	12.1
				150	1.19	6.49	73.9	12.0
				40	0.85	4.91	70.8	11.5
	15	480	100	100	1.04	5.98	69.1	11.2
				150	1.13	6.44	68.3	11.1
				40	0.81	4.67	65.1	10.5
	30	720	100	100	1.02	6.35	63.2	10.2
				150	1.13	6.51	62.3	10.1
				40	0.79	4.14	61.9	10.0
	45	720	100	100	1.00	6.13	59.9	9.6
				150	1.06	6.53	59.3	9.6

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Note: SNR = $20\log\left(\frac{V_{IN(RMS)}}{V_{N(RMS)}}\right)$, ENOB = $(SNR - 1.76) / 6.02$

Note: $V_{IN(P-P)} = 2V / \text{TOTAL GAIN}$, which represents the largest signal that can be input into the ECG channel.

$$V_{IN(RMS)} = V_{IN(P-P)} / (2\sqrt{2})$$

Table 17. Biopotential Channel Noise Performance with ECG_INA_RGE = 0x2

ECG_INA_RGE	PGA GAIN (V/V)	INA GAIN (V/V)	TOTAL GAIN (V/V)	BAND-WIDTH (Hz)	NOISE (μVRMS)	NOISE (μV_{P-P})	SNR (dB)	ENOB (bits)
1	5	5	5	40	1.63	9.24	98.7	16.1
				100	2.00	10.90	97.0	15.8
				150	2.14	11.59	96.4	15.7
	10	10	10	40	1.14	5.61	95.8	15.6
				100	1.45	8.07	93.7	15.3
				150	1.56	9.48	93.1	15.2
	20	20	20	40	0.90	5.58	91.9	15.0
				100	1.21	6.91	89.3	14.5
				150	1.35	7.36	88.3	14.4
	30	30	30	40	1.22	6.72	85.7	14.0
				100	1.41	8.61	84.5	13.7
				150	1.51	9.26	83.9	13.6
2	5	10	10	40	1.38	6.89	94.2	15.4
				100	1.65	10.51	92.6	15.1
				150	1.78	10.86	92.0	15.0
	10	20	20	40	1.11	6.28	90.1	14.7
				100	1.39	8.12	88.1	14.3
				150	1.54	9.64	87.2	14.2
	20	40	40	40	1.05	6.19	84.5	13.7
				100	1.31	8.39	82.6	13.4
				150	1.42	8.93	81.9	13.3
	30	60	60	40	0.98	4.91	81.6	13.3
				100	1.22	7.13	79.7	12.9
				150	1.37	8.77	78.7	12.8
4	5	20	20	40	1.09	6.65	90.2	14.7
				100	1.50	9.05	87.4	14.2
				150	1.63	9.31	86.7	14.1
	10	40	40	40	1.00	5.45	85.0	13.8
				100	1.32	8.03	82.6	13.4
				150	1.42	8.56	81.9	13.3
	20	80	80	40	1.10	6.16	78.1	12.7
				100	1.34	7.89	76.4	12.4
				150	1.44	8.92	75.7	12.3
	30	120	120	40	0.90	5.63	76.3	12.4
				100	1.19	7.53	73.9	12.0
				150	1.30	7.55	73.2	11.9

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**Table 17. Biopotential Channel Noise Performance with ECG_INA_RGE = 0x2
 (continued)**

ECG_INA_RGE	PGA GAIN (V/V)	INA GAIN (V/V)	TOTAL GAIN (V/V)	BAND-WIDTH (Hz)	NOISE (μVRMS)	NOISE ($\mu\text{VP-P}$)	SNR (dB)	ENOB (bits)
8	5	40	40	40	1.01	6.13	84.8	13.8
				100	1.34	8.53	82.4	13.4
				150	1.52	9.40	81.3	13.2
	10	80	80	40	1.07	6.14	78.3	12.7
				100	1.41	8.28	76.0	12.3
				150	1.53	8.96	75.3	12.2
	20	160	160	40	0.89	6.16	73.9	12.0
				100	1.18	7.13	71.5	11.6
				150	1.31	8.48	70.6	11.4
	30	240	240	40	1.06	6.81	68.9	11.2
				100	1.31	8.63	67.0	10.8
				150	1.39	8.57	66.5	10.8
16	5	80	80	40	1.17	5.92	77.6	12.6
				100	1.42	8.55	75.9	12.3
				150	1.53	9.08	75.2	12.2
	10	160	160	40	1.08	5.61	72.2	11.7
				100	1.39	7.75	70.1	11.3
				150	1.50	8.44	69.4	11.2
	20	320	320	40	0.86	4.88	68.2	11.0
				100	1.16	6.72	65.6	10.6
				150	1.31	8.76	64.6	10.4
	30	480	480	40	1.02	5.70	63.2	10.2
				100	1.31	7.09	61.0	9.8
				150	1.43	8.29	60.3	9.7

Note: $\text{SNR} = 20 \log \left(\frac{V_{\text{IN(RMS)}}}{V_{\text{N(RMS)}}} \right)$, $\text{ENOB} = (\text{SNR} - 1.76) / 6.02$

Note: $V_{\text{IN(P-P)}} = 2V / \text{TOTAL GAIN}$, which represents the largest signal that can be input into the ECG channel.

$V_{\text{IN(RMS)}} = V_{\text{IN(P-P)}} / (2\sqrt{2})$.

Table 18. Biopotential Channel Noise Performance with ECG_INA_RGE = 0x3

ECG_INA_RGE	PGA GAIN (V/V)	INA GAIN (V/V)	TOTAL GAIN (V/V)	BAND-WIDTH (Hz)	NOISE (μVRMS)	NOISE ($\mu\text{VP-P}$)	SNR (dB)	ENOB (bits)
3	1	2.5	2.5	40	3.19	18.67	99.0	16.2
				100	3.81	24.08	97.4	15.9
				150	3.99	24.94	97.0	15.8
	5	5	5	40	2.13	11.22	96.4	15.7
				100	2.64	15.90	94.6	15.4
				150	2.83	17.91	94.0	15.3
	10	10	10	40	2.01	10.29	90.9	14.8
				100	2.50	15.47	89.0	14.5

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(continued)**

ECG_INA_RGE	PGA GAIN (V/V)	INA GAIN (V/V)	TOTAL GAIN (V/V)	BAND-WIDTH (Hz)	NOISE (μVRMS)	NOISE ($\mu\text{Vp-p}$)	SNR (dB)	ENOB (bits)
2	15	15	15	150	2.65	18.48	88.5	14.4
				40	2.07	11.73	87.2	14.2
				100	2.45	16.32	85.7	13.9
				150	2.55	18.00	85.3	13.9
	2.5	5	5	40	2.58	14.89	94.8	15.5
				100	3.15	18.70	93.0	15.2
				150	3.26	19.79	92.7	15.1
	5	10	10	40	2.22	11.78	90.1	14.7
				100	2.69	14.87	88.4	14.4
				150	2.82	15.70	88.0	14.3
	10	20	20	40	1.81	9.20	85.8	14.0
				100	2.27	14.19	83.9	13.6
				150	2.39	14.97	83.4	13.6
	15	30	30	40	1.66	9.01	83.1	13.5
				100	2.12	15.00	80.9	13.1
				150	2.35	15.75	80.0	13.0
4	2.5	10	10	40	2.22	11.75	90.1	14.7
				100	2.74	15.08	88.2	14.4
				150	3.02	16.57	87.4	14.2
	5	20	20	40	1.82	11.28	85.8	14.0
				100	2.26	14.08	83.9	13.6
				150	2.45	15.47	83.2	13.5
	10	40	40	40	1.80	10.23	79.9	13.0
				100	2.27	13.15	77.8	12.6
				150	2.43	14.95	77.2	12.5
	15	60	60	40	1.53	7.91	77.7	12.6
				100	1.99	9.81	75.4	12.2
				150	2.18	11.18	74.6	12.1
8	2.5	20	20	40	2.12	12.93	84.4	13.7
				100	2.51	17.03	83.0	13.5
				150	2.73	17.35	82.2	13.4
	5	40	40	40	1.79	10.80	79.9	13.0
				100	2.24	13.57	77.9	12.7
				150	2.40	14.57	77.3	12.6
	10	80	80	40	1.65	9.66	74.6	12.1
				100	2.09	11.69	72.5	11.8
				150	2.26	13.31	71.8	11.6
	15	120	120	40	1.76	11.21	70.5	11.4
				100	2.21	11.97	68.5	11.1

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(continued)**

ECG_INA_RGE	PGA GAIN (V/V)	INA GAIN (V/V)	TOTAL GAIN (V/V)	BAND-WIDTH (Hz)	NOISE (μVRMS)	NOISE ($\mu\text{Vp-p}$)	SNR (dB)	ENOB (bits)
16	2.5	40	150	150	2.36	13.98	67.9	11.0
				40	2.05	11.85	78.7	12.8
				100	2.56	16.60	76.8	12.5
				150	2.66	17.07	76.5	12.4
	5	80	100	40	2.19	12.51	72.1	11.7
				100	2.56	18.25	70.8	11.5
				150	2.58	19.19	70.7	11.5
	10	160	150	40	1.89	10.11	67.4	10.9
				100	2.24	13.51	65.9	10.7
				150	2.37	13.97	65.4	10.6
	15	240	100	40	1.64	8.82	65.1	10.5
				100	2.23	13.42	62.4	10.1
				150	2.39	15.23	61.8	10.0

Note: $\text{SNR} = 20\log\left(\frac{V_{\text{IN(RMS)}}}{V_{N(\text{RMS})}}\right)$, $\text{ENOB} = (\text{SNR} - 1.76) / 6.02$

Note: $V_{\text{IN(P-P)}} = 2V / \text{TOTAL GAIN}$, which represents the largest signal that can be input into the ECG channel.

$$V_{\text{IN(RMS)}} = V_{\text{IN(P-P)}} / (2\sqrt{2}).$$

Right Leg Drive and Body Bias

The right leg drive (RLD) circuit enables improved system-level common-mode rejection of signals coupled to the user from the environment, primarily 50Hz or 60Hz power-line interference. When RLD is enabled through RLD_EN[7](0x92), the circuit senses the AC common-mode input signal from the input electrodes, inverts and amplifies the signal, and drives it onto the body through a third electrode. This has the effect of attenuating the common-mode signal at the inputs and driving them toward a selectable reference voltage, typically $V_{\text{MID_ECG}}$. This also ensures proper common-mode biasing of the electrodes, allowing the internal lead bias resistors to be disabled. Alternatively, the RLD circuit acts as a DC body-bias buffer when RLD_MODE[6](0x92) is set to 0. When RLD_EN = 0, the output of the RLD amplifier and the RLD pin are high-impedance.

The RLD circuit, shown in [Figure 35](#), has three main parts: a common-mode averager, an amplifier, and an out-of-range detector. The common-mode detector selects a combination of the input voltage, with ACTV_CM_P[3](0x92) and ACTV_CM_N[2](0x92) enabling the positive and negative inputs to the detector, and RLD_SEL_ECG[6](0x93) and RLD_SEL_BIOZ[7](0xA7) selecting ECGP and ECGN, CAPP and CAPN, or BIP and BIN. The voltages at CAPP and CAPN are low-pass filtered, so these are less effective at attenuating higher frequency common-mode signals such as power-line interference. The use of BIP and BIN voltages might be considered in case one is simultaneously using the biopotential channel for ECG and the bioimpedance channel for BIA/BIS work.

The amplifier applies inverting gain to the common-mode signal and applies negative feedback with a selectable reference and bandwidth. The default reference setting is $V_{\text{MID_ECG}}$, but this can be adjusted up or down to compensate for electrode offset voltages by setting BODY_BIAS_DAC[3:0](0x93). The amplifier can use internal or external feedback with RLD_EXT_RES[7](0x93) connecting or disconnecting the internal feedback network. The internal feedback network sets the gain to 12V/V, 24V/V, 48V/V, or 97V/V according to RLD_GAIN[1:0](0x92). The external feedback network cannot be disconnected internally, so RLD_INV should be left disconnected if using internal feedback only. If using external feedback, the gain is equal to $(100\text{k}\Omega + R_{\text{RLDFB}}) / 150\text{k}\Omega$ when averaging both inputs. The higher gain settings provide the best results for electrodes with high contact impedance, including dry electrodes.

The amplifier bandwidth can be adjusted with RLD_BW[5:4](0x93), but the lowest bandwidth setting is adequate for

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power-line frequencies. Higher bandwidth settings consume more power. If enabled by EN_RLD_OOR[4](0x92), the out-of-range detector detects if the RLD output voltage goes outside of $0.127 \times V_{AVDD}$ and $0.870 \times V_{AVDD}$ for 128ms, and asserts the RLD_OOR[3](0x04) status bit. If BYP_DLY[7](0x12) is enabled, the 128ms delay is bypassed and RLD_OOR is asserted immediately. This function indicates that the total impedance between the RLD electrode and the input electrodes is too high to maintain the feedback loop, usually because electrodes are off or have poor contact on the person.

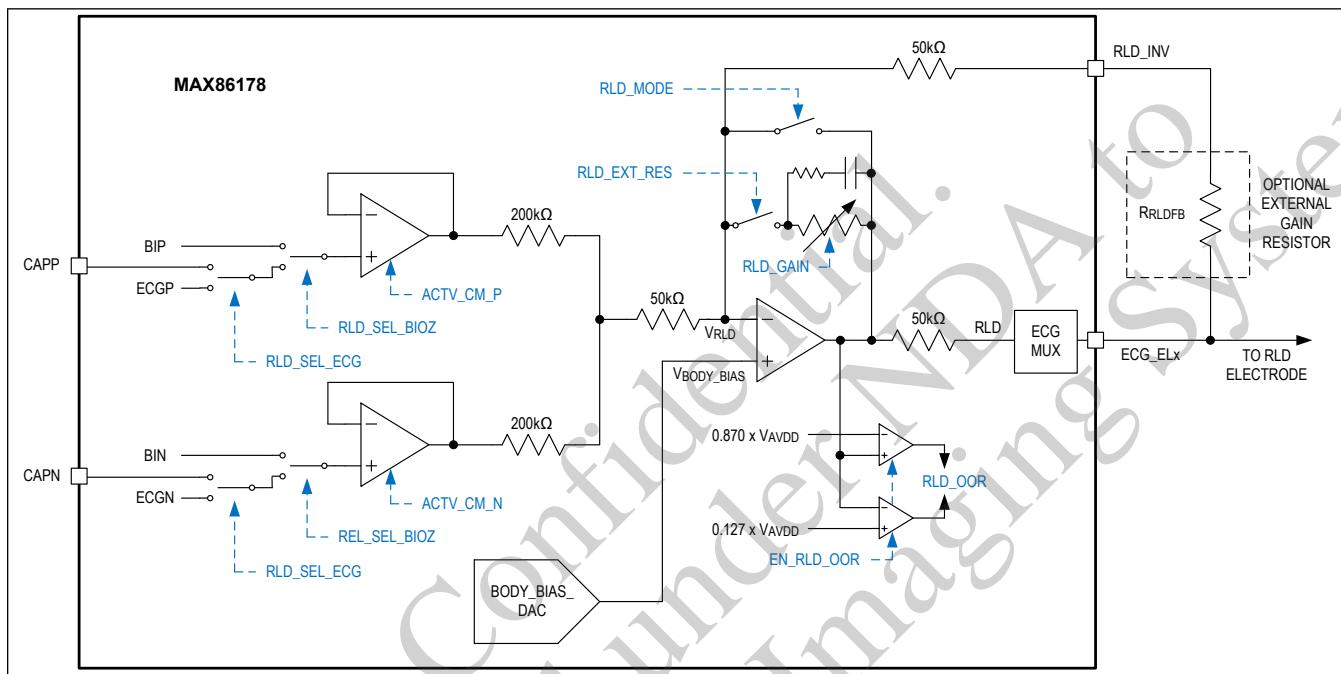


Figure 35. Detailed Right Leg Drive (RLD) Block Diagram

ECG Lead Bias

The MAX86178 limits the ECGP and ECGN DC input common-mode range between 0.25V and ($V_{AVDD} - 0.5V$). This range can be maintained either through external or internal lead biasing.

Internal DC lead biasing consists of $50\text{M}\Omega$, $100\text{M}\Omega$, or $200\text{M}\Omega$ selectable resistors connected from ECGP and ECGN to either V_{MID_ECG} or V_{RLD} that bias the MAX86178 to the proper potential relative to the body in battery-powered systems. By matching the voltage of V_{MID_ECG} to the body, the lead bias ensures that the common-mode input voltage of ECGP and ECGN are within the DC input range of the ECG channel. Lead bias is only effective when the MAX86178 system has high galvanic isolation from earth ground. See ECG RBIAS_VALUE[3:2](0x90) to select a resistance value, and EN_ECG RBIASP[1](0x90) and EN_ECG RBIASN[1](0x90) to enable lead bias. The lead bias voltage is selected by RLD RBIAS[5](0x92). Selecting V_{RLD} (the output of the right leg drive common-mode averager) as the lead bias voltage can improve the ECG channel CMRR without needing a third electrode. If the ECG and BioZ receive channels share electrodes, only one channel should have the lead bias enabled.

BioZ

The BioZ system shown in Figure 36 primarily consists of a transmit (TX) channel, a receive (RX) channel, and an input/output MUX. The BioZ system supports calibration using internal or external calibration resistors, enabling 0.1% accuracy in the I/Q channel. The flexible I/O MUX, lead-on and lead-off detection, adjustable amplifier bias, and lead bias allow for flexible hardware designs capable of multiple measurement types with low power consumption. The stimulus frequency and sample rate are determined by the timing subsystem (see the [Timing Subsystem](#) section).

The BioZ channel can measure impedances across multiple application areas with a wide range of frequencies and magnitudes as shown in Figure 37. Each type of stimulus can operate over frequencies between 16Hz and 806kHz, as

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well as DC current-mode measurements.

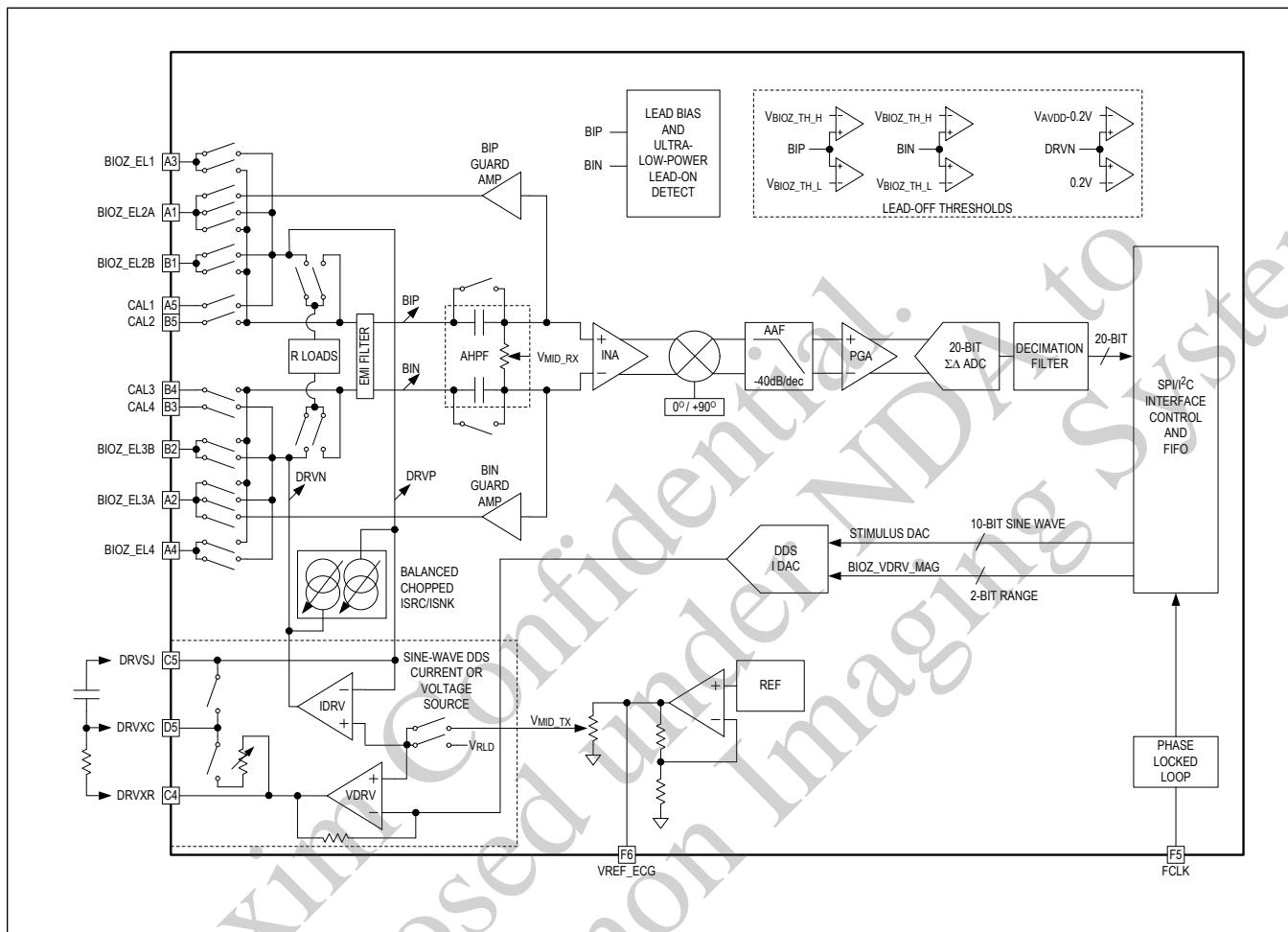


Figure 36. BioZ System Block Diagram

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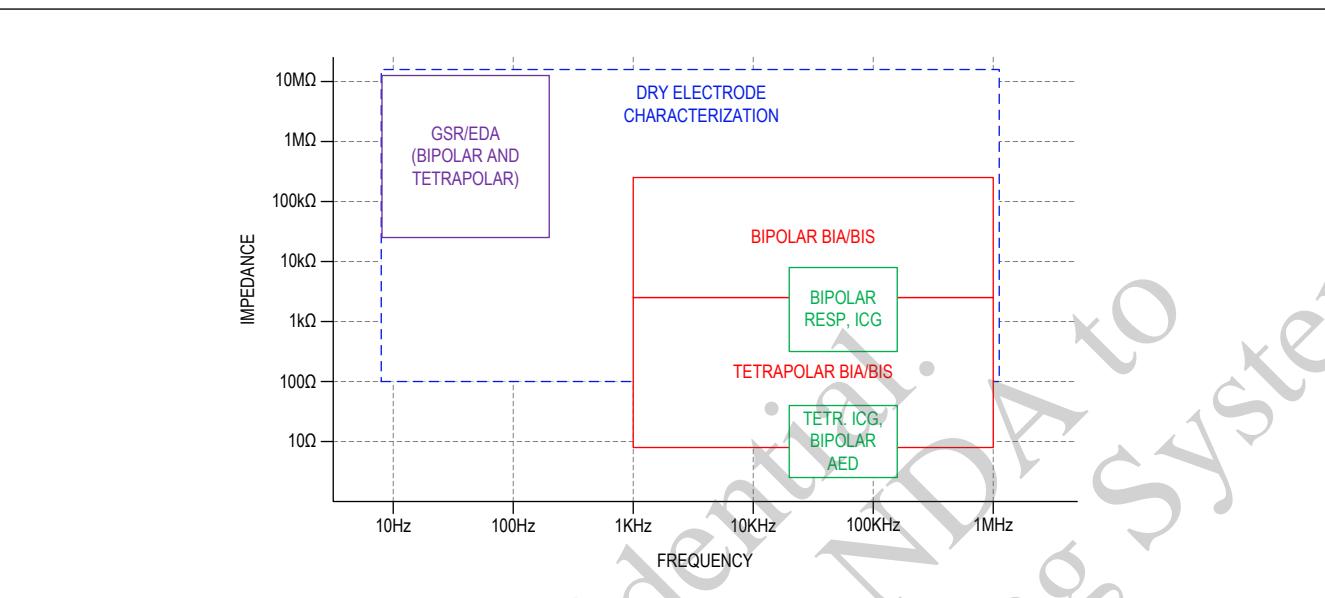
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Figure 37. BioZ Typical Application Areas

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To power on the BioZ subsystem, set ECG_BIOZ_BG_EN[2](0xA0) to 1, which enables the bandgap reference shared by the ECG and BioZ channels, V_{REF_ECG}. After a startup time of approximately 200ms, BioZ measurements can be initiated by selecting in-phase (I) or quadrature (Q) in BIOZ_EN[1:0](0xA0). BioZ data begins within 2ms of enabling the measurement.

When the measurement is finished, the BioZ subsystem can be shut down by writing ECG_BIOZ_BG_EN and BIOZ_EN to 0x0. Alternatively, if another measurement is set to follow shortly after, setting BIOZ_DRV_MODE[1:0](0xA2) to 0x3 can place the BioZ TX channel into standby mode, while ECG_BIOZ_BG_EN and BIOZ_EN remain set to their active values. Standby mode disables the stimulus but maintains the DC bias of the drive electrodes, preventing any settling time associated with charging the electrode and body capacitance during the next measurement. In standby mode, the receive channel stops sampling and enters low-power mode unless BIOZ_STBYON[4](0xA7) is set. Setting BIOZ_STBYON = 1 can further reduce settling time during the next measurement by maintaining the receive channel in an active state.

Note that if the BioZ channel is disabled while a sample is being pushed to the FIFO, the FIFO will contain an extra sample containing the value 0x4000, which should be ignored. This can be avoided by disabling the BioZ channel immediately after a FIFO_DATA_RDY or A_FULL interrupt.

BioZ Transmit Channel

The MAX86178 can generate four types of stimuli: a balanced square-wave source/sink current, a sine-wave current, a sine-wave voltage, and an H-bridge voltage square wave. Each of these modes are described in the following sections. The stimulus generator can be put into a low-power standby mode by setting BIOZ_DRV_MODE[1:0](0xA2) to 0x3. In this mode, the DDS circuit remains active, but the BIOZ_DRV_RESET switch is closed, driving DRVN to V_{MID_TX}. The amplifiers are put into a low-power state to reduce power consumption, and the H-bridge driver is disabled.

Balanced Square-Wave Current Source/Sink Stimulus

The primary stimulus mode recommended for respiration measurements and ICG measurements is the balanced square-wave source/sink current generator, shown in [Figure 38](#). To select this mode, set BIOZ_EN[1:0](0xA0) to 0x1 or 0x2 and set RESP_EN[0](0xB6) to 1.

Current amplitudes between 8μA_{PK} to 384μA_{PK} are selectable using this mode of operation. The magnitude of the

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CG stimulus is controlled by RESP(CG_MAG[6:4](0xB1) and RESP(CG_MAG_4X[7](0xB1). The range of frequencies intended for use with this mode is 10kHz to 131kHz. For patient safety according to IEC 60601-1, do not assert the RESP(CG_MAG_4X bit unless the stimulus frequency is greater than 10kHz. The current amplitude should also be chosen to not exceed 1000mVp-p at the BIP and BIN inputs based on the network impedance at the current injection frequency. 47nF DC blocking capacitors are required between the patient drive electrodes and the pins assigned to DRVP and DRVN, typically BIOZ_EL1 and BIOZ_EL4.

The current generators have several options for common-mode feedback, which corrects for current source/sink mismatch and maintains the common mode bias of the current generators. The type of common-mode feedback is selected by CG_MODE[2:1](0xB6), and the trade-offs of each mode are shown in [Table 19](#). Dynamic matching (or chopping) is used to reduce current source/sink mismatch, and greatly reduces 1/f flicker noise. Low-pass common-mode filtering reduces the dynamic matching bandwidth to maintain higher common-mode source impedance, which is important when using a two electrode configuration or sharing electrodes with the ECG channel. The bandwidth of the LPF is controlled by CG_LPF_DUTY[7:5](0xB6).

Table 19. Current Generator Common Mode Feedback Options

CG_MODE	Common Mode Feedback (CMFB) Operation
0x0	Dynamic matching disabled with analog low-pass filter. Higher 1/f noise with higher common-mode impedance at 50Hz/60Hz.
0x1	Dynamic matching enabled without analog low-pass filter. Lower 1/f noise with lower common-mode impedance at 50Hz/60Hz.
0x2	Dynamic matching enabled with analog low-pass filter. Lower 1/f noise with higher common-mode impedance. This is the recommended mode, but stability is not guaranteed across all circumstances due to the limited common mode feedback bandwidth.
0x3	Dynamic matching enabled with internal resistive common-mode load. Lower 1/f noise with 5MΩ resistors connecting each current source/sink output to V _{MID_TX} . This mode has high common-mode impedance at 50Hz and 60Hz, but has lower input impedance than can be achieved with the CMFB amplifier.

The user should consider the CG_MODE selection as a toolbox for optimizing the BioZ measurement results. Further optimization of the CG_MODE = 0x0 and CG_MODE = 0x2 options, which use the low-pass filter within the CMFB circuit, can be achieved by adjusting CG_LPF_DUTY that sets the CMFB circuit bandwidth. The CMFB bandwidth can be set to various values of CG_LPF_DUTY, which varies the number of FCLK cycles in the setting of the duty cycle feedback signal, acting as a low-pass filter. A CG_LPF_DUTY of 1 FCLK cycle yields a 0.98Hz bandwidth. Each doubling of the the CG_LPF_DUTY doubles the bandwidth. See the Register Map for details. The bandwidth should be chosen according to the application; for instance, a respiration application might use the 7.79Hz or 15.54Hz setting, and an ICG application might use the 30.89Hz or 61.08Hz setting.

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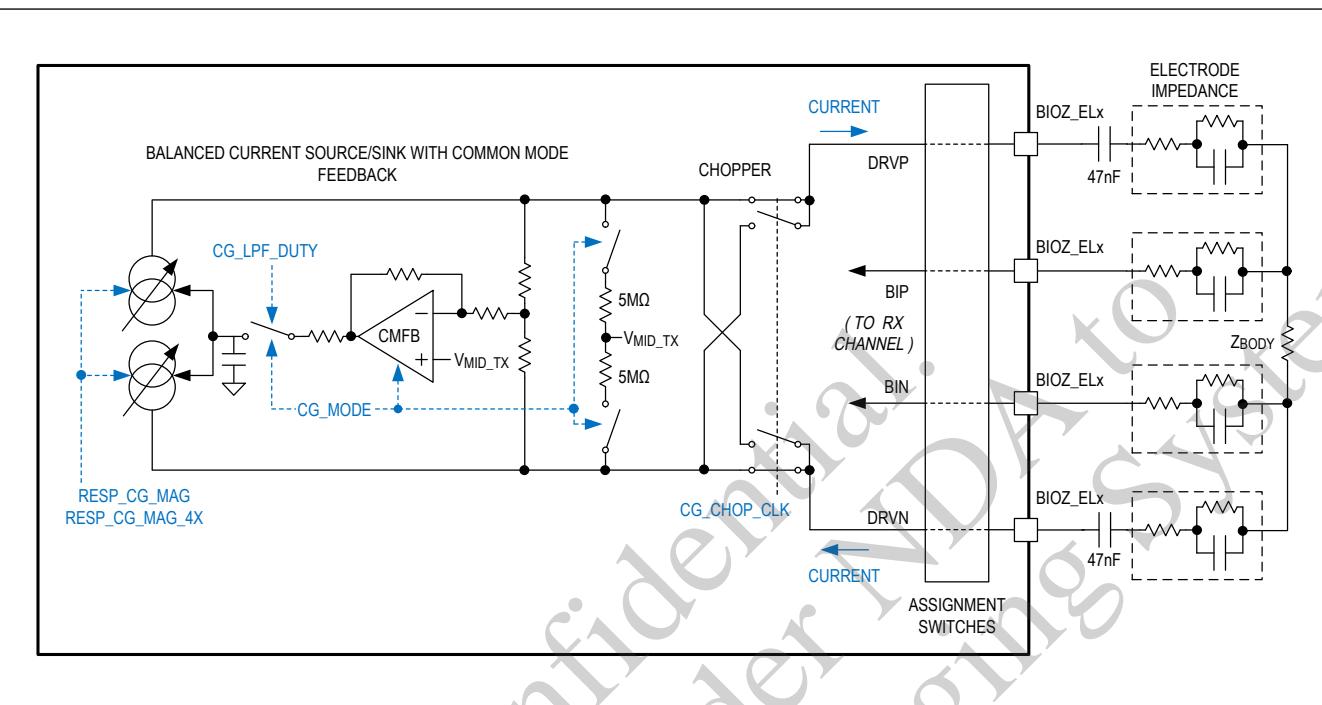
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Figure 38. Bioimpedance Stimulus Generator—Balanced Square Wave Current Mode

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Sine-Wave Current Stimulus

To select the sine-wave current mode, set BIOZ_DRV_MODE[1:0](0xA2) to 0x0 and RESP_EN[0](0xB6) to 0. When generating a sine-wave current stimulus, the AC current is injected into the body using electrodes assigned to the DRVP and DRVN (drive) functions with the bioimpedance sensed differentially through the electrodes assigned to the BIP and BIN (bioimpedance receive) functions. Two and four electrode configurations are supported for typical wet or dry electrode impedances. [Figure 39](#) shows the stimulus signal path with a four electrode configuration. A sine-wave current stimulus is generated by a direct digital synthesis (DDS) circuit with the help of a 10-bit current DAC (I DAC). The VDRV amplifier converts this sine-wave current into a sine-wave voltage. One of four range resistors should be selected using BIOZ_IDRV_RGE[3:2](0xA2). The current range can alternatively be set with an external resistor by enabling BIOZ_EXT_RES[7](0xA2). The sine-wave voltage appears on one side of this resistor and the other side is held at V_{MID_TX} by the operation of the IDRV amplifier; thus, creating the sine-wave current stimulus in the IDRV amplifier feedback loop. This current flows through the range resistor, the electrodes, and the body impedance, then back into the IDRV amplifier output terminal.

A blocking capacitor (C_{EXT}) connected between the DRVXC and DRVSJ pins is required to avoid the DC current from being driven through the body. A 47nF capacitor is recommended for all applications.

Both amplifiers in the signal chain have adjustable range and bandwidth to optimize power consumption for the required performance. BIOZ_AMP_RGE[3:2](0xA6) sets the amplifier range, and BIOZ_AMP_BW[1:0](0xA6) sets the gain-bandwidth product. When using the MAX86178 for impedance cardiography (ICG), it is recommended to set the BIOZ_AMP_RGE and BIOZ_AMP_BW to higher values. It is generally acceptable to leave these settings at the lowest value for other applications.

When selecting a stimulus current magnitude, there are several restrictions that must be followed. The stimulus current is set by a combination of BIOZ_IDRV_RGE[3:2](0xA2) and BIOZ_VDRV_MAG[5:4](0xA2), and [Table 20](#) shows the stimulus current options available for MAX86178.

1. To ensure patient safety, some current amplitude and frequency combinations are not allowed (see [Table 20](#)). If an off-limits setting is selected, the BIOZ_VDRV_MAG and BIOZ_IDRV_RGE fields are automatically overwritten

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to the highest allowed value based on the frequency settings. It is the responsibility of the end application device manufacturer to ensure that the MAX86178 is programmed properly and in conformance with *IEC60601-1 Medical electrical equipment—Part 1: General requirements for basic safety and essential performance* with regards to patient auxiliary current limitations.

2. When using stimulus currents greater than $640\mu\text{A}_{\text{RMS}}$, BIOZ_EL1 and BIOZ_EL4 must be used for DRVP and DRVN, respectively. Electrode pins BIOZ_EL2A, BIOZ_EL2B, BIOZ_EL3A, and BIOZ_EL3B are not designed to support currents above $640\mu\text{A}_{\text{RMS}}$. Assigning the wrong pins does not damage the MAX86178, but switch resistance is higher and degrades measurement accuracy.
3. The current amplitude should be chosen to not exceed $1000\text{mV}_{\text{P-P}}$ at the BIP and BIN pins based on the network impedance at the current injection frequency.

Table 20. Stimulus Current Options

STEP	BIOZ_IDRV_RGE	RANGE RESISTOR	BIOZ_VDRV_MAG	RMS CURRENT	FREQUENCY RANGE (Hz)	RECOMMENDED BIOZ_AMP_RGE
1	1 (0x0)	552.5kΩ	low (0x0)	16nA	All frequencies	Low
2	1 (0x0)	552.5kΩ	low mid (0x1)	32nA	All frequencies	Low
3	1 (0x0)	552.5kΩ	high mid (0x2)	80nA	All frequencies	Low
4	1 (0x0)	552.5kΩ	high (0x3)	160nA	All frequencies	Medium-Low
5	2 (0x1)	110.5kΩ	low (0x0)	320nA	All frequencies	Medium-Low
6	2 (0x1)	110.5kΩ	low mid (0x1)	640nA	All frequencies	Medium-Low
7	2 (0x1)	110.5kΩ	high mid (0x2)	1.6μA	All frequencies	Medium-Low
8	2 (0x1)	110.5kΩ	high (0x3)	3.2μA	All frequencies	Medium-Low
9	3 (0x2)	5.525kΩ	low (0x0)	6.4μA	All frequencies	Medium-Low
10	3 (0x2)	5.525kΩ	low mid (0x1)	12.8μA	All frequencies	Medium-High
11	3 (0x2)	5.525kΩ	high mid (0x2)	32μA	All frequencies	Medium-High
12	3 (0x2)	5.525kΩ	high (0x3)	64μA	All frequencies	Medium-High
13	4 (0x3)	276.25Ω	low (0x0)	128μA	≥ 512	High
14	4 (0x3)	276.25Ω	low mid (0x1)	256μA	≥ 2048	High
15	4 (0x3)	276.25Ω	high mid (0x2)	640μA	≥ 8192	High
16	4 (0x3)	276.25Ω	high (0x3)	1.28mA	≥ 16384	High

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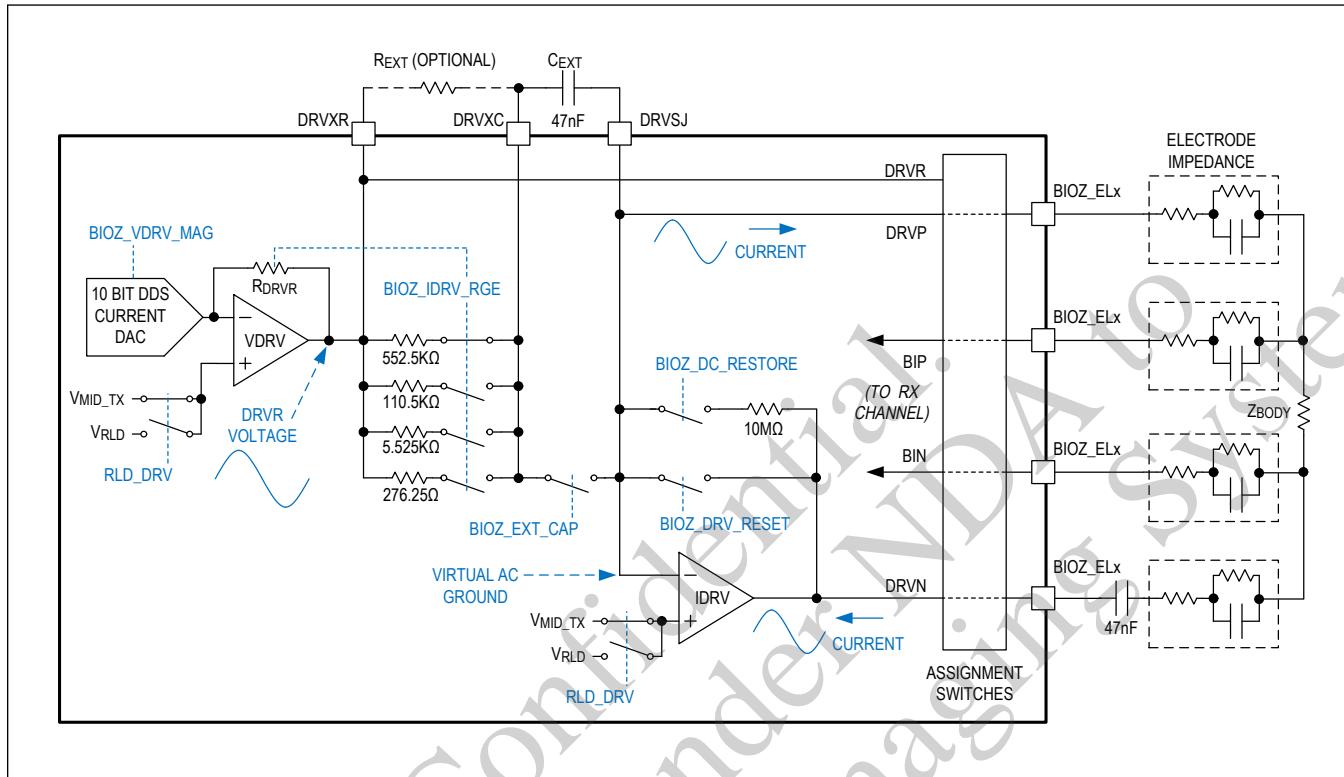


Figure 39. Bioimpedance Stimulus Generator Diagram—Sine-Wave Current Mode

Sine-Wave Voltage Stimulus

To select sine-wave voltage mode, set BIOZ_DRV_MODE[1:0](0xA2) to 0x1 and RESP_EN[0](0xB6) to 0. [Figure 40](#) shows the stimulus signal path for a four electrode configuration. The voltage output from the VDRV amplifier, available on the DRVXR node, is applied directly to the BIOZ_EL1 electrode by means of a switch within the MAX86178 I/O MUX. In this mode of operation, a switch is closed around the IDRVP amplifier so that the amplifier becomes a voltage follower and drives the BIOZ_EL4 node to VMID_TX. In this mode, external resistors on the BIOZ_EL1 and BIOZ_EL4 nodes are used to limit the patient current to $V_{RMS} / (2 \times R_{SERIES})$ where V_{RMS} is the voltage output amplitude out of the VDRV amplifier set by BIOZ_VDRV_MAG[5:4](0xA2). When using this voltage stimulus mode, BIOZ_EL1 must be selected for DRVP, and BIOZ_EL4 must be selected for DRVN. Electrode pins BIOZ_EL2A, BIOZ_EL2B, BIOZ_EL3A, and BIOZ_EL3B are not available for voltage mode stimulation.

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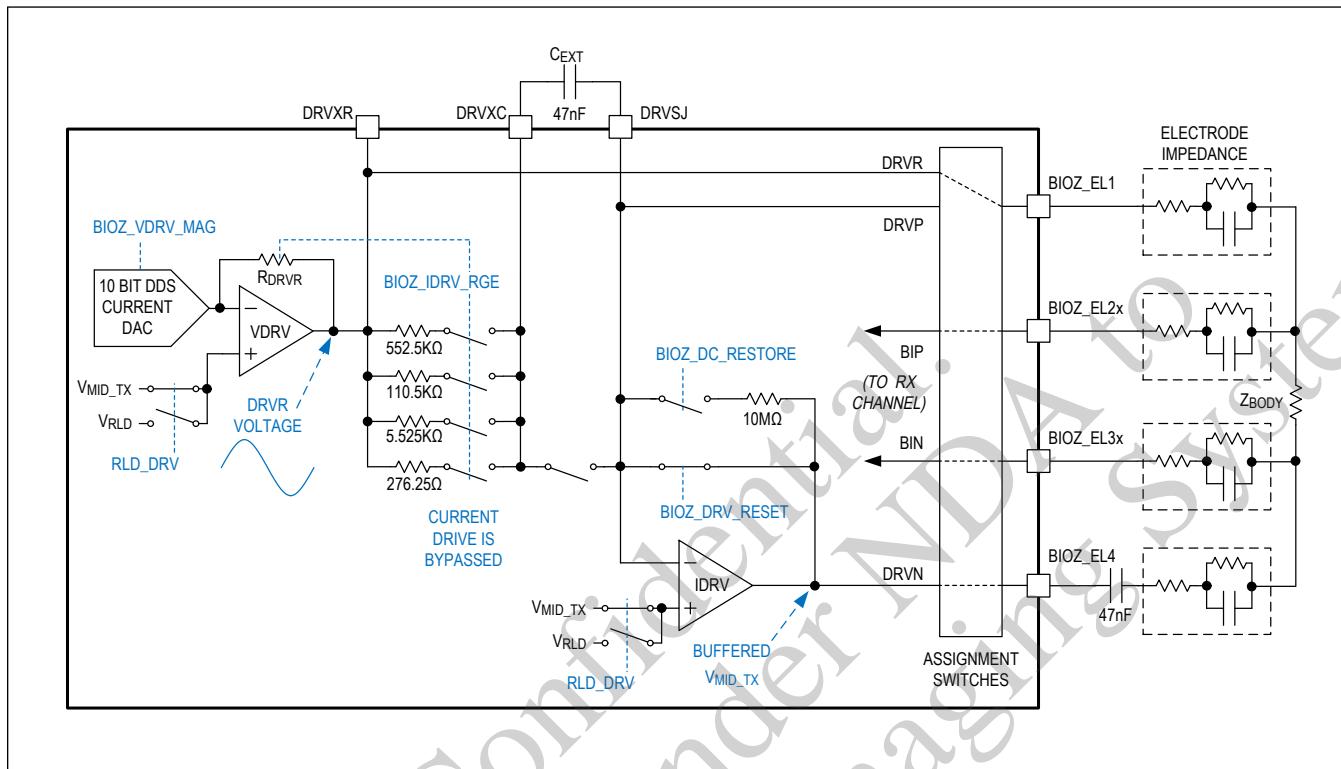


Figure 40. Bioimpedance Stimulus Generator Diagram—Sine-Wave Voltage Mode

Square-Wave Voltage (H-Bridge) Stimulus

To select H-bridge square-wave voltage stimulus mode, set `BIOZ_DRV_MODE[1:0](0xA2)` to 0x2 and `RESP_EN` to 0. [Figure 41](#) shows the signal path for H-bridge mode. An H-bridge is used to alternately switch AVDD and then AGND onto `BIOZ_EL1`, and AGND and then AVDD onto `BIOZ_EL4`. In this case, the DDS circuit and IDRIV amplifier are disabled and the range resistor switches are all opened. When using this mode of operation, there must be series precision resistors in both the `BIOZ_EL1` and `BIOZ_EL4` paths to limit the current to $V_{AVDD} / (2 \times R_{SERIES})$. The current from the H-bridge flows through R_{SERIES_EL1} , a 1st electrode impedance, body impedance with its variable component, a 2nd electrode impedance, and R_{SERIES_EL4} . The applied patient current is set by selecting the appropriate R_{SERIES} resistance value. The two R_{SERIES} resistors and the body form an impedance divider, and the portion of the AC voltage signal across the body impedance is sensed by the bioimpedance AFE receive channel with the inputs selected from `BIOZ_EL2A`, `BIOZ_EL2B`, `BIOZ_EL3A`, and `BIOZ_EL4B`. `DRV_P` must be assigned to `BIOZ_EL1` and `DRV_N` must be assigned to `BIOZ_EL4`.

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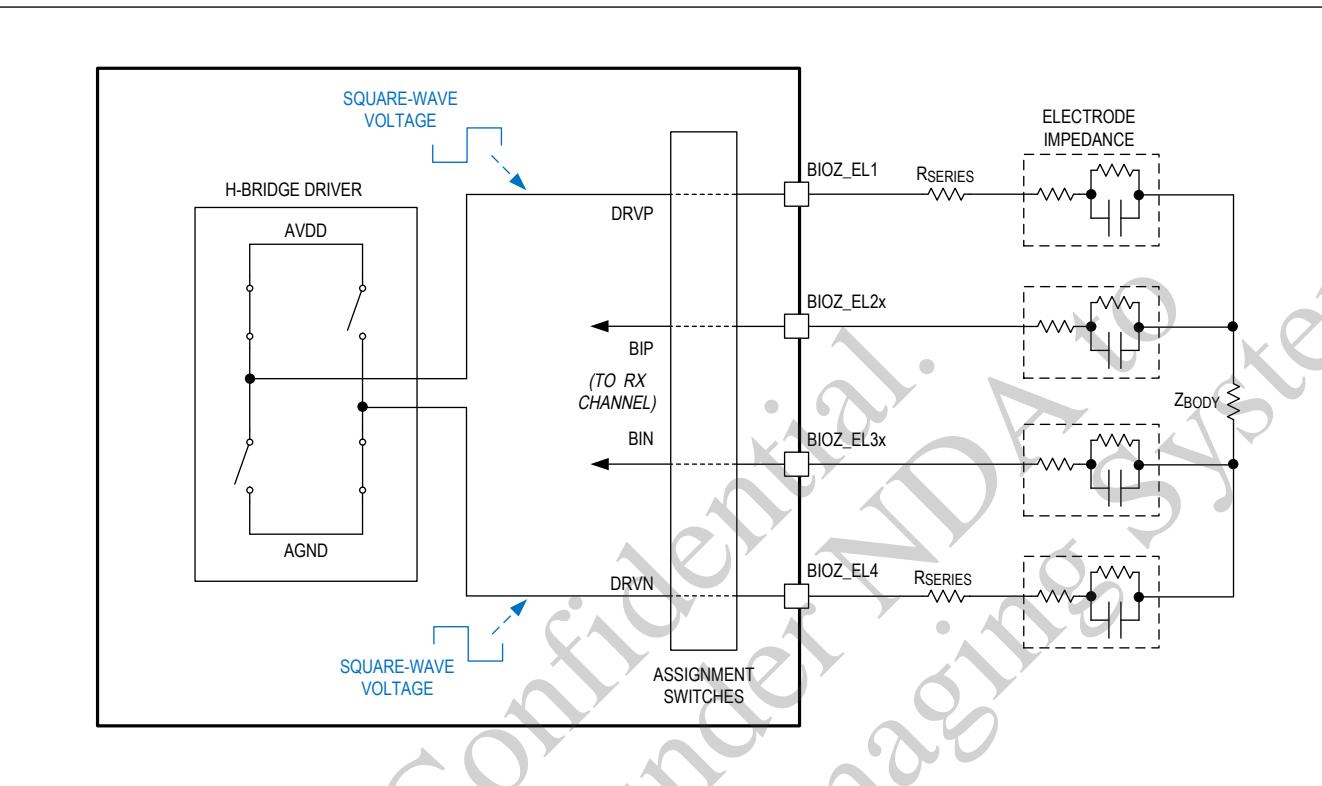
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Figure 41. Bioimpedance Stimulus Generator Diagram—H-Bridge Square-Wave Voltage Mode

BioZ Receive Channel

[Figure 42](#) illustrates the BioZ receive channel block diagram. The channel is comprised of an input MUX, a bypassable and programmable analog high-pass filter, an instrumentation amplifier with programmable gain, demodulator, anti-alias filter, another programmable gain amplifier, and an analog-to-digital converter (ADC). The input MUX includes several features such as EMI filtering, programmable electrode assignment switches, lead biasing, DC lead-off detection, and ultra-low power lead-on detection.

The MAX86178 BioZ receive channel instrumentation amplifier (INA) provides low-noise amplification of the differential signal, rejects differential DC voltage due to the analog high-pass filter, rejects common-mode interference such as AC mains interference, and provides high input impedance to guarantee high CMRR even in the presence of severe electrode impedance mismatch. The total channel gain can be set to 1V/V, 2V/V, 5V/V, or 10V/V, and is set by `BIOZ_GAIN[1:0](0xA5)`, which affects both the INA gain and the PGA gain. The demodulator multiplies the received signal by a square wave with the same frequency f_{STIM} to down-convert the measurement frequency to DC. The phase of the demodulator f_{DEMOD} signal is chosen by `BIOZ_EN[1:0](0xA0)`. Following the PGA amplifier is a 2-pole, active low-pass anti-aliasing filter (AAF) with a 600Hz, -3dB frequency that provides approximately 57dB of attenuation at half the sigma-delta ADC input sampling rate (`BIOZ_ADC_CLK`). After the AAF is a 20-bit sigma-delta ADC. The effective bits of the ADC depend on the value of `BIOZ_ADC_OSR[5:3](0xA0)` with higher oversampling ratios resulting in more effective bits (see the [Electrical Characteristics](#) sections).

When AC coupling the BioZ receive channel or using the internal analog high-pass filter (HPF), the AC differential range is $> 1000\text{mV}_{\text{P-P}}$ with an INA gain of 1V/V. When DC-coupling the bioimpedance receive channel, the usable common-mode range of the bioimpedance receive channel is 0.5V to $\text{V}_{\text{AVDD}} - 0.75\text{V}$. Internal lead biasing is used to achieve these requirements (see the [BioZ Lead Bias](#) section).

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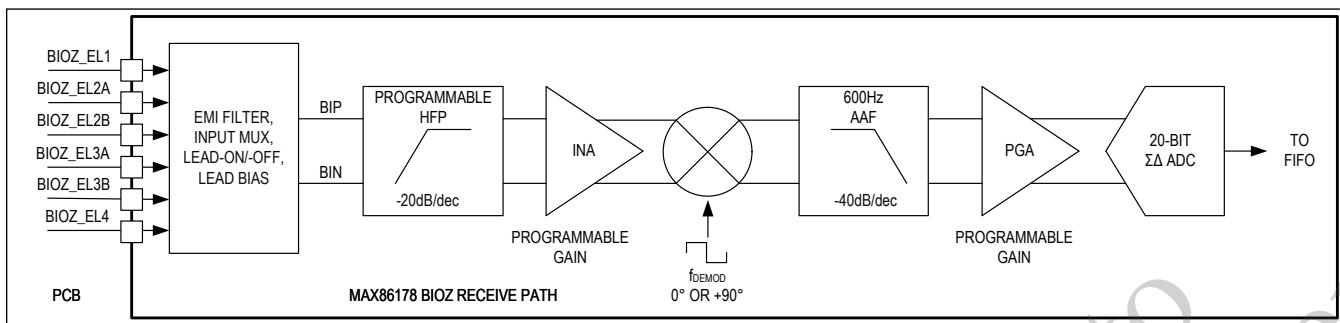
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Figure 42. BioZ Receive Channel

BioZ Decimation and Digital Filters

The decimation filter is used along with the sigma-delta modulator within the ADC to reduce the sample rate of the BIOZ_ADC_CLK to a smaller programmable output rate (SR_BIOZ). The decimation filter has a SINC3 response with a corner frequency at approximately $0.26 \times SR_BIOZ$. The decimation filter is followed by a programmable digital filter to implement HPF and LPF selections.

The programmable digital high-pass filter scales with the ADC clock rate and can be set to either $0.00025 \times SR_BIOZ$, $0.002 \times SR_BIOZ$, or bypassed by setting BIOZ_DHPF[7:6](0xA1). Similarly, the programmable digital low-pass filter scales with the ADC clock rate and can be set to $0.005 \times SR_BIOZ$, $0.02 \times SR_BIOZ$, $0.08 \times SR_BIOZ$, $0.25 \times SR_BIOZ$, or bypassed using BIOZ_LPF[5:3](0xA1).

Converting Digitized BioZ Samples to Voltage and Impedance

BioZ channel samples are recorded in 20-bit left-justified 2's complement format. These samples represent the voltage at the ADC, which has passed through the INA, demodulator, PGA, and AAF. The INA and PGA apply a combined gain of 1V/V, 2V/V, 5V/V, or 10V/V as set by BIOZ_GAIN[1:0](0xA5). The demodulator multiplies the incoming sine wave or square wave by a square wave with the same frequency as f_{STIM} . The AAF is a two-pole low-pass filter with a 600Hz corner frequency. The decimation filter in the ADC has a bandwidth of approximately $0.26 \times SR_BIOZ$.

When performing absolute impedance measurements for applications such as BIA/BIS and GSR/EDA, the DC component of the demodulated voltage represents the measured impedance. When $f_{STIM} \gg 600\text{Hz}$ or when $SR_BIOZ \ll f_{STIM}$, the harmonics resulting from the square-wave demodulation can be ignored, and the digitized samples represent the DC component of the demodulated voltage. For sine-wave stimulation, the square-wave demodulation applies a scaling factor of $2 / \pi$ to the DC component, as shown in Figure 43.

The DC component of the demodulated voltage is converted by the ADC, and represents load impedance in current-stimulus mode according to the following equations.

$$\text{Sine-Wave Stimulus: } Z_{BIOZ}(\Omega) = \text{ADC_COUNT} \times V_{REF_ECG} / (2^{19} \times \text{BIOZ_GAIN} \times 2 / \pi \times I_{MAG})$$

$$\text{Square-Wave Stimulus: } Z_{BIOZ}(\Omega) = \text{ADC_COUNT} \times V_{REF_ECG} / (2^{19} \times \text{BIOZ_GAIN} \times I_{MAG})$$

where,

ADC_COUNT = ADC counts in signed magnitude format

V_{REF_ECG} = 1V (typ, see the [Electrical Characteristics](#) section)

BIOZ_GAIN = Options 1V/V, 2V/V, 5V/V, and 10V/V.

I_{MAG} = Stimulus current in A_{PK} set by BIOZ_VDRV_MAG[5:4](0xA2) and BIOZ_IDRV_RGE[3:2](0xA2), or RESP(CG_MAG[6:4](0xB1) and RESP(CG_MAG_4X[7](0xB1))

The input-referred voltage amplitude can likewise be calculated with the following equations.

$$\text{Sine-Wave Stimulus: } V_{BIOZ}(V_{PK}) = \text{ADC_COUNT} \times V_{REF_ECG} / (2^{19} \times \text{BIOZ_GAIN} \times 2 / \pi)$$

$$\text{Square-Wave Stimulus: } V_{BIOZ}(V_{PK}) = \text{ADC_COUNT} \times V_{REF_ECG} / (2^{19} \times \text{BIOZ_GAIN})$$

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For voltage stimulus modes, the impedance can be calculated from an impedance divider with the series resistors.

For respiration and ICG applications, the signal of interest is contained in the time-varying impedance signal, so the DC component is not as important. The respiration signal band is typically 0.05Hz to 4Hz, and the ICG signal band is typically DC to 64Hz. For these applications, the BioZ sample rate and digital filters can be adjusted to select the signal band of interest, considering the decimation filter $0x26 \times SR_BIOZ$ bandwidth. The above impedance or voltage calculations can be performed for these applications, but these conversions are not strictly necessary.

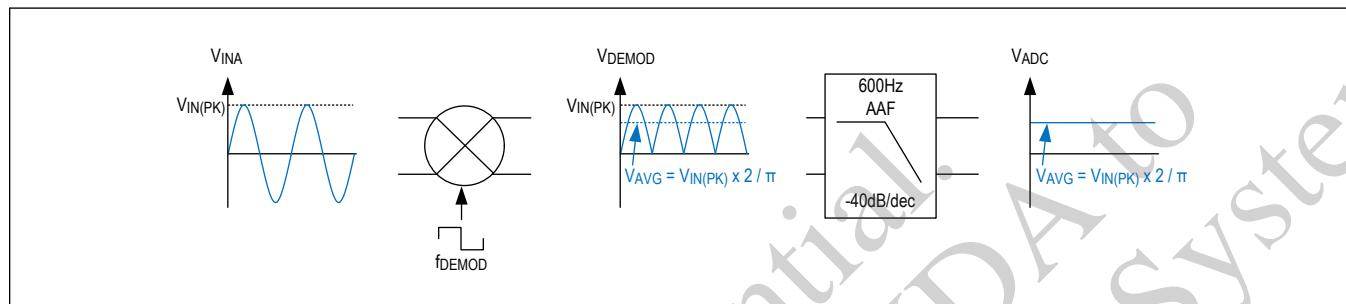


Figure 43. Square-Wave Demodulation for a Sine-Wave Stimulus (INA and PGA Gain Not Shown)

BioZ Noise Measurements

[Table 21](#) shows the input referred voltage noise of the BioZ receive channel measured with the inputs shorted and the frequency settings shown in [Table 22](#) and [BIOZ_AHPF\[7:4\]\(0xA5\) = 5kHz](#).

Table 21. BioZ Receive Channel Input-Referred Noise, 256spS

BIOZ_GAIN (V/V)	BIOZ_DLPF (Hz)	NOISE (μV_{RMS})	NOISE (μV_{P-P})	SNR (dB)	ENOB
1	bypass	10.05	51.50	90.9	14.8
	1.28	2.44	7.63	103.2	16.9
	5.12	4.17	17.17	98.6	16.1
	20.48	5.75	28.61	95.8	15.6
	64	9.36	47.68	91.5	14.9
2	bypass	4.41	25.75	98.1	16.0
	1.28	1.88	4.77	105.5	17.2
	5.12	1.98	6.68	105.0	17.2
	20.48	3.08	14.31	101.2	16.5
	64	4.86	26.70	97.2	15.9
5	bypass	2.73	14.11	94.3	15.4
	1.28	0.97	2.67	103.3	16.9
	5.12	0.84	4.58	104.5	17.1
	20.48	1.70	8.39	98.4	16.0
	64	2.27	12.21	95.9	15.6
10	bypass	2.41	12.21	89.4	14.6
	1.28	0.76	2.67	99.4	16.2
	5.12	0.94	3.62	97.5	15.9
	20.48	1.28	6.29	94.9	15.5
	64	1.21	6.10	95.3	15.5

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Note: SNR = $20\log\left(\frac{V_{IN(RMS)}}{V_{N(RMS)}}\right)$, ENOB = (SNR - 1.76)/6.02

Note: $V_{IN(P-P)} = (2V_{P-P} / \text{BIOZ_GAIN})$ or $1V_{P-P}$, whichever is smaller. This represents the maximum signal of the receive channel: $V_{IN(RMS)} = \frac{V_{IN(P-P)}}{2\sqrt{2}}$

Table 22. Input-Referred Noise Frequency Settings

REF_CLK (Hz)	M	PLL_CLK (Hz)	BIOZ_KDIV	BIOZ_DAC_OSR	F_BIOZ (Hz)	BIOZ_NDIV	ADC_OSR	INTEGRATION CYCLES	ADC_SR (sps)	BIOZ_AHPF (kHz)
32768	256	8388608	1	128	65536	256	128	256	256	5

BioZ Input/Output MUX

The BioZ input MUX shown in [Figure 44](#) has many helpful circuits to support BioZ applications. For the electrodes assigned to the receive channel, this circuitry contains integrated EMI protection, DC lead-off detect current sources, lead biasing, programmable resistor loads as well as a programmable high-pass filter (HPF). The electrodes assigned to provide the stimulus have compliance monitors. The input/output MUX assigns physical electrodes to the available BioZ channel functions. For example, BIOZ_EL1 can be assigned to DRVP (positive drive), BIOZ_EL2B to BIP (positive input), BIOZ_EL3B to BIN (negative input), and BIOZ_EL4 to DRVN (negative drive). The BIOZ_EL2 and BIOZ_EL3 electrode inputs have A and B pins, allowing one board to support both GSR/EDA and BIA/BIS in the same application. In this case, the A inputs should be used for GSR/EDA and need external AC coupling capacitors, and the B inputs should be used for BIA/BIS and do not need external capacitors. The MUX also has 4-wire calibration port (CAL1 to CAL4) for in-situ calibration to one or more precision external resistors with more details shown in [Figure 50](#).

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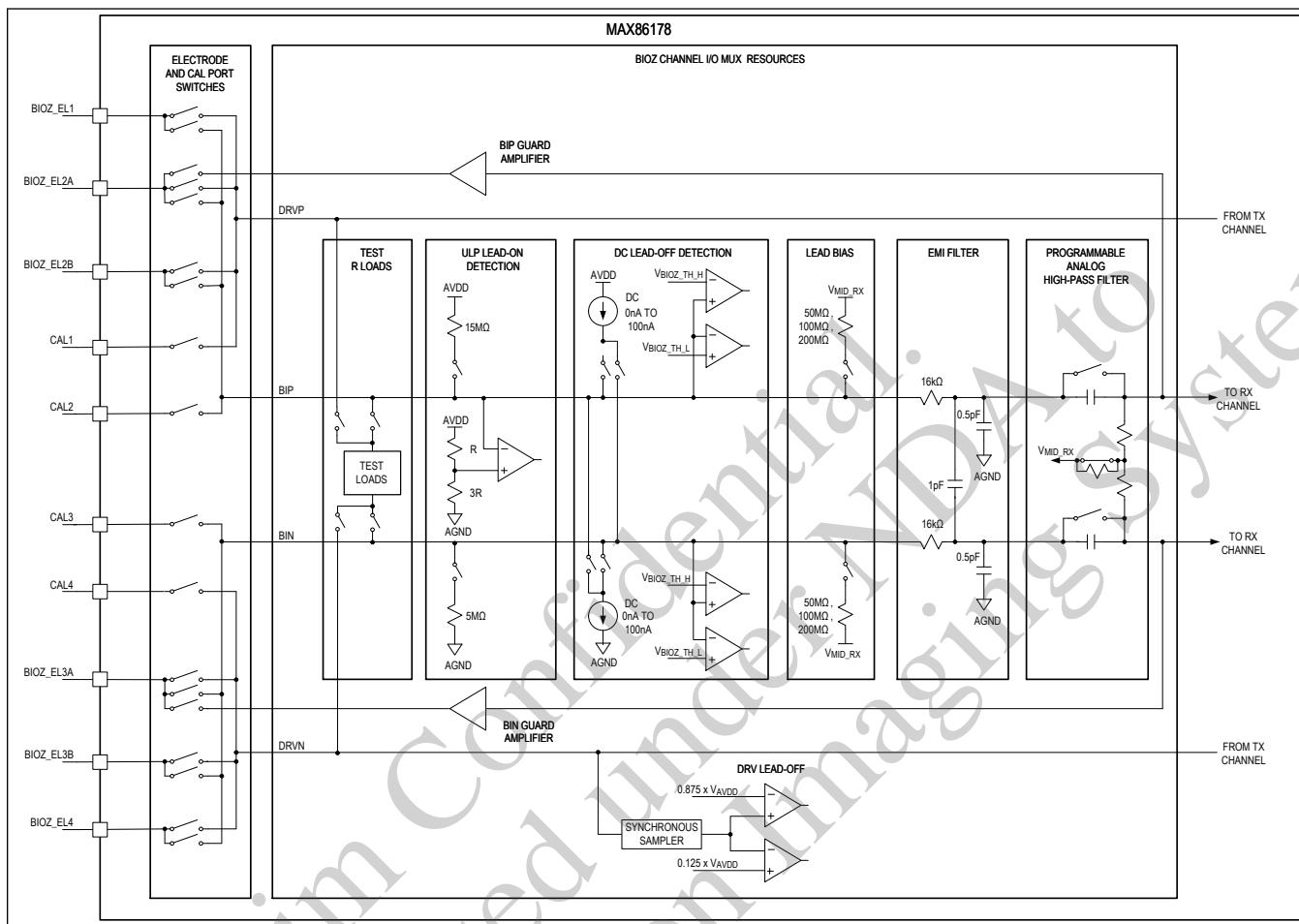


Figure 44. BioZ Input/Output MUX

BioZ EMI Filtering and ESD Protection

The EMI filter on the BIP and BIN internal inputs consists of $16\text{k}\Omega$ resistors connected to BIP and BIN followed by a 1pF differential-mode capacitor and 0.5pF common-mode capacitors. These form a single pole, low-pass, differential- and common-mode filter with the differential-mode pole located at approximately 4MHz and the common-mode pole located at approximately 20MHz . Additional external EMI filters are not recommended for applications with dry electrodes in order to maintain high input impedance, which helps mitigate the impact of electrode-impedance mismatch. With lower input impedance, the electrode impedance mismatch translates into increased conversion of common-mode voltage to differential-mode voltage. Applications with wet electrodes can use external EMI filters with high-precision components to minimize electrode impedance mismatch. In this case, the differential-mode pole can be set as low as the desired signal bandwidth, and the common-mode pole is set at least a decade below the AM radio band (535kHz).

The BIOZ_ELx and CALx pins have ESD protection compliance with 2kV HBM. For IEC ESD compliance, external ESD diodes must be added (see [Typical Applications Circuits](#)).

BioZ Lead Bias

The MAX86178 limits the BIP and BIN DC input range to 0.5V to $\text{V}_{\text{AVDD}} - 0.75\text{V}$. This range can be maintained either through external or internal lead biasing.

Internal DC lead biasing consists of $50\text{M}\Omega$, $100\text{M}\Omega$, or $200\text{M}\Omega$ selectable resistors from BIP and BIN to either $\text{V}_{\text{MID_RX}}$

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or V_{RLD} that bias the MAX86178 to the proper potential relative to the body in battery-powered systems. By matching the voltage of $VMID_RX$ to the body, lead bias ensures that the common-mode input voltage of the BIP and BIN are within the DC input range of the BioZ receive channel. Lead bias is only effective when the MAX86178 system has high galvanic isolation from earth ground. See $BIOZ_RBIAS_VALUE[3:2](0xB4)$ to select a resistance value, and $EN_BIOZ_RBIAS[1](0xB4)$ and $EN_BIOZ_RBIASN[0](0xB4)$ to enable lead bias. The lead bias voltage is selected by $RLD_RBIAS[5](0x92)$. Selecting V_{RLD} (the output of the right leg drive common mode averager) as the lead bias voltage can improve the BioZ receive channel CMRR without needing a dedicated RLD electrode. If the ECG and BioZ receive channels share electrodes, only one channel should have lead bias enabled.

Programmable BioZ Resistor Load

The programmable resistive load allows a built-in self-test of the current generator (CG) and the BioZ receive channel. Refer to [Figure 45](#) for implementation details. For BIA/BIS applications, there is a selection of low-impedance loads from which to choose: 200 Ω , 400 Ω , 800 Ω , and 5k Ω . For GSR/EDA applications, there is a selection of high-impedance loads from which to choose: 25k Ω , 100k Ω , 500k Ω , and 1M Ω .

See register fields $BMUX_RSEL[7:6](0xAA)$, $BMUX_BIST_EN[5](0xAA)$, $BMUX_GSR_RSEL[7:6](0xAB)$ and $GSR_LOAD_EN[5](0xAB)$ to set the resistor value.

The BIA/BIS resistive loads can also be used as internal calibration resistors. See $BIST_R_ERROR[7:0](0xAD)$ for details.

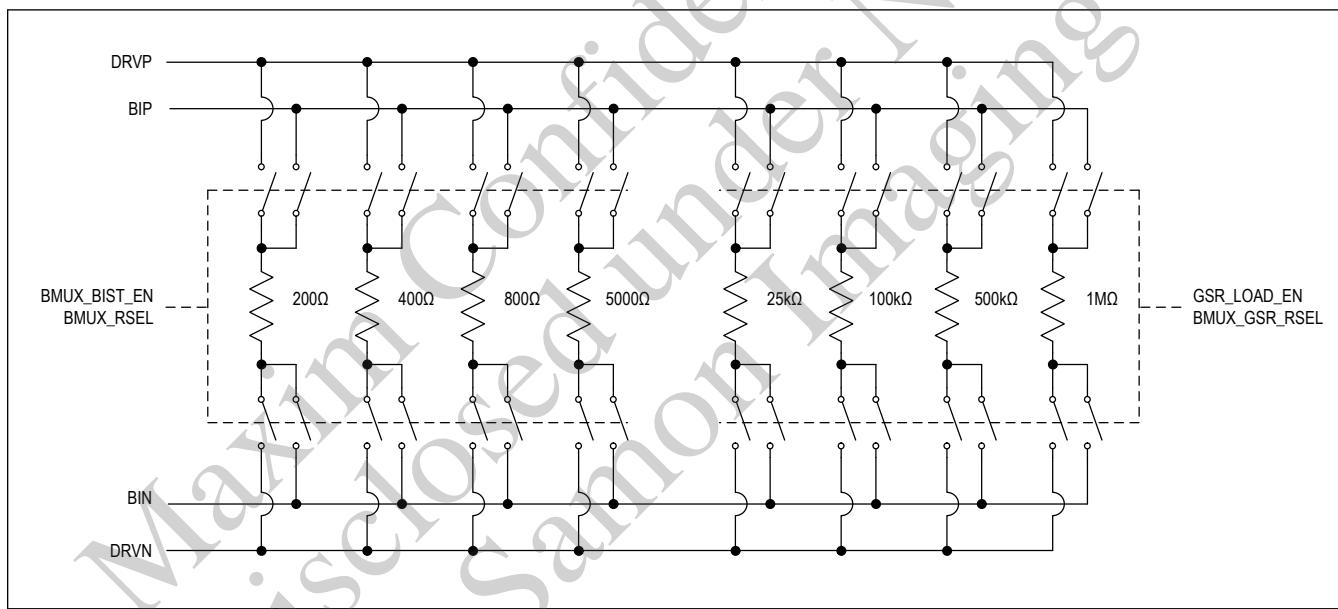


Figure 45. Programmable Resistor Load

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BioZ Lead-Off Detection

The MAX86178 has three techniques that can be used for determining if there is one or more electrode lead-off condition(s). Lead-off is a term used to indicate that one or more electrodes used during the bioimpedance measurements has/have become open. In other words, the electrode-tissue interface impedance is too high and the bioimpedance measurement might become unreliable. These three lead-off techniques are DC lead-off, DRV lead-off, and programmable thresholds (AC lead-off) circuit. The relevant techniques depend on the electrode configuration (bipolar or tetrapolar) and which electrode is off. The first two techniques use circuits that are contained within the I/O MUX circuitry and the final technique is accomplished using digital circuitry after the receive channel ADC.

There is also an ultra-low power (ULP) lead-on detect circuit that is only intended to be used to wake up the microcontroller that is controlling the MAX86178. This circuit should never be used while making bioimpedance

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measurements and should not be confused with the lead-off circuit functionality.

The DC lead-off detection circuit provides matched source and sink currents that are injected into the BIP and BIN electrodes. This current, when the electrodes are connected properly, flows through a first electrode-tissue interface, through the body and then through a second electrode-tissue interface. This current flow develops a differential voltage across the two input pins. If one or both electrode-tissue interfaces has a poor connection with the body, then this current path has much higher impedance and this voltage is large. If the electrodes are properly connected, then this voltage is small. The DC lead-off circuitry provides two sets of dual comparators to test if the differential voltage is too high.

This feature is enabled by EN_BIOZ_LOFF[6](0xB0), and the stimulus current magnitude (5nA to 100nA) is set by BIOZ_LOFF_IMAG[2:0](0xB0). The current magnitude should be chosen to match the expected acceptable maximum impedance of the specific electrodes used in the application.

When using DC lead-off detection, the microcontroller and user can be alerted if the viability of the electrode tissue interface electrodes has been compromised by dual comparators indicating if BIP or BIN voltages exceeds either a programmable high limit or a programmable low limit. The dual comparators can be used to generate a hardware interrupt if the DC lead-off voltage exceeds the threshold (i.e., a minimum continuous violation) for an interval exceeding either 115ms or 140ms depending on the setting of FCLK before asserting one of the BIOZ_LOFF interrupt flags. The comparator threshold is controlled by BIOZ_LOFF_THRESH[3:0](0xB1). See [Figure 46](#) for an example of the threshold and timing behavior.

For applications without external AC-coupling capacitors, the DC lead-off detection is applied directly to the BIP and BIN electrodes as shown in [Figure 47](#). However, when external AC-coupling capacitors are used, such as in GSR/EDA applications, DC lead-off detection must be applied externally. In this case, BIP and BIN must be assigned to BIOZ_EL2A and BIOZ_EL3A, and DC lead-off detection is applied externally through BIOZ_EL2B and BIOZ_EL3B. To enable this feature, BIOZ_EL2B and BIOZ_EL3B must be connected outside of the AC-coupling capacitors as shown in [Figure 48](#), and EN_EXT_BIOZ_LOFF[5](0xB0) must be enabled in addition to EN_BIOZ_LOFF.

The DRV lead-off circuit checks the BioZ current stimulus path to determine whether or not the DRVP and DRVN connections are in place when using a tetrapolar electrode configuration. In this case, one or both of the DRVP and DRVN electrodes are compromised and are not reliably connected to the body. When the impedance between the DRVP and DRVN electrodes becomes too high, the magnitude of this amplifier output signal starts to approach one or both rails (AVDD or AGND), getting very close to amplifier saturation. When the DRV lead-off circuit is enabled, a sample-and-hold circuit followed by a dual-comparator samples the IDRVP amplifier output signal and determines if it is outside of $0.125 \times V_{AVDD}$ and $0.875 \times V_{AVDD}$. If it is, the comparator trips and a DRV lead-off condition is flagged. To turn on the DRV lead-off circuit, set EN_BIOZ_DRV_OOR[4](0xB0) to 1. An out-of-range condition must be exceeded for either 125ms or 128ms, depending on CLK_FREQ_SEL[5](0x1D), before the BIOZ_DRV_OOR status bit is asserted.

The BioZ threshold (AC lead-off) detection circuit monitors the output of the BioZ ADC with programmable high or low thresholds, and is enabled by EN_BIOZ_THRESH[0](0xA1). The thresholds are set by BIOZ_LO_THRESH[7:0](0xA8) and BIOZ_HI_THRESH[7:0](0xA9). If the digitized output remains over BIOZ_HI_THRESH or under BIOZ_LO_THRESH for longer than 128ms, then the BIOZ_OVER[6](0x04) or BIOZ_UNDR[5](0x04) are asserted. This behavior is described graphically in [Figure 49](#).

[Table 23](#) shows the lead-off techniques suitable for each electrode configuration and lead-off condition. The internal HPF is suitable for stimulus frequencies above 1kHz, and external capacitors are need for stimulus frequencies under 1kHz.

Table 23. BioZ Lead-Off Cases

CONFIGURATION	CONDITION	DRV	DRV	BIP	BIN	MEASURED SIGNAL	LEAD-OFF TECHNIQUES
Bipolar, internal HPF	DRVP/BIP off	DDS sine	large signal	DDS sine	large signal	large	DC Lead-Off, DRVN Lead-Off, AC Lead-Off (Over)
Bipolar, internal HPF	DRVP/BIN off	DDS sine	large signal	DDS sine	large signal	large	DC Lead-Off, DRVN Lead-Off, AC Lead-Off (Over)
Bipolar, external capacitors	DRVP/BIP off	DDS sine	large signal	DDS sine	large signal	large	DRVN Lead-Off, AC Lead-Off (Over)
Bipolar, external capacitors	DRVN/BIN off	DDS sine	large signal	DDS sine	large signal	large	DRVN Lead-Off, AC Lead-Off (Over)

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CONFIGURATION	CONDITION	DRV _P	DRV _N	BIP	BIN	MEASURED SIGNAL	LEAD-OFF TECHNIQUES
Tetrapolar, internal HPF	DRV _P off	DDS sine	large signal	large signal	large signal	indeterminant	DRV _N Lead-Off
Tetrapolar, internal HPF	DRV _N off	DDS sine	railed	railed	railed	railed	DRV _N Lead-Off, AC Lead-Off (Over)
Tetrapolar, internal HPF	BIP off	V _{MID_TX}	normal	V _{MID_RX}	normal	1/2 of normal size	DC Lead-Off, AC Lead-Off (Under)
Tetrapolar, internal HPF	BIN off	V _{MID_TX}	normal	V _{MID_RX}	V _{MID_RX}	near DC	DC Lead-Off, AC Lead-Off (Under)
Tetrapolar, internal HPF	BIP and BIN off	V _{MID_TX}	normal	V _{MID_RX}	V _{MID_RX}	near DC	DC Lead-Off, AC Lead-Off (Under)
Tetrapolar, internal HPF	DRV _P and BIP off	DDS sine	large signal	V _{MID_RX}	large signal	large	DC Lead-Off, DRV _N Lead-Off, AC Lead-Off (Over)
Tetrapolar, internal HPF	DRV _P and BIN off	DDS sine	large signal	DDS sine	V _{MID_RX}	DDS sine magnitude	DC Lead-Off, DRV _N Lead-Off
Tetrapolar, internal HPF	DRV _N and BIP off	DDS sine	large signal	V _{MID_RX}	large signal	large	DC Lead-Off, DRV _N Lead-Off, AC Lead-Off (Over)
Tetrapolar, internal HPF	DRV _N and BIN off	DDS sine	large signal	DDS sine	V _{MID_RX}	DDS sine magnitude	DC Lead-Off, DRV _N Lead-Off
Tetrapolar, external capacitors	DRV _P off	DDS sine	large signal	large signal	DDS sine	large	DRV _N Lead-Off, AC Lead-Off (Over)
Tetrapolar, external capacitors	DRV _N off	DDS sine	large signal	large signal	large signal	indeterminant	AC Lead-Off (Over)
Tetrapolar, external capacitors	BIP off	V _{MID_TX}	normal	V _{MID_RX}	normal	DDS sine magnitude	DC Lead-Off
Tetrapolar, external capacitors	BIN off	V _{MID_TX}	normal	normal	V _{MID_RX}	DDS sine magnitude	DC Lead-Off
Tetrapolar, external capacitors	BIP and BIN off	V _{MID_TX}	normal	V _{MID_RX}	V _{MID_RX}	near DC	DC Lead-Off, AC Lead-Off (Under)
Tetrapolar, external capacitors	DRV _P and BIP off	DDS sine	large signal	V _{MID_RX}	large signal	large	DC Lead-Off, DRV _N Lead-Off, AC Lead-Off (Over)
Tetrapolar, external capacitors	DRV _P and BIN off	DDS sine	large signal	large signal	V _{MID_RX}	large	DC Lead-Off, DRV _N Lead-Off, AC Lead-Off (Over)
Tetrapolar, external capacitors	DRV _N and BIP off	DDS sine	large signal	V _{MID_RX}	DDS sine	DDS sine magnitude	DC Lead-Off
Tetrapolar, external capacitors	DRV _N and BIN off	DDS sine	large signal	DDS sine	V _{MID_RX}	DDS sine magnitude	DC Lead-Off

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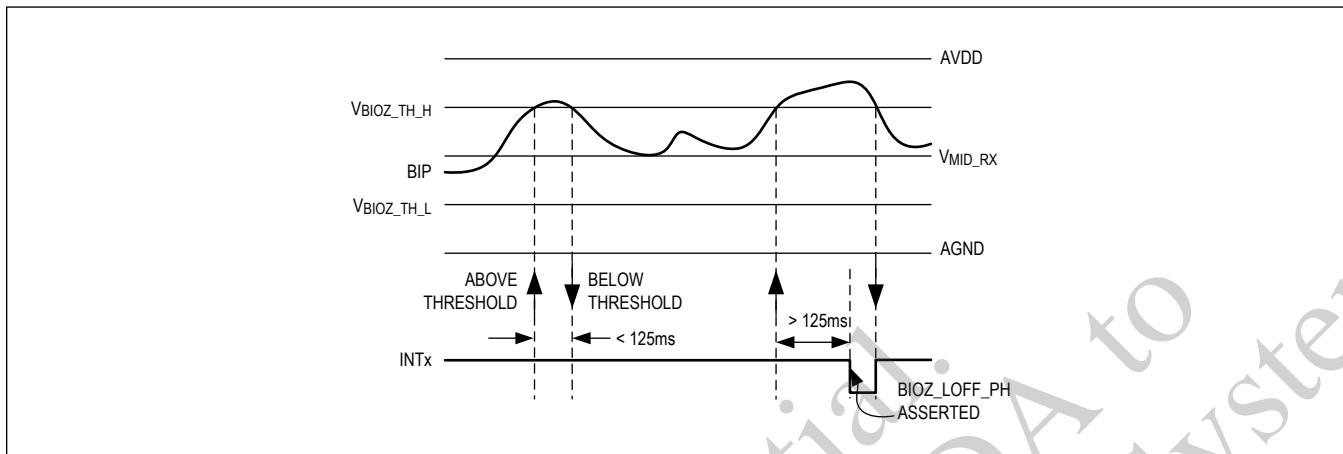


Figure 46. BioZ DC Lead-Off Behavior

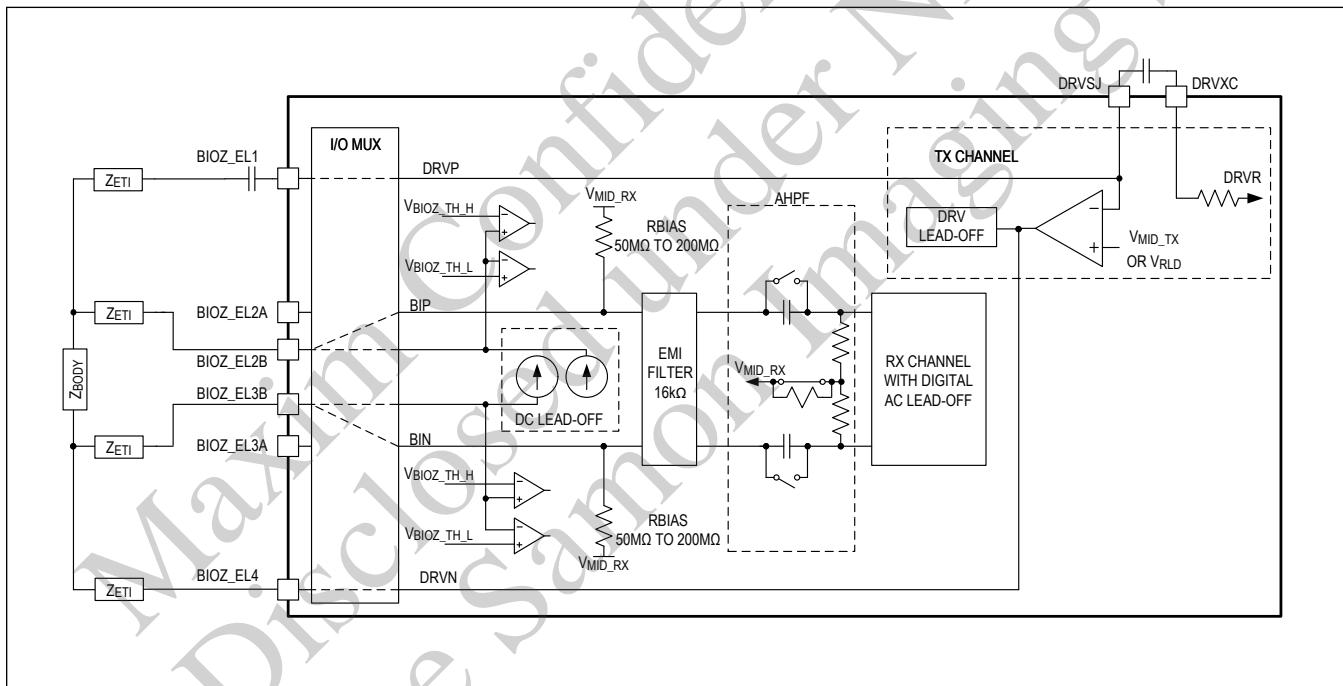


Figure 47. BioZ DC Lead-Off Detection with Internal Sense

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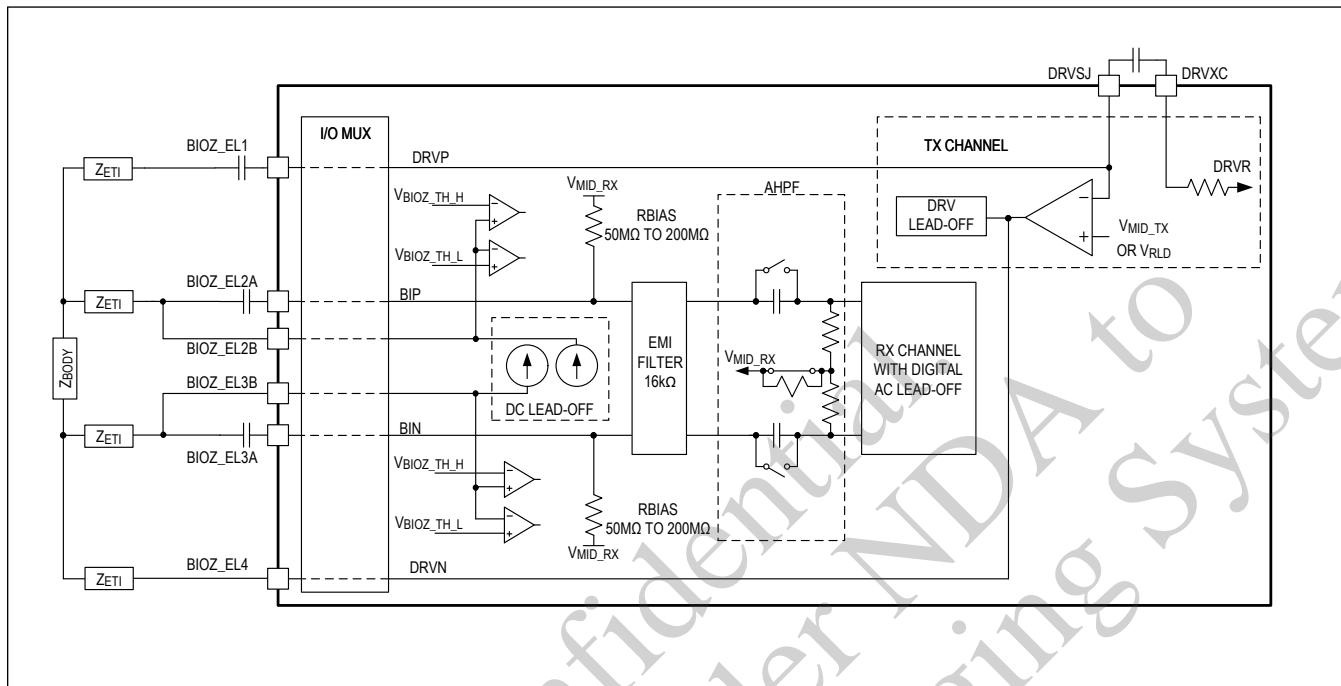


Figure 48. BioZ DC Lead-Off Detection with External Sense

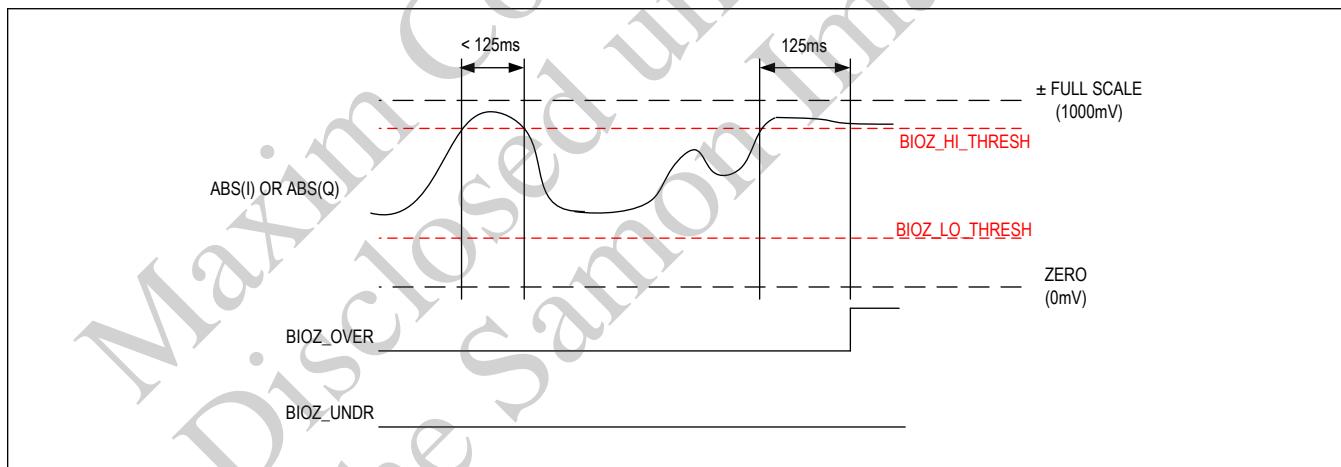


Figure 49. BioZ Threshold Behavior

BioZ Ultra-Low-Power (ULP) Lead-On Detection

The MAX86178 features an ultra-low-powered (ULP) lead-on detection circuit for the BioZ input electrodes. The BioZ channel must be disabled (`BIOZ_EN[1:0](0xA0) = 0x0`) when ULP lead-on detection is enabled.

The ULP lead-on detect circuit operates by pulling `BIN` low with a pulldown resistance of $5\text{M}\Omega$ (typ) and pulling `BIP` high with a pullup resistance of $15\text{M}\Omega$ (typ). A low-power comparator determines if `BIP` is pulled below $0.75 \times \text{AVDD}$ (typ), and asserts the `BIOZ_LON[7](0x05)` status bit if `BIP` remains below the threshold for at least 128ms. This circuit is shown in [Figure 44](#). Because this circuit relies on DC current flowing through the electrodes, it does not work when external

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AC-coupling capacitors are used on the pins assigned to BIP and BIN.

There are several conditions that can pull BIP below the threshold and trigger a lead-on status:

- The total impedance between BIP and BIN is below $40\text{M}\Omega$ (typ) due to both electrodes contacting the body.
- The total impedance between BIP and AGND is below $45\text{M}\Omega$ (typ) due to the the BIP electrode contacting a body that is coupled to AGND. For example, if the MAX86178 system is coupled to earth ground through a power or data cable, and the body is also coupled to earth ground, then a low-impedance path could pull the BIP electrode low.
- The ECGP electrode is contacting the body and has a large half-cell potential. The half-cell potential can push the ECGP voltage below the threshold.

If the BIOZ_LON interrupt is enabled by BIOZ_LON_EN1[7](0xC5) or BIOZ_LON_EN2[7](0xC9), an interrupt is generated to alert the host microcontroller of the lead-on condition. This interrupt allows the microcontroller to sleep when the system is not in use, and only wake up when the user touches the device electrodes. Upon receiving an interrupt and waking up, the microcontroller should read the BIOZ_LON status register to determine if a lead-on condition has occurred. Because of the bit's clear-on-read behavior, the status register should be read a second time to determine if the lead-on condition persists.

BioZ Calibration

The MAX86178 can be calibrated and can achieve impedance magnitude errors of 0.1% and impedance phase errors of 0.1° . The calibration can be performed at the factory by applying a precision resistor to the device electrodes, or on-board by connecting a precision resistor to the CALx pins. To achieve 0.1% accuracy, the calibration resistor(s) must have 0.05% tolerance, or be measured by an external reference with 0.05% accuracy. If using an on-board calibration, the reference resistor (R_{CAL}) should have a low temperature coefficient and should be connected to the calibration port as shown in [Figure 50](#). To connect the on-board R_{CAL} , assert BIOZ_MUX_EN[1](0xAA) and BIOZ_CAL_EN[0](0xAA).

The calibration consists of measuring the I and Q offsets and magnitude and phase coefficients at each measurement frequency, according to the following steps. Registers not mentioned in the steps below should be set to the values intended for use during measurement.

1. Set the synthesis frequency to the desired frequency.
2. Measure the I and Q offsets:
 1. Set the stimulus current magnitude to the minimum 16nA_{RMS} by setting BIOZ_VDRV_MAG[5:4](0xA2) and BIOZ_IDRV_RGE[3:2](0xA2) to 0x0.
 2. Enable BIOZ_DRV_RESET[5](0xA6) to apply a short-circuit across the load.
 3. Set BIOZ_EN[1:0](0xA0) to 0x1 to enable I phase measurement.
 4. Record data until the impedance signal has settled, and then record the average impedance in Ohms ($I_{\text{offset}} [\Omega]$). Settling time varies with sample rate, filter selections, and other settings.
 5. Set BIOZ_EN[1:0](0xA0) to 0x2 to enable Q phase measurement.
 6. Record data until the impedance signal has settled, and then record the average impedance in Ohms ($Q_{\text{offset}} [\Omega]$).
 7. Note: I_{offset} and Q_{offset} should be calculated using the intended measurement current magnitude, not the minimum 16nA_{RMS} .
3. Measure the calibration resistor I and Q impedances:
 1. Set the stimulus current to the desired value by adjusting BIOZ_VDRV_MAG[5:4](0xA2) and BIOZ_IDRV_RGE[3:2](0xA2).
 2. Disable BIOZ_DRV_RESET[5](0xA6).
 3. Set BIOZ_EN[1:0](0xA0) to 0x1 to enable I phase measurement.
 4. Record data until the impedance signal has settled, and then record the average impedance in Ohms ($I_{\text{resistor}} [\Omega]$).
 5. Set BIOZ_EN[1:0](0xA0) to 0x2 to enable Q phase measurement.
 6. Record data until the impedance signal has settled, and then record the average impedance in Ohms ($Q_{\text{resistor}} [\Omega]$).
4. Subtract the offsets from the resistor measurements:
 1. $I_{\text{calibration}} [\Omega] = I_{\text{resistor}} - I_{\text{offset}}$
 2. $Q_{\text{calibration}} [\Omega] = Q_{\text{resistor}} - Q_{\text{offset}}$
5. Calculate the calibration magnitude and phase coefficients:

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1. Mag_calibration [Ω] = $\sqrt{I_{\text{calibration}}^2 + Q_{\text{calibration}}^2}$
2. Mag_coef = Mag_calibration / R_{CAL}
3. Phase_coef [°] = arctan(Q_{calibration} / I_{calibration}) × 180° / π

To apply the calibration coefficients to a measured impedance, follow the steps below.

1. Measure I and Q load impedances (I_{load} [Ω] and Q_{load} [Ω]).
2. Subtract the offsets from the load impedances:
 1. I_{load-offset} [Ω] = I_{load} - I_{offset}
 2. Q_{load-offset} [Ω] = Q_{load} - Q_{offset}
3. Calculate the load impedance magnitude and phase:
 1. Mag_{load} [Ω] = $\sqrt{I_{\text{load-offset}}^2 + Q_{\text{load-offset}}^2}$
 2. Phase_{load} [°] = arctan(Q_{load-offset} / I_{load-offset}) × 180° / π
4. Apply the calibration coefficients:
 1. Mag_{calibrated} [Ω] = Mag_{load} / Mag_{coef}
 2. Phase_{calibrated} [°] = Phase_{load} - Phase_{coef}
 3. I_{calibrated} [Ω] = Mag_{calibrated} × cos(Phase_{calibrated} × π / 180°)
 4. Q_{calibrated} [Ω] = Mag_{calibrated} × sin(Phase_{calibrated} × π / 180°)

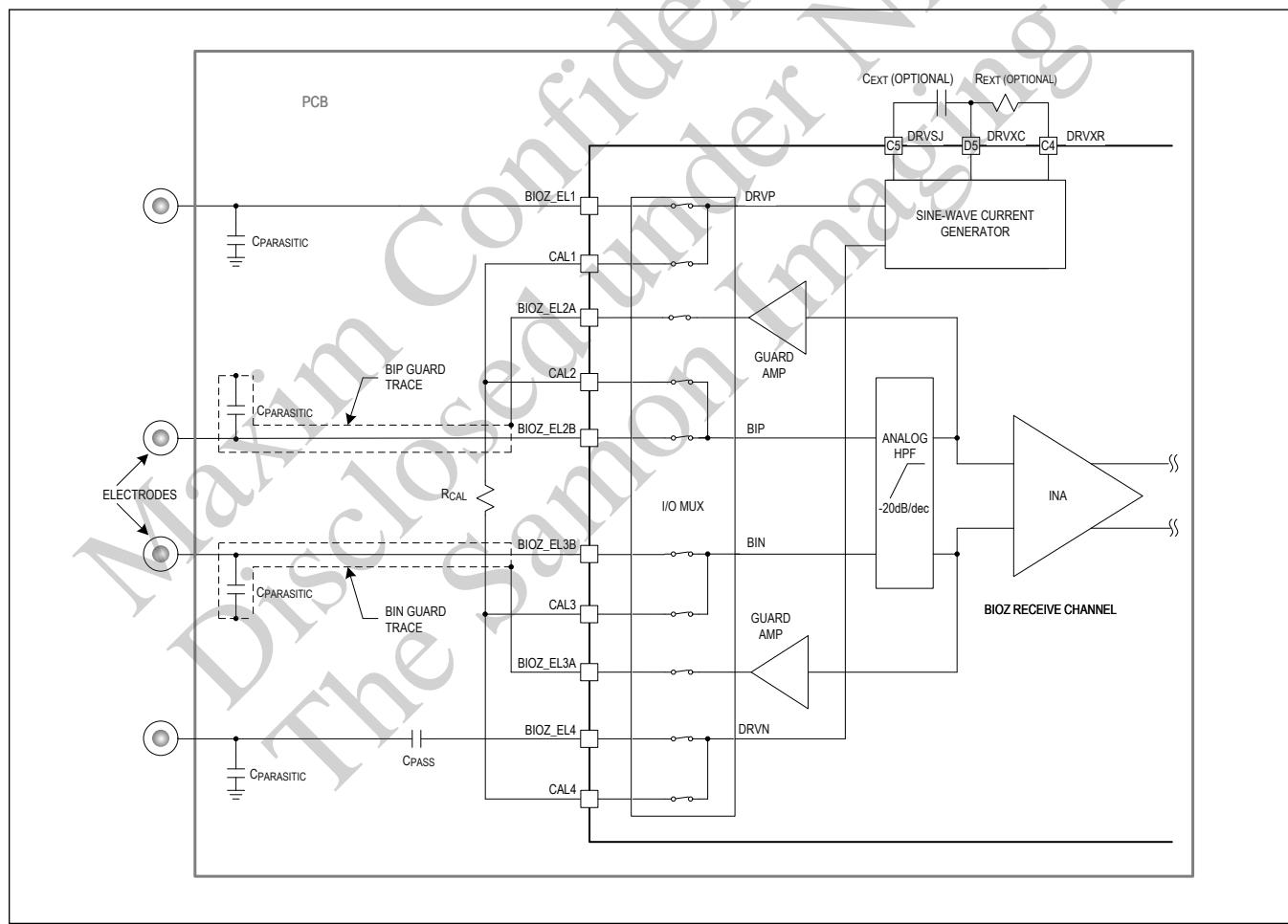


Figure 50. Calibration Port Connections

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The parasitic capacitance on the pins assigned to DRVP and DRVN can be calibrated out using the procedure described above. However, the parasitic capacitances on the pins assigned to BIP and BIN are more difficult to manage. The MAX86178 has two features that can be used to minimize the effect of these receive-channel parasitic capacitances.

First, it is important to realize that differences in BIP and BIN electrode tissue interface impedances working against these parasitic BIP and BIN capacitances can create phase accuracy issues, for instance, if the two PCB traces used to route BIP and BIN to the MAX86178 are carefully managed so that their parasitic capacitances are nearly equal, but the BIP electrode has a higher electrode tissue interface impedance than the BIN electrode. In such a case, the BIP side has more phase lag than the BIN side, creating a potential source of inaccuracy.

This problem can be mitigated by use of driven guard amplifiers and BIP and BIN guard traces. The BIP and BIN driven guard amplifiers can be enabled using EN_EXT_INLOAD[1](0xAB). The outputs of the BIP and BIN guard amplifiers are offered at pins BIOZ_EL2A and BIOZ_EL3A, respectively. Guard traces remove the effect of the parasitic PCB capacitances by driving a guard signal, that moves at the same frequency, amplitude, and phase as the input signal of interest; one can then use these guard signal routes to surround the BIP and BIN nets, usually parallel to the nets and on both sides; since there is no AC voltage drop across these parasitic capacitances, there is no associated AC currents needed to charge or discharge them.

To help mitigate the effects of parasitic capacitances within the MAX86178 itself, assert the EN_INT_INLOAD[0](0xAB), which enables an inverse capacitive load on each input.

FIFO Description

The FIFO holds a maximum of 256 samples and supports various data types from the ECG, PPG, and BioZ channels. Each sample in the FIFO is three bytes wide and contains the tag and data. The tag embedded in the FIFO_DATA[23:0] identifies the source and type of each sample. The data in FIFO_DATA[23:0] is right justified for all data types. [Table 24](#) shows each data type in the FIFO along with the associated tags.

Table 24. FIFO Tags

DATA TYPE	TAG AND DATA																																									
BIT	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0																		
PPG1/2 MEAS 1	0	0	0	0	PPG_MEAS1_DATA[19:0]																																					
PPG1/2 MEAS 2	0	0	0	1	PPG_MEAS2_DATA[19:0]																																					
PPG1/2 MEAS 3	0	0	1	0	PPG_MEAS3_DATA[19:0]																																					
PPG1/2 MEAS 4	0	0	1	1	PPG_MEAS4_DATA[19:0]																																					
PPG1/2 MEAS 5	0	1	0	0	PPG_MEAS5_DATA[19:0]																																					
PPG1/2 MEAS 6	0	1	0	1	PPG_MEAS6_DATA[19:0]																																					
PPG1/2 DARK	0	1	1	0	PPG_DARK_DATA[19:0]																																					
PPG1/2 ALC OVF	0	1	1	1	PPG_ALC_OVF_DATA[19:0]																																					
PPG1/2 EXP OVF	1	0	0	0	PPG_EXP_OVF_DATA[19:0]																																					
BIOZ I	1	0	0	1	BIOZ_I_DATA[19:0]																																					
BIOZ Q	1	0	1	0	BIOZ_Q_DATA[19:0]																																					
ECG and Fast Recover Flag	1	0	1	1	0	F	ECG_DATA[17:0]																																			
ECGP ECGN Differential	1	1	0	0	ECGP_DATA[19:0]/ECGN_DATA[19:0]/ECGPN_DIFF_DATA[19:0]																																					
CAPP CAPN Differential	1	1	0	1	CAPPN_DIFF_DATA[19:0]																																					
ECG to PPG Timing	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																		
BIOZ to PPG Timing	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	BIOZ_PPG_TIMING_DATA[13:0]																									

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Vital-Sign AFE**Table 24. FIFO Tags (continued)**

DATA TYPE	TAG AND DATA																
ECG to BIOZ Timing	1 1 1 0 1 0 0 0 0 0 0 0 0 0 0 ECG_BIOZ_TIMING_DATA[9:0]																
Marker	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0																
Invalid data	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1																

PPG Tags

PPG tags are four bits. The PPG data is in two's complement format and is 20 bits. The MSB of the PPG data FIFO_DATA[19:0] is the sign bit. The sequencing of exposures is controlled by MEAS1_EN through MEAS6_EN bits in PPG Configuration 1 register 0x20. The ADC conversion sequence cycles through the enabled measurements starting from MEAS1.

The exposures selected for each of the six measurements, and their configuration are setup in the MEAS1 Setup to MEAS6 Setup registers (see the Register Map for details). If a measurement has both PPG channels enabled, the two resulting samples have the same tag and the FIFO position determines the corresponding channel. The first sample is from channel 1 and the second sample is from channel 2.

When COLLECT_RAW_DATA[1](0x22) is disabled, the computed data is stored as a single MEASx sample in the FIFO (see the [Ambient Rejection](#) section). When COLLECT_RAW_DATA is enabled, the raw exposure sample and the dark (ambient) sample(s) are stored as separate samples in the FIFO. The raw exposure sample is tagged with its corresponding MEASx tag, but all dark samples are tagged with the same DARK tag, regardless of which measurement it came from.

When ALC_OVF[4](0x00) is detected for any measurement, the computed data for that measurement is tagged with the PPG_ALC_OVF_DATA tag, which is 0x7. When EXP_OVF[3](0x00) is detected for any measurement, the computed data for that measurement is tagged with the PPG_EXP_OVF_DATA tag, which is 0x8. The positions of the data with the PPG_ALC_OVF_DATA or PPG_EXP_OVF_DATA tags indicate which measurement and which optical channel the data belongs to. When both ALC_OVF and EXP_OVF are detected on the same measurement, the sample is tagged with the ALC OVF tag.

BioZ Tags:

BioZ tags are four bits. Tags for I channel data and Q channel data are 0x9 and 0xA, respectively.

Note that if the BioZ channel is disabled while a sample is being pushed to the FIFO, the FIFO will contain an extra sample containing the value 0x4000, which should be ignored. This can be avoided by disabling the BioZ channel immediately after a FIFO_DATA_RDY or A_FULL interrupt.

ECG Tag:

The ECG tag is six bits, of which the LSB indicates if the data corresponds to normal mode ($F = 0$) or fast recovery mode ($F = 1$). The tag for normal mode is 0x2C and for fast recovery mode is 0x2D.

Timing Data Tags:

The timing data tags are six bits and the timing data is right justified. The tag for ECG to PPG timing data is 0x38, and the data is ten bits. The tag for BioZ to PPG timing data is 0x39, and the data is fourteen bits. The tag for ECG to BioZ timing data is 0x3A and the data is ten bits. See the [Timing Data in the FIFO](#) section for more information.

Utility Data Tags:

Utility data tags are four bits. These are used for ECGP to ECGN differential input and CAPP-to-CAPN differential input measurements. The tags used for these are 0xC and 0xD, respectively.

Other Tags:

Invalid data and marker tags are 24 bits each.

An attempt to read an empty FIFO returns the INVALID_DATA tag, which is 0xFFFFFFF.

MAX86178 provides a feature of saving a FIFO marker when needed in an application. For example, in order to distinguish data saved in the FIFO before and after a configuration change, a marker can be saved in the FIFO just before the configuration change. The marker tag is 0xFFFFFE.

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For details on FIFO configuration, see the Register Map (registers 0x08 to 0x0E).

FIFO Configuration Examples

FIFO configuration is best explained by a few examples.

Example 1: PPG only

Assume it is desired to perform an SpO₂ measurement along with heart-rate monitoring using dual optical channels and also monitor the ambient level on the photodiode to adjust the LED intensity. To perform this measurement, configure the following registers.

```
//PLL Configuration
Set REF_CLK_SEL as desired           //Use internal oscillator or external clock signal
Set CLK_FREQ_SEL as desired          //Select 32kHz or 32.768kHz REF_CLK

//PPG Frame Rate Configuration
Set FR_CLK_DIV as desired           //Set the frame rate divider

//PPG configuration
Set PPG1_PWRDN = 0                  //Do not power down PPG1 ADC
Set PPG2_PWRDN = 0                  //Do not power down PPG2 ADC
Set MEAS1_EN = 1                    //Enable measurement 1 to 4
Set MEAS2_EN = 1
Set MEAS3_EN = 1
Set MEAS4_EN = 1

//MEASUREMENT 1 Configuration
Set MEAS1_AMB = 0                  //Ambient measurement off
Set MEAS1_DRVA = 0x0               //LED Driver A driving green LED on LED1_DRV
Set MEAS1_AVER as desired          //Number of LED pulses in each frame
Set MEAS1_PPG1_ADC_RGE as desired   //Gain range control for PPG1 ADC
Set MEAS1_PPG2_ADC_RGEas desired    //Gain range control for PPG2 ADC
Set MEAS1_PPG_TINT as desired       //ADC integration time control
Set MEAS1_LED_RGE as desired        //LED drive current range
Set MEAS1_PD_SETLNG as desired      //Settling time for photodiodes
Set MEAS1_LED_SETLNG as desired     //LED settling time
Set MEAS1_DRVA_PA as desired        //LED driver A current driving the green LED on LED1_DRV
Set MEAS1_DRVB_PA = 0x00            //LED driver B current should be set to 0
Set MEAS1_PD1_SEL = 0x2             //Photodiode 1 selected on optical channel 1
Set MEAS1_PD3_SEL = 0x3             //Photodiode 3 selected on optical channel 2

//MEASUREMENT 2 Configuration
Set MEAS2_AMB = 0                  //Ambient measurement off
Set MEAS2_DRVA = 0x1               //LED Driver A driving IR LED on LED2_DRV
Set MEAS2_AVER as desired          //Number of LED pulses in each frame
Set MEAS2_PPG1_ADC_RGE as desired   //Gain range control for PPG1 ADC
Set MEAS2_PPG2_ADC_RGEas desired    //Gain range control for PPG2 ADC
Set MEAS2_PPG_TINT as desired       //ADC integration time control
Set MEAS2_LED_RGE as desired        //LED drive current range
Set MEAS2_PD_SETLNG as desired      //Settling time for photodiodes
Set MEAS2_LED_SETLNG as desired     //LED settling time
Set MEAS2_DRVA_PA as desired        //LED driver A current driving the IR LED on LED2_DRV
Set MEAS2_DRVB_PA = 0x00            //LED driver B current should be set to 0
```

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```

Set MEAS2_PD2_SEL = 0x2           //Photodiode 2 selected on optical channel 1

//MEASUREMENT 3 Configuration
Set MEAS3_AMB = 0                 //Ambient measurement off
Set MEAS3_DRV_B = 0x2             //LED Driver B driving red LED on LED3_DRV
Set MEAS3_AVER as desired         //Number of LED pulses in each frame
Set MEAS3_PPG1_ADC_RGE as desired //Gain range control for PPG1 ADC
Set MEAS3_PPG2_ADC_RGE as desired //Gain range control for PPG2 ADC
Set MEAS3_PPG_TINT as desired    //ADC integration time control
Set MEAS3_LED_RGE as desired     //LED drive current range
Set MEAS3_PD_SETLNG as desired   //Settling time for photodiodes
Set MEAS3_LED_SETLNG as desired  //LED settling time
Set MEAS3_DRVA_PA = 0x00          //LED driver A current should be set to 0
Set MEAS3_DRV_B_PA as desired    //LED driver B current driving the red LED on LED3_DRV
Set MEAS3_PD2_SEL = 0x2           //Photodiode 2 selected on optical channel 1

//MEASUREMENT 4 Configuration
Set MEAS4_AMB = 1                 //Ambient measurement selected
Set MEAS4_PPG1_ADC_RGE as desired //Gain range control for PPG1 ADC
Set MEAS4_PPG2_ADC_RGE as desired //Gain range control for PPG2 ADC
Set MEAS4_PPG_TINT as desired    //ADC integration time control
Set MEAS4_PD1_SEL = 0x2           //Photodiode 1 selected on optical channel 1
Set MEAS4_PD3_SEL = 0x3           //Photodiode 3 selected on optical channel 2

```

With this configuration the sample sequence and the data format in the FIFO follows the following time/location sequence.

TAG[23:20]	DATA[19:0]
0b0000	PPG1 Measurement 1 data
0b0000	PPG2 Measurement 1 data
0b0001	PPG1 Measurement 2 data
0b0001	PPG2 Measurement 2 data
0b0010	PPG1 Measurement 3 data
0b0010	PPG2 Measurement 3 data
0b0011	PPG1 Measurement 4 data
0b0011	PPG2 Measurement 4 data
.	
.	
.	
0b0000	PPG1 Measurement 1 data
0b0000	PPG2 Measurement 1 data
0b0001	PPG1 Measurement 2 data
0b0001	PPG2 Measurement 2 data
0b0010	PPG1 Measurement 3 data
0b0010	PPG2 Measurement 3 data
0b0011	PPG1 Measurement 4 data
0b0011	PPG2 Measurement 4 data

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where:

- PPGm Measurement 1 data = Ambient corrected exposure data from green LED in optical channel m
- PPGm Measurement 2 data = Ambient corrected exposure data from IR LED in optical channel m
- PPGm Measurement 3 data = Ambient corrected exposure data from red LED in optical channel m
- PPGm Measurement 4 data = Direct ambient sample in optical channel m
- m is 1 for optical channel 1, and 2 for optical channel 2

The number of bytes of data for the two optical channels in one frame is given by: $2 \times 3 \times N$ where:

N = the number of measurements enabled

Example 2: ECG with three dry electrodes

This setup performs ECG measurements at 512sps and assumes three dry electrodes are in contact with the body, so it applies right leg drive and AC lead-off detection. To perform this measurement, configure the following registers.

//PLL Configuration (SR_ECG = 512sps)

```
Set REF_CLK_SEL as desired      //Use internal oscillator or external clock signal
Set CLK_FREQ_SEL = 1           //Select 32.768kHz clock frequency

Set MDIV = 0x07F               //PLL M divider set to 128 (PLL CLK = 4.19MHz)
Set ECG_NDIV = 0x010            //ECG N divider set to 16
Set ECG_FDIV = 0x1              //ECG F divider set to 1
Set PLL_EN = 1                  //Enable the PLL
```

//ECG Configuration (SR_ECG = 512sps)

```
Set ECG_DEC_RATE = 0x5          //ECG decimation ratio is 512
Set ECG_PGA_GAIN = 0x0          //PGA gain is 1V/V
Set ECG_INA_RGE = 0x0            //INA gain is 10V/V
Set ECG_INA_GAIN = 0x0            //INA gain is 10V/V
Set ECG_AUTO_REC = 1             //Automatic INA recovery enabled
Set EN_ECG_FAST_REC = 0x2        //Automatic fast recovery enabled
Set ECG_FAST_REC_THRESHOLD = 0x3D //Fast recovery threshold set to 95% of full scale
Set EN_ECG_RBIASP = 0             //Bias resistor on ECGP is disabled
Set EN_ECG_RBIASN = 0             //Bias resistor on ECGN is disabled
Set ECG_MUX_SEL as desired       //Enable the ECG MUX and assign the proper electrodes
Set ECG_OPEN_P = 0                //Connect ECGP to the selected electrode
Set ECG_OPEN_N = 0                //Connect ECGN to the selected electrode

Set ECG_EN = 1                  //ECG channel is enabled
```

//AC Lead-Off Detection Configuration (8192Hz)

```
Set ECG_LOFF_FREQ = 0x7          //ACLO N divider set to 64
Set ECG_LOFF_IMAG = 0x6            //ACLO current = 200nAPK, or as desired to match  $Z_{ETI}$ 
Set ECG_LOFF_THRESH = 0x2          //ACLO threshold =  $V_{MID\_ECG} \pm 200mV$ , or as desired
Set ECG_LOFF_MODE = 1              //AC lead-off detection mode
```

```
Set EN_ECG_LOFF = 1              //Enable lead-off detection
```

//RLD Configuration

```
Set RLD_MODE = 1                  //Closed loop RLD (AC Common Mode feedback)
```

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```

Set EN_RLD_OOR = 1           //Out of Range detection is enabled
Set ACTV_CM_P = 1            //Positive input buffer is enabled
Set ACTV_CM_N = 1            //Negative input buffer is enabled
Set RLD_GAIN = 0x3           //RLD Gain is 97V/V
Set RLD_EXT_RES = 0          //Internal gain resistor is used
Set RLD_SEL_ECG = 1          //Input voltages from ECGP and ECGN
Set RLD_BW = 0x0              //Low bandwidth
Set BODY_BIAS_DAC = 0x0      //Reference is VMID_ECG

Set RLD_EN = 1                //Right Leg Drive is enabled

```

In this case, the FIFO only contains ECG samples in the following format:

TAG[23:18]	DATA[17:0]
0b10110F	ECG data
0b10110F	ECG data
0b10110F	ECG data
...	

Example 3: ECG with two wet electrodes, respiration, and PPG with one LED in single-channel mode

ECG to PPG timing data and ECG to BioZ timing data are also enabled. This setup performs ECG measurements at 512sps and assumes two wet electrodes are attached to the body, so it applies internal lead bias and uses DC lead-off detection. Respiration shares the ECG electrodes, and measures at 128sps with a stimulus frequency of 65.536kHz. PPG enables one green LED on pin 1 with a single-channel configuration. ECG to PPG timing data indicates the time difference between measurement 1 in each frame and the last ECG sample saved in the FIFO. ECG to BioZ timing data indicates the time difference between the BioZ samples entering the FIFO and the last ECG samples saved in the FIFO.

```

//System Configuration
Set ECG_PPG_TIMING_DATA = 1      //ECG to PPG timing data is enabled
Set ECG_BIOZ_TIMING_DATA = 1      //ECG to BioZ timing data is enabled

//PLL Configuration (SR_ECG = 512sps, SR_RESP = 128sps, F_RESP = 65.563kHz)

Set REF_CLK_SEL as desired       //Use internal oscillator or external clock signal
Set CLK_FREQ_SEL = 1             //Select 32.768kHz clock frequency

Set MDIV = 0x1FF                //PLL M divider set to 512
Set ECG_NDIV = 0x100             //ECG N divider set to 512
Set ECG_FDIV = 0x1               //ECG/Respiration F divider set to 1
Set BIOZ_KDIV = 0x0              //BioZ K divider set to 1
Set BIOZ_NDIV = 0x1              //BioZ N divider set to 512
Set PLL_EN = 1                  //Enable the PLL

//PPG Frame Rate Clock Configuration (PPG_FR_CLK = ECG_ADC_CLK = 16.384kHz)
Set FR_CLK_DIV = 0x00A0          //FR divider set to 160, FR_PPG = 102.4fps

//PPG Configuration

Set PPG1_PWRDN = 0               //Do not power down PPG1 ADC
Set PPG2_PWRDN = 1               //PPG2 ADC is powered down
Set MEAS1_EN = 1                 //Only measurement 1 is enabled

```

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```

//MEASUREMENT 1 Configuration
Set MEAS1_AMB = 0           //Ambient measurement off
Set MEAS1_DRVA = 0x0         //LED driver A driving green LED on LED1_DRV
Set MEAS1_AVER as desired   //Number of LED pulses in each frame
Set MEAS1_PPG1_ADC_RGE as desired //Gain range control for PPG1 ADC
Set MEAS1_PPG2_ADC_RGEas desired //Don't care because PPG2 is powered down
Set MEAS1_PPG_TINT as desired //ADC integration time control
Set MEAS1_LED_RGE as desired //LED drive current range
Set MEAS1_PD_SETLNG as desired //Settling time for photodiodes
Set MEAS1_LED_SETLNG as desired //LED settling time
Set MEAS1_DRVA_PA as desired //LED driver A current driving the green LED on LED1_DRV
Set MEAS1_DRVB_PA = 0x00     //LED driver B current should be set to 0
Set MEAS1_PPG1_PDSEL = 0x0   //Photodiode 1 selected on optical channel 1
Set MEAS1_PPG2_PDSEL       //Don't care because PPG2 is powered down

//ECG Configuration (SR_ECG = 512sps)
Set ECG_DEC_RATE = 0x3      //ECG ADC OSR = 128
Set ECG_PGA_GAIN = 0x0       //PGA gain is 1V/V
Set ECG_INA_GAIN = 0x1       //INA gain is 20V/V
Set ECG_INA_RGE = 0x0       //INA gain is 20V/V
Set ECG_AUTO_REC = 1        //Automatic fast recovery is enabled
Set ECG_FAST_REC_THRESHOLD = 0x3D //Fast recovery threshold set to 95% of full scale
Set ECG_RBIAS_VALUE = 0x1    //Bias resistor value is 100MΩ
Set EN_ECG_RBIASP = 1        //Bias resistor on ECGP is enabled
Set EN_ECG_RBIASN = 1        //Bias resistor on ECGN is enabled
Set ECG_MUX_EN as desired   //Enable the ECG MUX and assign the proper electrodes

Set ECG_EN = 1               //ECG channel is enabled

//ECG DC Lead-Off Detection Configuration
Set EN_ECG_LOFF = 1          //DC lead-off detection enabled
Set ECG_LOFF_IMAG = 0x4       //Current magnitude is 50nA
Set ECG_LOFF_THRESH = 0x5      //Threshold is V_MID_ECG ±300mV

//BioZ and Respiration Configuration (SR_RESP = 128sps, F_RESP = 65.536kHz)
Set ECG_BIOZ_BG_EN = 1        //Enable the ECG/BioZ reference
Set BIOZ_ADC_OSР = 0x5        //BioZ ADC OSR set to 256
Set CG_CHOP_CLK = 0x0          //Respiration CG clock divider set to 256
Set BIOZ_DHPF = 0x1            //Set the digital HPF to SR_BIOZ x 0.00025 = 0.032Hz
Set BIOZ_AHPF = 0x5            //Set the analog HPF to 5kHz
Set BIOZ_GAIN = 0x0             //Set the receive channel gain to 1V/V, or as desired
Set BIOZ_CH_FSEL = 0           //F_BIOZ is not equal to BIOZ_ADC_CLK/16
Set RESP(CG_MAG_4X as desired //Match the current magnitude to the expected load impedance

Set RESP(CG_MAG as desired    //Match the current magnitude to the expected load impedance
Set CG_MODE = 0x2              //Enable dynamic matching with LPF
Set CG_LPF_DUTY = 0x3          //Set the LPF bandwidth to approximately 7.79Hz
Set DRVP_ASSIGN = 0x0           //DRVP is set to BIOZ_EL1
Set DRVN_ASSIGN = 0x0           //DRVN is set to BIOZ_EL4
Set BIP_ASSIGN = 0x2             //BIP is set to BIOZ_EL2B
Set BIN_ASSIGN = 0x2             //BIN is set to BIOZ_EL3B
Set BIOZ_MUX_EN = 1             //Enable the MUX
Set RESP_EN = 1                 //Enable respiration mode
Set BIOZ_EN = 0x1               //Enable in-phase BioZ measurements

```

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In this case, the FIFO contains ECG, BioZ, and PPG samples, along with ECG to PPG timing data and ECG to BioZ timing data in the following format:

TAG	DATA
...	
0b10110F	ECG data
0b10110F	ECG data
0b111010	ECG to BioZ Timing data
0b1001	BioZ I data
0b10110F	ECG data
0b111000	ECG to PPG Timing data
0b0000	PPG1 Measurement 1 data
0b10110F	ECG data
0b10110F	ECG data
...	

Example 4: BIA measurement at 10kHz

This setup measures BioZ at 78.13sps and a stimulus frequency of 10.0kHz, and assumes a tetrapolar electrode configuration. For a typical bioimpedance analysis (BIA), this measurement would be repeated for the I and Q phases at multiple frequencies with the TX channel placed in standby mode between measurements.

```
//PLL Configuration (SR_BIOZ = 78.13sps, F_BIOZ = 10.0kHz)
Set REF_CLK_SEL as desired           //Use internal oscillator or external clock signal
Set CLK_FREQ_SEL = 1                 //Select 32.768kHz clock frequency

Set MDIV = 0x270                    //PLL M divider set to 625
Set BIOZ_KDIV = 0x3                 //BioZ K divider set to 8
Set BIOZ_NDIV = 0x2                 //BioZ N divider set to 1024
Set PLL_EN = 1                      //Enable the PLL

//BioZ Configuration (SR_BIOZ = 78.13sps, F_BIOZ = 10.0kHz)
Set ECG_BIOZ_BG_EN = 1              //Enable the ECG/BioZ reference
Set BIOZ_ADC_OSR = 0x5              //BioZ ADC OSR set to 256
Set BIOZ_DAC_OSR = 0x3              //BioZ DAC OSR set to 256
Set BIOZ_AHPF = 0x2                 //Set the analog HPF to 500Hz
Set BIOZ_GAIN = 0x0                 //Set the receive channel gain to 1V/V, or as desired
Set BIOZ_CH_FSEL = 0                //F_BIOZ is not equal to BIOZ_ADC_CLK/16
Set BIOZ_DRV_MODE = 0x0             //Sine wave current mode
Set BIOZ_VDRV_MAG = 0x2             //Set current magnitude to 32µARMS

Set BIOZ_IDRV_RGE = 0x2            //Set current magnitude to 32µARMS
Set BIOZ_AMP_RGE = 0x2              //Match the amplifier range with the current range
Set BIOZ_AMP_BW = 0x2               //Set amplifier BW to mid-high
Set BIOZ_INA_MODE = 0                //INA is in low-noise mode
Set BIOZ_INT_INLOAD = 1              //Enable internal input load cancellation
Set BIOZ_EXT_INLOAD = 1              //Enable guard amplifiers (if guard traces are routed)
Set DRVP_ASSIGN = 0x0               //DRVP is set to BIOZ_EL1
Set DRVN_ASSIGN = 0x0               //DRVN is set to BIOZ_EL4
Set BIP_ASSIGN = 0x2                 //BIP is set to BIOZ_EL2B
Set BIN_ASSIGN = 0x2                 //BIN is set to BIOZ_EL3B
```

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```
Set BIOZ_MUX_EN = 1           //Enable the MUX
Set BIOZ_EN = 0x1             //Enable in-phase BioZ measurements
```

In this case, the FIFO contains only BioZ I data in the following format:

TAG	DATA
...	
0b1001	BioZ I data
...	

If the application always responds much faster than the selected sample rate, it could just read 256 minus FIFO_A_FULL[7:0] items when it gets an A_FULL interrupt, and be assured that all data from the FIFO are read. However, if there is a need to calculate the number of items available in the FIFO one can perform the following pseudo-code:

```
read the OVF_COUNTER register
read the FIFO_DATA_COUNT registers
if OVF_COUNTER == 0 //no overflow occurred
    NUM_AVAILABLE_SAMPLES = FIFO_DATA_COUNT
else
    NUM_AVAILABLE_SAMPLES = 256 // overflow occurred and data has been lost
endif
```

LDO

The MAX86178 includes a low dropout (LDO) linear regulator, enabling operation from a single supply in size-constrained applications, or applications powered by a primary coin-cell battery. The single supply voltage should be selected according to the highest LED forward voltage plus the minimum voltage overhead (see the [Optical Transmitter](#) section). This supply is then connected to V_{LED}, the LED anodes, and LDO_IN. LDO_OUT provides 1.825V (typ) to power AVDD and DVDD (and IOVDD if needed), but must not be used to power other components or ICs due to the thermal constraints of the MAX86178 package. This configuration is shown in [Typical Application Circuit 1](#) and [Typical Application Circuit 2](#). If the LDO is not used, connect LDO_IN to AGND and leave LDO_OUT unconnected as shown in [Typical Application Circuit 3](#).

Digital Interface

The MAX86178 supports I²C and SPI serial interfaces. The CSB/I²C_SEL pin selects the interface being used at any one time. When the I²C_SEL pin is high using an external pullup resistor, the interface is in I²C mode and idles looking for a start condition on the SCL and SDA pins, while the SPI interface is held in a reset state. When the CSB/I²C_SEL pin is low, the I²C interface is disabled and the SPI interface is activated. In the following sections, timings and protocols for both interfaces are described.

SPI Interface

The SPI interface on the MAX86178 is SPI-/QSPI-/microwire-/DSP-compatible consisting of a serial data input (SDI), a serial data output (SDO), a serial clock line (SCLK), and a chip select (CSB). In SPI mode, the SDI/SDA pin operates as SDI and the SCLK/SCL pin operates as SCLK. The timing of the SPI interface is shown in [Figure 51](#). Data is strobed on the SCLK rising edge while clocked out on the SCLK falling edge. All single-word SPI read and write operations are done in a 3-byte, 24-clock-cycle SPI instruction framed by a CSB low interval. The content of the SPI operation consists of a one-byte register address (A[7:0]) followed by a one-byte command word, which defines the transaction as write or read, followed by a single-byte data word either written to or read from the register location provided in the first byte.

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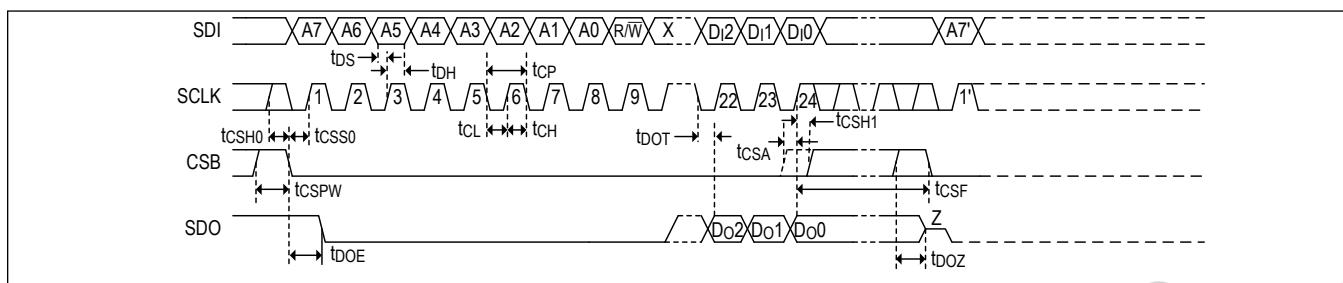


Figure 51. Detailed SPI Timing Diagram

Single-Word SPI Register Read and Write Transactions

SPI write mode operations for MAX86178 are executed on the 24th SCLK rising edge using the first three bytes of data available. In write mode, any data supplied after the 24th SCLK rising edge is ignored as shown in [Figure 52](#). Subsequent writes require CSB to deassert high and then assert low for the next write command. A rising CSB edge preceding the 24th rising edge of SCLK by tCSA as shown in [Figure 51](#), results in the transaction being aborted.

Read mode operations access the requested data on the 16th SCLK rising edge, and present the MSB of the requested data on the following SCLK falling edge, allowing the microcontroller to latch the data MSB on the 17th SCLK rising edge as shown in [Figure 53](#). Configuration and status registers are available using normal-mode read-back sequences. FIFO reads must be done with a burst mode FIFO read (see the [SPI Burst Mode Read Transaction](#) section). In a normal read sequence, any SCLK rising edges after the 24th SCLK rising edge are ignored and if more than 24 SCLK rising edges are provided, the device reads back zeros.

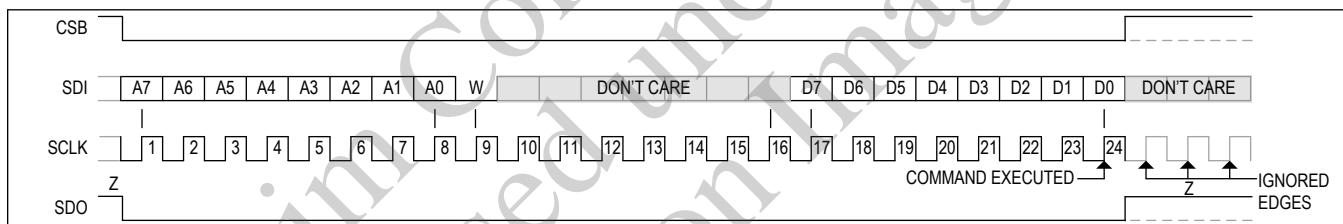


Figure 52. SPI Write Transaction

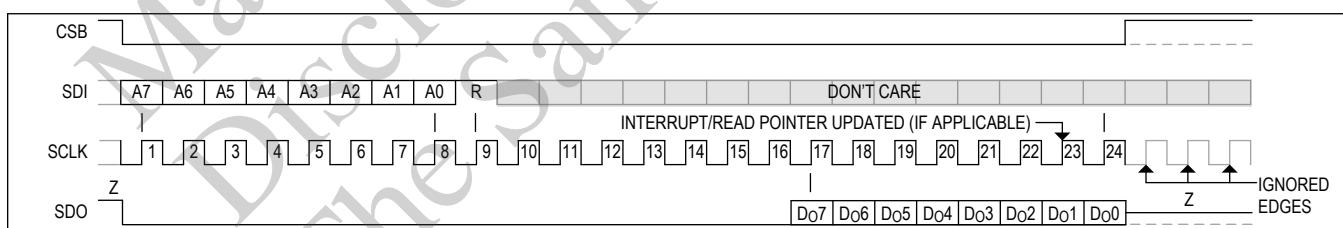


Figure 53. SPI Read Transaction

SPI Burst Mode Read Transaction

The MAX86178 has a FIFO burst-read mode to increase data transfer efficiency. The first 16 SCLK cycles operate exactly as described for the normal read mode, where the first byte is the register address and the second is the read command. The subsequent SCLKs consist of FIFO data, 24 SCLKs per word. All words in the FIFO should be read with a single FIFO burst-read command.

Each FIFO sample consists of 3 bytes per sample, and thus, requires 24 SCLKs per sample to read out. The first byte

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(SCLK 17 to 24) consists of a tag indicating the data type of the subsequent bits as well as the MSBs of the data. The next two bytes (SCLK 24 to 40) consist of data. For example, [Figure 54](#) shows a FIFO burst read consisting of three PPG samples in FIFO, labeled A through C, each with a 4-bit tag and 20-bit data. The number of words in the FIFO depends on the FIFO configuration. See the [FIFO Description](#) section for more details about the FIFO configuration and readout.

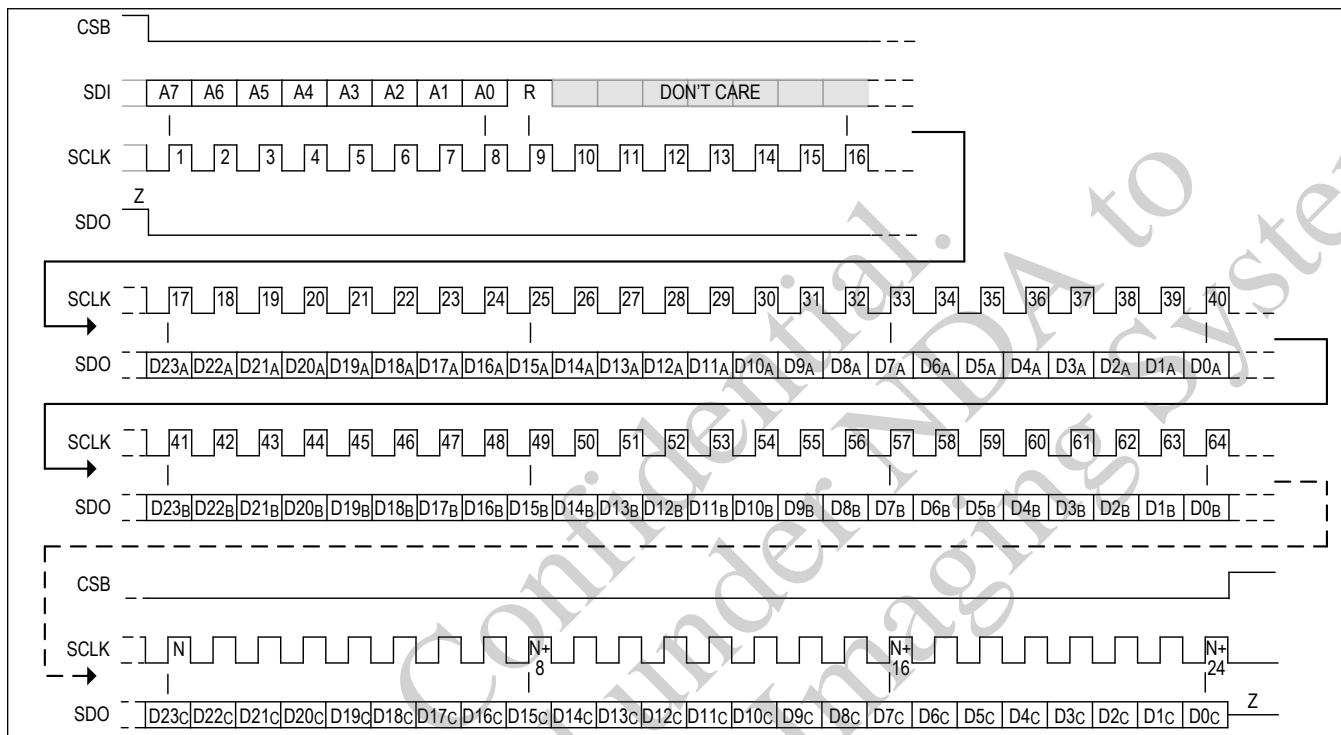
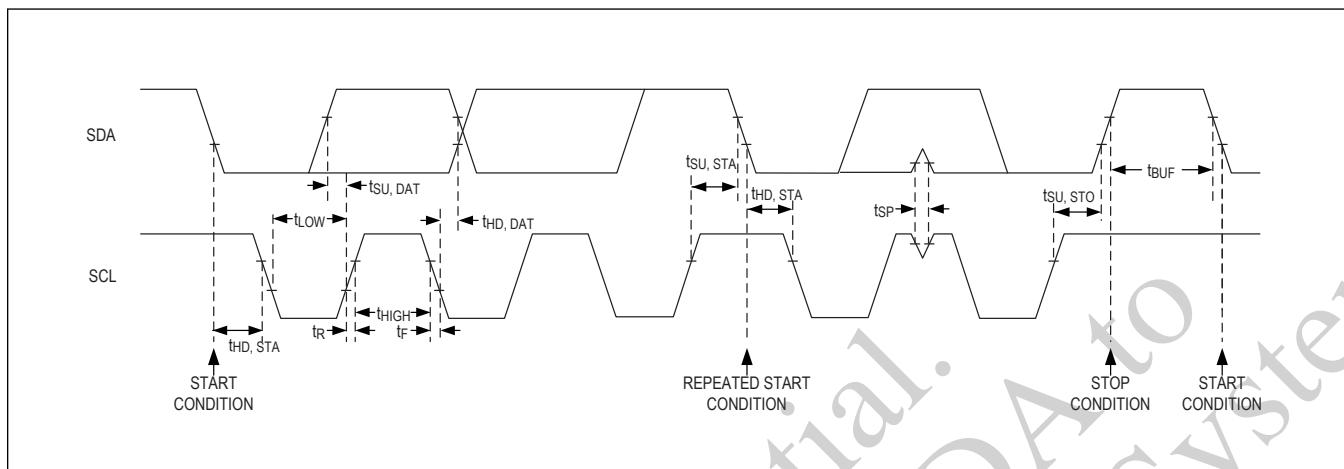


Figure 54. SPI FIFO Burst Mode Read Transaction

I²C-/SMBus-Compatible Serial Interface

The I²C interface on the MAX86178 is an I²C-/SMBus-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). In I²C mode, the SDI/SDA pin operates as SDA and the SCLK/SCL pin operates as SCL. These two pins are used for the communication between the MAX86178 and the master at clock rates up to 400kHz. [Figure 55](#) shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX86178 by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX86178 is 8-bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX86178 transmits the proper slave address followed by a series of nine SCL pulses. The MAX86178 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge (NACK), and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pullup resistor is required on SDA. SCL operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

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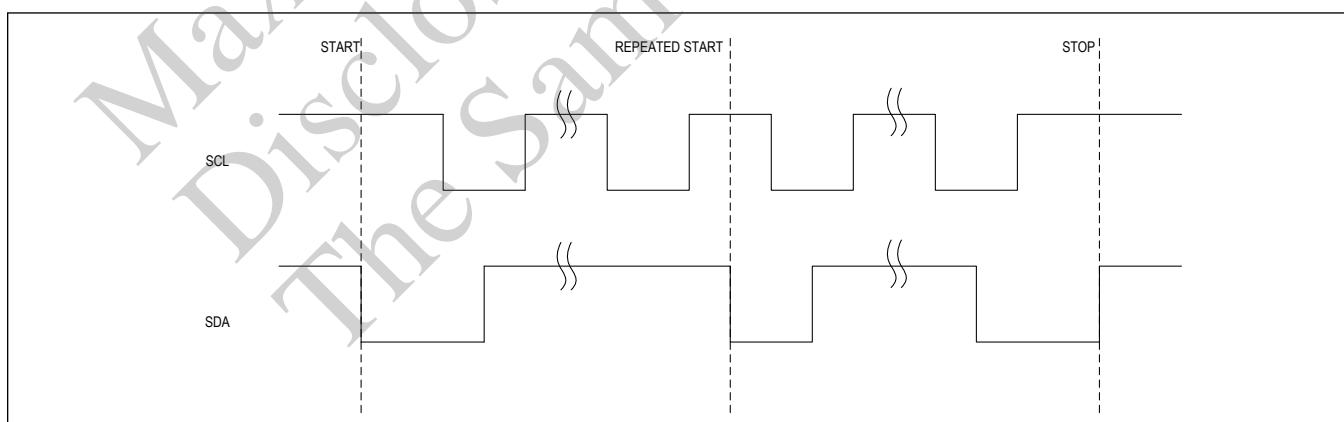
MAX86178**Ultra-Low-Power, Clinical-Grade
Vital-Sign AFE**Figure 55. Detailed I²C Timing Diagram**Bit Transfer**

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the [START and STOP Conditions](#) section).

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition, which indicates the beginning of a transmission to the MAX86178. A START condition is a high-to-low transition on SDA while SCL is high as shown in [Figure 56](#). The master terminates transmission, and frees the bus, by issuing a STOP condition. A STOP condition is a low-to-high transition on SDA while SCL is high as shown in [Figure 56](#). The bus remains active if a REPEATED START condition is generated instead of a STOP condition. A REPEATED START condition is the same as a START condition (high-to-low transition with SCL high), but it is sent after a START condition.

The MAX86178 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

PRELIMINARYFigure 56. I²C START, STOP, and REPEATED START Conditions

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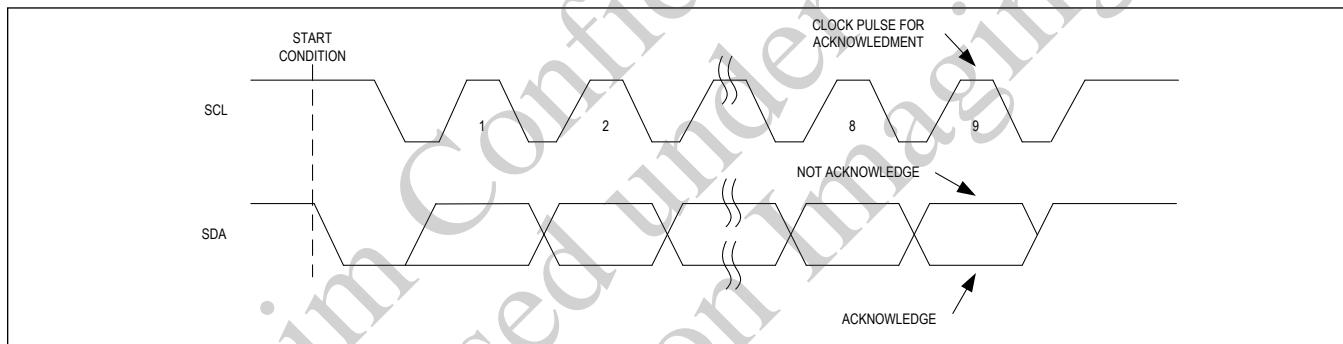
In I²C mode, the SDO/ADDR pin acts as the device address selector pin. The I²C slave address has two values, selected by SDO/ADDR when the I²C_SEL pin is pulled high. When ADDR is pulled low, either by a pulldown resistor or by the host controller, the slave address is 0xD8 (write) and 0xD9 (read), or 0b1101100 + R/W. When ADDR is pulled high, the slave address is 0xDA (write) and 0xDB (read), or 0b1101101 + R/W.

Table 25. I²C Addresses for MAX86178

ADDR PIN	WRITE ADDRESS	READ ADDRESS
Low	0xD8	0xD9
High	0xDA	0xDB

Acknowledge Bit

The acknowledge bit (ACK) is a clocked 9th bit that the MAX86178 uses to handshake-receipt each byte of data when in write mode as shown in [Figure 57](#). The MAX86178 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX86178 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the MAX86178, followed by a STOP condition.

[Figure 57. I²C Acknowledge Bit](#)**I²C Write Data Format**

A write to the MAX86178 includes transmission of a START condition, the slave address with the R/W bit set to 0, one byte of data to configure the internal register-address pointer, one or more bytes of data, and a STOP condition. [Figure 58](#) illustrates the proper frame format for writing one byte of data to the MAX86178. [Figure 59](#) illustrates the frame format for writing multiple bytes of data to the MAX86178.

The slave address with the R/W bit set to 0 indicates that the master intends to write data to the MAX86178. The device acknowledges receipt of the address byte during the master-generated 9th-SCL pulse.

The second byte transmitted from the master configures the internal register-address pointer of the MAX86178. The pointer tells the device where to write the next byte of data. An acknowledge pulse is sent by the MAX86178 upon receipt of the address-pointer data.

The third byte sent to the MAX86178 contains the data to be written to the pointed register. An acknowledge pulse from the MAX86178 signals receipt of the data byte. The address pointer auto increments to the next register address after each received data byte. This auto-increment feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition. The auto-increment feature is disabled when there is an attempt to write to the FIFO Data register(0x0C).

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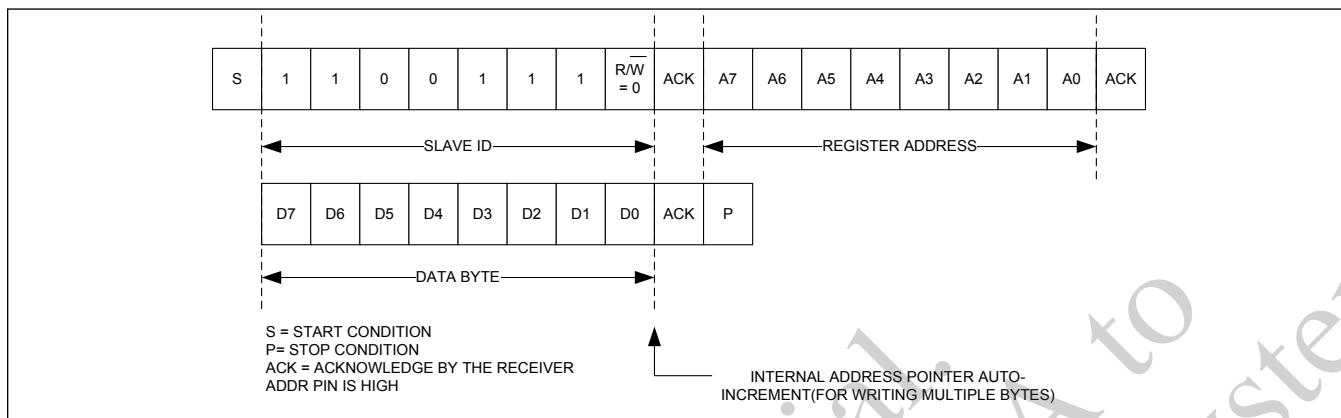


Figure 58. I^2C Single-Byte Write Transaction

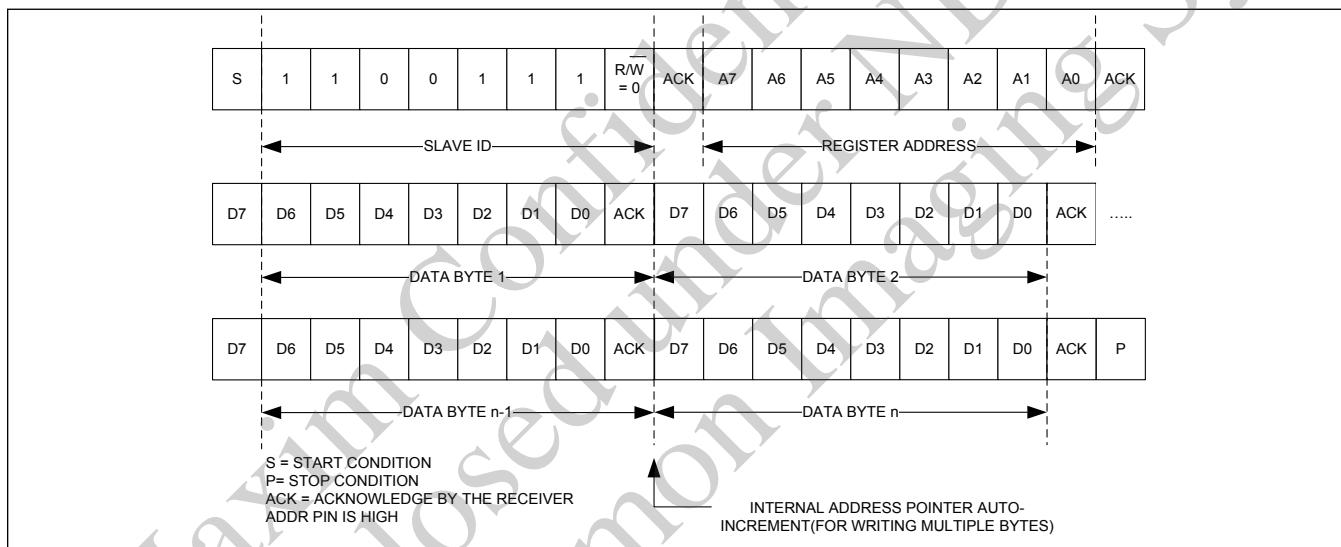


Figure 59. I^2C Multi-Byte Write Transaction

I^2C Read Data Format

A read from the MAX86178 includes sending the slave address with the R/W bit set to 1 to initiate a read operation. The MAX86178 acknowledges receipt of the slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the MAX86178 is the content of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer auto-increments after each read data byte. This auto-increment feature allows all registers to be read sequentially within one continuous frame. The auto-increment feature is disabled when there is an attempt to read from the FIFO Data register (0x0C). A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX86178 slave address with the R/W bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the slave address with the R/W bit set to 1. The MAX86178 then transmits the content of the specified register. The address pointer auto-increments after transmitting the first byte.

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The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. [Figure 60](#) illustrates the frame format for reading one byte from the MAX86178. [Figure 61](#) illustrates the frame format for reading multiple bytes from the MAX86178.

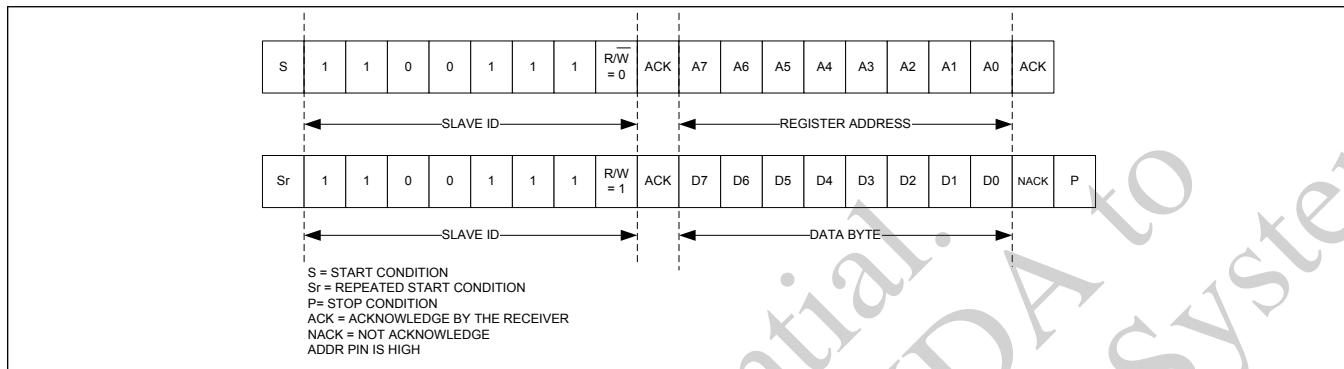


Figure 60. I²C Single-Byte Read Transaction

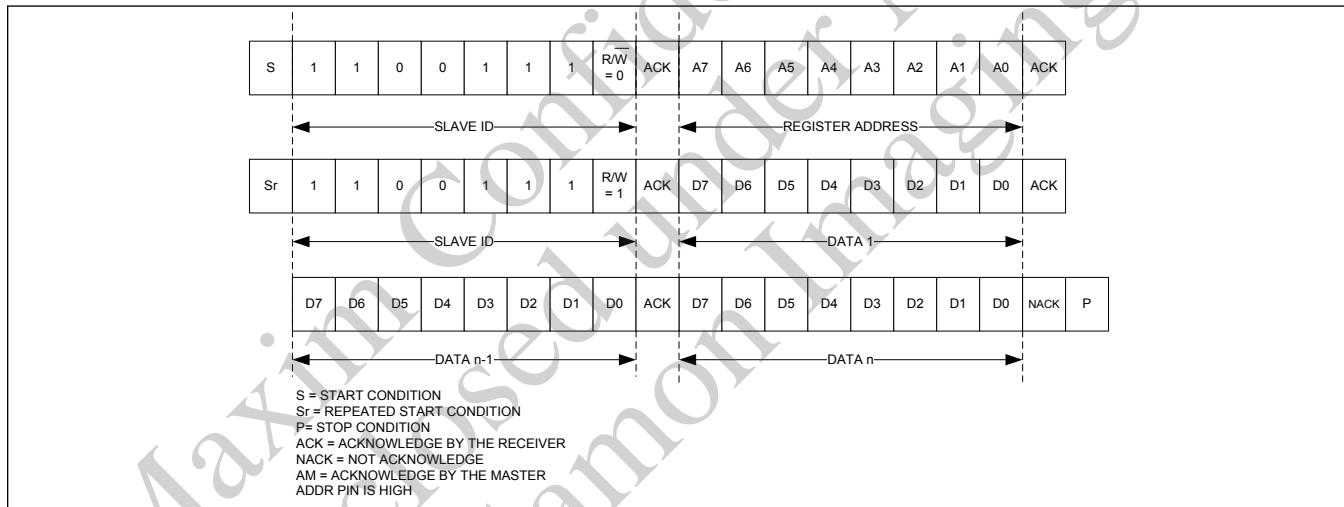


Figure 61. I²C Multi-Byte Read Transaction

I²C Broadcast

The MAX86178 provides a feature of I²C broadcast write transactions to multiple devices simultaneously using the I²C serial interface. The host microcontroller uses the address programmed in I₂C_BCAST_ADDR[7:1](0x15) to send a write command to multiple devices and the slave devices respond with an ACK. To use the broadcast feature, I₂C_BCAST_EN[0](0x15) must be set to 1.

This feature is especially useful for:

1. Synchronizing PLLs on multiple devices using the TIMING_SYS_RESET[7](0x10) bit; thereby, avoiding any external connections.
2. Programming the same configuration to multiple devices at the same time.

Read transactions in broadcast mode are not supported. If a host sends out a read command using the I²C broadcast address, the device responds with a NACK.

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Register Map

User Register Map

ADDRESS	NAME	MSB							LSB
Status									
0x00	<u>Status 1[7:0]</u>	A_FULL	PPG_FR AME_RD Y	FIFO_D ATA_RD Y	ALC_OV F	EXP_OV F	PPG_TH RESH2_HILO	PPG_TH RESH1_HILO	PWR_R DY
0x01	<u>Status 2[7:0]</u>	INVALID_PPG_C FG	-	LED6_C OMPB	LED5_C OMPB	LED4_C OMPB	LED3_C OMPB	LED2_C OMPB	LED1_C OMPB
0x02	<u>Status 3[7:0]</u>	-	-	-	FREQ_U NLOCK	FREQ_L OCK	PHASE_UNLOCK	PHASE_LOCK	-
0x03	<u>Status 4[7:0]</u>	ECG_LO N	-	ECG_FA ST_REC	RLD_OO R	ECG_LO FF_PH	ECG_LO FF_PL	ECG_LO FF_NH	ECG_LO FF_NL
0x04	<u>Status 5[7:0]</u>	BIOZ_L ON	BIOZ_O VER	BIOZ_U NDR	BIOZ_D RV_OO R	BIOZ_L OFF_PH	BIOZ_L OFF_PL	BIOZ_L OFF_NH	BIOZ_L OFF_NL
FIFO									
0x08	<u>FIFO Write Pointer[7:0]</u>						FIFO_WR_PTR[7:0]		
0x09	<u>FIFO Read Pointer[7:0]</u>						FIFO_RD_PTR[7:0]		
0x0A	<u>FIFO Counter 1[7:0]</u>	FIFO_D ATA_CO UNT[8]					OVF_COUNTER[6:0]		
0x0B	<u>FIFO Counter 2[7:0]</u>						FIFO_DATA_COUNT[7:0]		
0x0C	<u>FIFO Data Register[7:0]</u>						FIFO_DATA[7:0]		
0x0D	<u>FIFO Configuration 1[7:0]</u>						FIFO_A_FULL[7:0]		
0x0E	<u>FIFO Configuration 2[7:0]</u>	-	-	FIFO_M ARK	FLUSH_FIFO	FIFO_ST AT_CLR	A_FULL _TYPE	FIFO_R O	-
System Control									
0x10	<u>System Sync[7:0]</u>	TIMING_SYS_RESET	-	-	-	-	-	-	-
0x11	<u>System Configuration 1[7:0]</u>	-	DISABL_E_I2C	ECG_PP G_TIMING_DATA	BIOZ_P PG_TIMI NG_DAT A	ECG_BI OZ_TIMI NG_DAT A	-	SHDN	RESET
0x12	<u>System Configuration 2[7:0]</u>	BYP_DL Y	-	-			ECG_SAMP_SYNC_FREQ[4:0]		
0x13	<u>Pin Functional Configuration[7:0]</u>			TRIG_FCFG[2:0]	TRIG_IC FG	INT2_FCFG[1:0]	INT1_FCFG[1:0]		
0x14	<u>Output Pin Configuration[7:0]</u>		TRIG_OCFG[1:0]	-	-	INT2_OCFG[1:0]	INT1_OCFG[1:0]		
0x15	<u>I2C Broadcast Address[7:0]</u>							I2C_BCAST_ADDR[6:0]	I2C_BCAST_ST_EN

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ADDRESS	NAME	MSB							LSB
PLL									
0x18	<u>PLL Configuration 1[7:0]</u>		MDIV[9:8]	-	-	-	-	PLL_LO CK_WN DW	PLL_EN
0x19	<u>PLL Configuration 2[7:0]</u>				MDIV[7:0]				
0x1A	<u>PLL Configuration 3[7:0]</u>		BIOZ_NDIV[1:0]	-	-			BIOZ_KDIV[3:0]	
0x1B	<u>PLL Configuration 4[7:0]</u>			ECG_NDIV[10:8]	-	-		ECG_FDIV[2:0]	
0x1C	<u>PLL Configuration 5[7:0]</u>					ECG_NDIV[7:0]			
0x1D	<u>PLL Configuration 6[7:0]</u>	-	REF_CL K_SEL	CLK_FR EQ_SEL			CLK_FINE_TUNE[4:0]		
PPG Setup									
0x20	<u>PPG Configuration 1[7:0]</u>	-	-	MEAS6_EN	MEAS5_EN	MEAS4_EN	MEAS3_EN	MEAS2_EN	MEAS1_EN
0x21	<u>PPG Configuration 2[7:0]</u>	-	-	PPG_SY NC_MO DE	-	PPG2_P WRDN	PPG1_P WRDN	-	-
0x22	<u>PPG Configuration 3[7:0]</u>	-		SMP_AVE[2:0]		ALC_DIS ABLE	-	COLLEC T_RAW_ DATA	MEAS1_ CONFIG _SEL
0x23	<u>PPG Configuration 4[7:0]</u>	-	-	-	PROX_D ATA_EN	PROX_A UTO	-	-	-
0x24	<u>Photodiode Bias[7:0]</u>	PD4_BIAS[1:0]		PD3_BIAS[1:0]		PD2_BIAS[1:0]		PD1_BIAS[1:0]	
PPG Frame Rate Clock									
0x28	<u>FR Clock Divider MSB[7:0]</u>	-				FR_CLK_DIV[14:8]			
0x29	<u>FR Clock Divider LSB[7:0]</u>					FR_CLK_DIV[7:0]			
PPG MEAS1 Setup									
0x30	<u>MEAS1 Selects[7:0]</u>	-	MEAS1_AMB		MEAS1_DRVB[2:0]		MEAS1_DRVA[2:0]		
0x31	<u>MEAS1 Configuration 1[7:0]</u>	MEAS1_SINC3_SEL	MEAS1_FILT2_SEL	MEAS1_FILT_SE L	MEAS1_TINT[1:0]		MEAS1_AVER[2:0]		
0x32	<u>MEAS1 Configuration 2[7:0]</u>	-	-	MEAS1_PPG2_ADC _RGE[1:0]	-	-	MEAS1_PPG1_ADC _RGE[1:0]		
0x33	<u>MEAS1 Configuration 3[7:0]</u>			MEAS1_PPG2_DACOFF[3:0]			MEAS1_PPG1_DACOFF[3:0]		
0x34	<u>MEAS1 Configuration 4[7:0]</u>	MEAS1_PD_SETLN G[1:0]	-	-	MEAS1_LED_SETL NG[1:0]	MEAS1_LED_RGE[1:0]			
0x35	<u>MEAS1 Configuration 5[7:0]</u>	MEAS1_PD4_SEL[1: 0]	MEAS1_PD3_SEL[1: 0]	MEAS1_PD2_SEL[1: 0]	MEAS1_PD1_SEL[1: 0]				
0x36	<u>MEAS1 LEDA Current[7:0]</u>				MEAS1_DRVA_PA[7:0]				
0x37	<u>MEAS1 LEDB Current[7:0]</u>				MEAS1_DRVB_PA[7:0]				
PPG MEAS2 Setup									
0x38	<u>MEAS2 Selects[7:0]</u>	-	MEAS2_AMB		MEAS2_DRVB[2:0]		MEAS2_DRVA[2:0]		

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ADDRESS	NAME	MSB						LSB					
0x39	MEAS2 Configuration 1[7:0]	MEAS2_SINC3_SEL	MEAS2_FILT2_SEL	MEAS2_FILT_SEL	MEAS2_TINT[1:0]		MEAS2_AVER[2:0]						
0x3A	MEAS2 Configuration 2[7:0]	-	-	MEAS2_PPG2_ADC_RGE[1:0]	-		MEAS2_PPG1_ADC_RGE[1:0]						
0x3B	MEAS2 Configuration 3[7:0]	MEAS2_PPG2_DACOFF[3:0]				MEAS2_PPG1_DACOFF[3:0]							
0x3C	MEAS2 Configuration 4[7:0]	MEAS2_PD_SETLN_G[1:0]	-	-	MEAS2_LED_SETLNG[1:0]	MEAS2_LED_RGE[1:0]							
0x3D	MEAS2 Configuration 5[7:0]	MEAS2_PD4_SEL[1:0]	MEAS2_PD3_SEL[1:0]	MEAS2_PD2_SEL[1:0]	MEAS2_PD1_SEL[1:0]	MEAS2_DRVA_PA[7:0]							
0x3E	MEAS2 LEDA Current[7:0]	MEAS2_DRVB_PA[7:0]											
0x3F	MEAS2 LEDB Current[7:0]	MEAS2_DRVB_PA[7:0]											
PPG MEAS3 Setup													
0x40	MEAS3 Selects[7:0]	-	MEAS3_AMB	MEAS3_DRVB[2:0]			MEAS3_DRVA[2:0]						
0x41	MEAS3 Configuration 1[7:0]	MEAS3_SINC3_SEL	MEAS3_FILT2_SEL	MEAS3_FILT_SEL	MEAS3_TINT[1:0]		MEAS3_AVER[2:0]						
0x42	MEAS3 Configuration 2[7:0]	-	-	MEAS3_PPG2_ADC_RGE[1:0]	-	-	MEAS3_PPG1_ADC_RGE[1:0]						
0x43	MEAS3 Configuration 3[7:0]	MEAS3_PPG2_DACOFF[3:0]				MEAS3_PPG1_DACOFF[3:0]							
0x44	MEAS3 Configuration 4[7:0]	MEAS3_PD_SETLN_G[1:0]	-	-	MEAS3_LED_SETLNG[1:0]	MEAS3_LED_RGE[1:0]							
0x45	MEAS3 Configuration 5[7:0]	MEAS3_PD4_SEL[1:0]	MEAS3_PD3_SEL[1:0]	MEAS3_PD2_SEL[1:0]	MEAS3_PD1_SEL[1:0]	MEAS3_DRVA_PA[7:0]							
0x46	MEAS3 LEDA Current[7:0]	MEAS3_DRVB_PA[7:0]											
0x47	MEAS3 LEDB Current[7:0]	MEAS3_DRVB_PA[7:0]											
PPG MEAS4 Setup													
0x48	MEAS4 Selects[7:0]	-	MEAS4_AMB	MEAS4_DRVB[2:0]			MEAS4_DRVA[2:0]						
0x49	MEAS4 Configuration 1[7:0]	MEAS4_SINC3_SEL	MEAS4_FILT2_SEL	MEAS4_FILT_SEL	MEAS4_TINT[1:0]		MEAS4_AVER[2:0]						
0x4A	MEAS4 Configuration 2[7:0]	-	-	MEAS4_PPG2_ADC_RGE[1:0]	-	-	MEAS4_PPG1_ADC_RGE[1:0]						
0x4B	MEAS4 Configuration 3[7:0]	MEAS4_PPG2_DACOFF[3:0]				MEAS4_PPG1_DACOFF[3:0]							
0x4C	MEAS4 Configuration 4[7:0]	MEAS4_PD_SETLN_G[1:0]	-	-	MEAS4_LED_SETLNG[1:0]	MEAS4_LED_RGE[1:0]							
0x4D	MEAS4 Configuration 5[7:0]	MEAS4_PD4_SEL[1:0]	MEAS4_PD3_SEL[1:0]	MEAS4_PD2_SEL[1:0]	MEAS4_PD1_SEL[1:0]	MEAS4_DRVA_PA[7:0]							
0x4E	MEAS4 LEDA Current[7:0]	MEAS4_DRVB_PA[7:0]											

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ADDRESS	NAME	MSB							LSB						
0x4F	<u>MEAS4 LEDB</u> <u>Current[7:0]</u>		MEAS4_DRVB_PA[7:0]												
PPG MEAS5 Setup															
0x50	<u>MEAS5 Selects[7:0]</u>	-	MEAS5_AMB	MEAS5_DRVB[2:0]				MEAS5_DRVA[2:0]							
0x51	<u>MEAS5 Configuration 1[7:0]</u>	MEAS5_SINC3_SEL	MEAS5_FILT2_SEL	MEAS5_FILT_SEL	MEAS5_TINT[1:0]		MEAS5_AVER[2:0]								
0x52	<u>MEAS5 Configuration 2[7:0]</u>	-	-	MEAS5_PPG2_ADC_RGE[1:0]	-	-	-	MEAS5_PPG1_ADC_RGE[1:0]							
0x53	<u>MEAS5 Configuration 3[7:0]</u>	MEAS5_PPG2_DACOFF[3:0]				MEAS5_PPG1_DACOFF[3:0]									
0x54	<u>MEAS5 Configuration 4[7:0]</u>	MEAS5_PD_SETLN_G[1:0]	-	-	MEAS5_LED_SETLNG[1:0]	MEAS5_LED_RGE[1:0]									
0x55	<u>MEAS5 Configuration 5[7:0]</u>	MEAS5_PD4_SEL[1:0]	MEAS5_PD3_SEL[1:0]	MEAS5_PD2_SEL[1:0]	MEAS5_PD1_SEL[1:0]										
0x56	<u>MEAS5 LEDA</u> <u>Current[7:0]</u>	MEAS5_DRVA_PA[7:0]													
0x57	<u>MEAS5 LEDB</u> <u>Current[7:0]</u>	MEAS5_DRVB_PA[7:0]													
PPG MEAS6 Setup															
0x58	<u>MEAS6 Selects[7:0]</u>	-	MEAS6_AMB	MEAS6_DRVB[2:0]				MEAS6_DRVA[2:0]							
0x59	<u>MEAS6 Configuration 1[7:0]</u>	MEAS6_SINC3_SEL	MEAS6_FILT2_SEL	MEAS6_FILT_SEL	MEAS6_TINT[1:0]		MEAS6_AVER[2:0]								
0x5A	<u>MEAS6 Configuration 2[7:0]</u>	-	-	MEAS6_PPG2_ADC_RGE[1:0]	-	-	-	MEAS6_PPG1_ADC_RGE[1:0]							
0x5B	<u>MEAS6 Configuration 3[7:0]</u>	MEAS6_PPG2_DACOFF[3:0]				MEAS6_PPG1_DACOFF[3:0]									
0x5C	<u>MEAS6 Configuration 4[7:0]</u>	MEAS6_PD_SETLN_G[1:0]	-	-	MEAS6_LED_SETLNG[1:0]	MEAS6_LED_RGE[1:0]									
0x5D	<u>MEAS6 Configuration 5[7:0]</u>	MEAS6_PD4_SEL[1:0]	MEAS6_PD3_SEL[1:0]	MEAS6_PD2_SEL[1:0]	MEAS6_PD1_SEL[1:0]										
0x5E	<u>MEAS6 LEDA</u> <u>Current[7:0]</u>	MEAS6_DRVA_PA[7:0]													
0x5F	<u>MEAS6 LEDB</u> <u>Current[7:0]</u>	MEAS6_DRVB_PA[7:0]													
PPG Threshold Interrupts															
0x70	<u>THRESHOLD MEAS SEL[7:0]</u>	-	THRESH2_MEAS_SEL[2:0]				-	THRESH1_MEAS_SEL[2:0]							
0x71	<u>THRESHOLD HYST[7:0]</u>	THRESH2_PPG_SEL	THRESH1_PPG_SEL	-	TIME_HYST[1:0]			LEVEL_HYST[2:0]							
0x72	<u>PPG HI THRESHOLD1[7:0]</u>	THRESHOLD1_UPPER[7:0]													
0x73	<u>PPG LO THRESHOLD1[7:0]</u>	THRESHOLD1_LOWER[7:0]													
0x74	<u>PPG HI THRESHOLD2[7:0]</u>	THRESHOLD2_UPPER[7:0]													

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ADDRESS	NAME	MSB							LSB			
0x75	PPG LO THRESHOLD2[7:0]		THRESHOLD2_LOWER[7:0]									
ECG Setup												
0x80	ECG Configuration 1[7:0]	-	-	-	-	ECG_DEC_RATE[2:0]		ECG_EN				
0x81	ECG Configuration 2[7:0]	ECG_IPOL	ECG_PGA_GAIN[2:0]			ECG_INA_RGE[1:0]		ECG_INA_GAIN[1:0]				
0x82	ECG Configuration 3[7:0]	-	-	-	-	ECG_IM_P_HI	ECG_AU_TO_REC	ECG_MUX_SEL[1:0]				
0x83	ECG Configuration 4[7:0]	EN_ECG_FAST_REC[1:0]	ECG_FAST_REC_THRESHOLD[5:0]									
ECG Calibration												
0x84	ECG CAL Configuration 1[7:0]	ECG_CAL_HIGH[10:8]			ECG_CAL_FREQ[2:0]			ECG_CAL_DUTY	ECG_CAL_EN			
0x85	ECG CAL Configuration 2[7:0]	ECG_CAL_HIGH[7:0]										
0x86	ECG CAL Configuration 3[7:0]	ECG_OP_EN_P	ECG_OP_EN_N	ECG_CAL_MODE	ECG_CAL_MAG	ECG_CAL_P_SEL[1:0]	ECG_CAL_N_SEL[1:0]					
ECG Lead Detect												
0x88	ECG Lead Detect Configuration 1[7:0]	EN_ECG_LON	EN_ECG_LOFF	-	-	ECG_LOFF_MOD	ECG_LOFF_FREQ[2:0]					
0x89	ECG Lead Detect Configuration 2[7:0]	ECG_LOFF_IPOL	ECG_LOFF_IMAG[2:0]			ECG_LOFF_THRESH[3:0]						
ECG Lead Bias												
0x90	ECG Lead Bias Configuration 1[7:0]	-	-	-	-	ECG_RBIAS_VALUE[1:0]	EN_ECG_RBIAS_P	EN_ECG_RBIAS_N				
ECG RLD and CM Amps												
0x92	RLD Configuration 1[7:0]	RLD_EN	RLD_MODE	RLD_RB_IAS	EN_RLD_OOR	ACTV_CM_P	ACTV_CM_N	RLD_GAIN[1:0]				
0x93	RLD Configuration 2[7:0]	RLD_EX_T_RES	RLD_SEL_ECG	RLD_BW[1:0]		BODY_BIAS_DAC[3:0]						
BIOZ Setup												
0xA0	BIOZ Configuration 1[7:0]	BIOZ_DAC_OSRA[1:0]		BIOZ_ADC_OSRA[2:0]			ECG_BIOZ_BG_EN	BIOZ_EN[1:0]				
0xA1	BIOZ Configuration 2[7:0]	BIOZ_DHPF[1:0]		BIOZ_DLDPF[2:0]			-	-	EN_BIOZ_THRESH			
0xA2	BIOZ Configuration 3[7:0]	BIOZ_EXT_RES	-	BIOZ_VDRV_MAG[1:0]	BIOZ_IDRV_RGE[1:0]	BIOZ_DRV_MODE[1:0]						
0xA3	BIOZ Configuration 4[7:0]	EN_UTIL_MODE	-	-	-	-	-	-	-			
0xA4	BIOZ Configuration 5[7:0]	BIOZ_DC_CODE_SEL	BIOZ_DC_DAC_CODE[6:0]									
0xA5	BIOZ Configuration 6[7:0]	BIOZ_AHPF[3:0]				BIOZ_INA_MODE	BIOZ_DMIS	BIOZ_GAIN[1:0]				

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0xA6	BIOZ Configuration 7[7:0]	BIOZ_E_XT_CAP	BIOZ_D_C_REST_ORE	BIOZ_D_RV_RES_ET	BIOZ_D_AC_RES_ET	BIOZ_AMP_RGE[1:0]			BIOZ_AMP_BW[1:0]
0xA7	BIOZ Configuration 8[7:0]	RLD_SE_L_BIOZ	RLD_DR_V	BIOZ_C_MRES_D_IS	BIOZ_ST_BYON	BIOZ_IPOL	BIOZ_FA_ST	BIOZ_IN_A_CHOP_EN	BIOZ_C_H_FSEL
0xA8	BIOZ Low Threshold[7:0]					BIOZ_LO_THRESH[7:0]			
0xA9	BIOZ High Threshold[7:0]					BIOZ_HI_THRESH[7:0]			
BIOZ Calibration									
0xAA	BIOZ Mux Configuration 1[7:0]		BMUX_RSEL[1:0]	BMUX_BIST_EN	-	-	CONNECT_CAL_ONLY	BIOZ_MUX_EN	BIOZ_CAL_EN
0xAB	BIOZ Mux Configuration 2[7:0]		BMUX_GSR_RSEL[1:0]	GSR_LOAD_EN	-	-	-	EN_EXT_INLOAD	EN_INT_INLOAD
0xAC	BIOZ Mux Configuration 3[7:0]		BIP_ASSIGN[1:0]	BIN_ASSIGN[1:0]	DRV_P_ASSIGN[1:0]	DRV_N_ASSIGN[1:0]			
0xAD	BIOZ Mux Configuration 4[7:0]				BIST_R_ERR[7:0]				
BIOZ Lead Detect									
0xB0	BIOZ Lead Detect Configuration 1[7:0]	EN_BIOZ_LON	EN_BIOZ_LOFF	EN_EXT_BIOZ_LOFF	EN_BIOZ_DRV_OOR	BIOZ_LOFF_IPOL			BIOZ_LOFF_IMAG[2:0]
0xB1	BIOZ Lead-Off Threshold[7:0]	RESP_CG_MAG_4X		RESP(CG_MAG)[2:0]			BIOZ_LOFF_THRESH[3:0]		
BIOZ Lead Bias									
0xB4	BIOZ Lead Bias Configuration 1[7:0]	-	-	-	-	BIOZ_RBIAST_VALUE[1:0]	EN_BIOZ_RBIAST_P	EN_BIOZ_RBIAST_N	
Respiration Setup									
0xB6	Respiration Configuration 1[7:0]		CG_LPF_DUTY[2:0]		CG_CHOP_CLK[1:0]		CG_MODE[1:0]	RESP_EN	
Interrupt Enables									
0xC0	Interrupt1 Enable 1[7:0]	A_FULL_EN1	PPG_FRAME_RDY_EN1	FIFO_DATA_RDY_EN1	ALC_OVF_EN1	EXP_OVF_EN1	PPG_THRESH2_HILO_E_N1	PPG_THRESH1_HILO_E_N1	-
0xC1	Interrupt1 Enable 2[7:0]	INVALID_PPG_CFG_EN1	-	LED6_COMPBE_N1	LED5_COMPBE_N1	LED4_COMPBE_N1	LED3_COMPBE_N1	LED2_COMPBE_N1	LED1_COMPBE_N1
0xC2	Interrupt1 Enable 3[7:0]	-	-	-	FREQ_UNLOCK_EN1	FREQ_LOCK_EN1	PHASE_UNLOCK_EN1	PHASE_LOCK_EN1	-
0xC3	Interrupt1 Enable 4[7:0]	ECG_LON_EN1	-	ECG_FAST_REC_EN1	RLD_OOR_EN1	ECG_LOFF_PH_EN1	ECG_LOFF_NH_EN1	ECG_LOFF_NL_EN1	

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ADDRESS	NAME	MSB							LSB
0xC4	<u>Interrupt1 Enable 5[7:0]</u>	BIOZ_L ON_EN1	BIOZ_O VER_EN 1	BIOZ_U NDR_EN 1	BIOZ_D RVP_OF F_EN1	BIOZ_L OFF_PH _EN1	BIOZ_L OFF_PL _EN1	BIOZ_L OFF_NH _EN1	BIOZ_L OFF_NL _EN1
0xC5	<u>Interrupt2 Enable 1[7:0]</u>	A_FULL _EN2	PPG_FR AME_RD Y_EN2	FIFO_D ATA_RD Y_EN2	ALC_OV F_EN2	EXP_OV F_EN2	PPG_TH RESH2 HILO_E N2	PPG_TH RESH1 HILO_E N2	-
0xC6	<u>Interrupt2 Enable 2[7:0]</u>	INVALID PPG_C FG_EN2	-	LED6_C OMPB_E N2	LED5_C OMPB_E N2	LED4_C OMPB_E N2	LED3_C OMPB_E N2	LED2_C OMPB_E N2	LED1_C OMPB_E N2
0xC7	<u>Interrupt2 Enable 3[7:0]</u>	-	-	-	FREQ_U NLOCK_ EN2	FREQ_L OCK_EN 2	PHASE_UNLOCK _EN2	PHASE_LOCK_E N2	-
0xC8	<u>Interrupt2 Enable 4[7:0]</u>	ECG_LO N_EN2	-	ECG_FA ST_REC _EN2	RLD_OO R_EN2	ECG_LO FF_PH _EN2	ECG_LO FF_PL _EN2	ECG_LO FF_NH _EN2	ECG_LO FF_NL _EN2
0xC9	<u>Interrupt2 Enable 5[7:0]</u>	BIOZ_L ON_EN2	BIOZ_O VER_EN 2	BIOZ_U NDR_EN 2	BIOZ_D RVP_OF F_EN2	BIOZ_L OFF_PH _EN2	BIOZ_L OFF_PL _EN2	BIOZ_L OFF_NH _EN2	BIOZ_L OFF_NL _EN2
Part ID									
0xFF	<u>Part ID[7:0]</u>	PART_ID[7:0]							

Register Details

Status 1 (0x00)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL	PPG_FRAM E_RDY	FIFO_DATA _RDY	ALC_OVF	EXP_OVF	PPG_THRE SH2_HILO	PPG_THRE SH1_HILO	PWR_RDY
Reset	0	0	0	0	0	0	0	1
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

A_FULL

A_FULL is set to 1 when the FIFO has reached the threshold programmed in the FIFO_A_FULL[7:0](0x0D). This is a read-only bit and it is cleared when the Status 1 Register is read. It is also cleared when the FIFO Data Register(0x0C) is read if FIFO_STAT_CLR[3](0x0E) = 1.

A_FULL	DECODE
0	Normal operation
1	Indicates that the FIFO buffer has reached the threshold set by FIFO_A_FULL[7:0](0x0D).

PPG_FRAME_RDY

PPG_FRAME_RDY is set to 1 when a full frame conversion has completed. A frame consists of FIFO data for all the PPG ADC conversions for the sequence programmed in the MEASx (x = 1 to 6) enable registers. This is a read-only bit and it is cleared by reading the Status 1 register. It is also cleared by reading the FIFO Data register(0x0C) if FIFO_STAT_CLR[3](0x0E) = 1.

PPG_FRAME_RDY	DECODE
0	Normal operation
1	A complete PPG frame is available in the FIFO.

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FIFO_DATA_RDY bit is set to 1 when new data is available in the FIFO. This is a read-only bit and it is cleared by reading the Status 1 register. It is also cleared by reading the FIFO Data Register(0x0C) if FIFO_STAT_CLR[3](0x0E) = 1

FIFO_DATA_RDY	DECODE
0	Normal operation
1	New data is available in the FIFO

ALC_OVF

ALC_OVF is set to 1 when a dark current measurement is either under range or over range for any of the assigned PPG measurements. A measurement is over range if it is more than positive full-scale (524287), and under range if it is less than negative full-scale / 4 (-131072). This is a read-only bit, and it is cleared by reading the Status 1 register.

ALC_OVF	DECODE
0	Normal operation
1	The dark current data is over range or under range.

EXP_OVF

EXP_OVF set to 1 when an exposure measurement is either over range or under range for any of the enabled PPG measurements. A measurement is over range if it is more than positive full scale (524287) minus roughly 16384, and under range if it is lower than negative full-scale / 4 (-131072) minus roughly 16384. This is a read-only bit, and it is cleared by reading the Status 1 register.

EXP_OVF	DECODE
0	Normal operation
1	The exposure data is over range or under range.

PPG_THRESH2_HILO

PPG_THRESH2_HILO is set to 1 when the PPG ADC reading qualifies as above THRESHOLD2_UPPER[7:0](0x74) or below THRESHOLD2_LOWER[7:0](0x75). This is a read-only bit and it is cleared by reading the status 1 register (0x00).

See the Threshold Detect Function section for a complete explanation of how the PPG ADC is qualified as above or below threshold.

PPG_THRESH2_HILO	DECODE
0	ADC reading is within the threshold 2 range.
1	ADC reading is either above the THRESHOLD2_UPPER level or below the THRESHOLD2_LOWER level.

PPG_THRESH1_HILO

PPG_THRESH1_HILO is set to 1 when the PPG ADC reading qualifies as above THRESHOLD1_UPPER[7:0](0x72) or below THRESHOLD1_LOWER[7:0](0x73). This is a read-only bit and it is cleared by reading the status 1 register (0x00).

See the Threshold Detect Function section for a complete explanation of how the PPG ADC is qualified as above or below threshold.

PPG_THRESH1_HILO	DECODE
0	ADC reading is within the threshold 1 range.
1	ADC reading is either above the THRESHOLD1_UPPER level or below the THRESHOLD1_LOWER level.

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Vital-Sign AFE****PWR_RDY**

PWR_RDY is set to 1 when V_{DVDD} goes below the undervoltage lockout (UVLO) threshold, which is nominally 1.38V. If this condition occurs, all registers are reset to their POR state. This bit is not triggered by a soft-reset. This is a read-only bit and it is cleared when Status 1 register is read, or by setting SHDN[1](0x11) bit to 1.

PWR_RDY is a non-maskable interrupt, so it gets asserted on both INT1 and INT2.

Value	Decode
0	Normal operation
1	Indicates that V _{DVDD} went below the UVLO threshold.

Status 2 (0x01)

BIT	7	6	5	4	3	2	1	0
Field	INVALID_PPG_CFG	—	LED6_COMPB	LED5_COMPB	LED4_COMPB	LED3_COMPB	LED2_COMPB	LED1_COMPB
Reset	0	—	0	0	0	0	0	0
Access Type	Read Only	—	Read Only					

INVALID_PPG_CFG

INVALID_PPG_CFG is set to 1 when the PPG frame rate set by clock divider FR_CLK_DIV[14:0](0x28, 0x29) is too fast to accommodate the programmed PPG frame sequence. This is a read-only bit and it is cleared when the Status 2 register is read.

INVALID_PPG_CFG	DECODE
0	Normal operation
1	The PPG frame rate is too fast to accommodate the programmed PPG frame sequence.

LED6_COMPB

LEDn_COMPB is set to 1 when the voltage at the LEDn_DRV pin is below the LED compliance voltage (n = 1 to 6). LEDn_COMPB is a read-only bit and it is cleared when the Status 2 register is read.

LEDn_COMPB	DECODE
0	The LEDn_DRV pin has sufficient voltage to support the programmed current.
1	The LEDn_DRV pin is below the voltage needed to support the programmed current. Power supply rejection on LEDn is degraded and LEDn current is inaccurate.

LED5_COMPB

See LED6_COMPB for details.

LED4_COMPB

See LED6_COMPB for details.

LED3_COMPB

See LED6_COMPB for details.

LED2_COMPB

See LED6_COMPB for details.

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LED1_COMPB

See LED6_COMPB for details.

Status 3 (0x02)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	FREQ_UNL_OCK	FREQ_LOC_K	PHASE_UNLOCK	PHASE_LOCK	—
Reset	—	—	—	0	0	0	0	—
Access Type	—	—	—	Read Only	Read Only	Read Only	Read Only	—

FREQ_UNLOCK

FREQ_UNLOCK is set to 1 when the PLL loses the frequency lock. This is a read-only bit and is cleared by reading the Status 3 register. If the frequency unlock state persists, the FREQ_UNLOCK bit is set again.

FREQ_UNLOCK	DECODE
0	The PLL is frequency locked
1	The PLL is frequency unlocked

FREQ_LOCK

FREQ_LOCK is set to 1 when the PLL achieves frequency lock. This is a read-only bit and is cleared by reading the Status 3 register. If the PLL remains frequency locked, the FREQ_LOCK bit is set again.

FREQ_LOCK	DECODE
0	The PLL is frequency unlocked.
1	The PLL is frequency locked.

PHASE_UNLOCK

PHASE_UNLOCK is set to 1 when the PLL phase was locked and then lost its phase lock. This is a read-only bit and cleared by reading the status 3 register. If the PLL remains phase unlocked, the PHASE_UNLOCK bit is set again.

PHASE_UNLOCK	DECODE
0	The PLL is phase locked.
1	The PLL is phase unlocked.

PHASE_LOCK

PHASE_LOCK is set to 1 when the PLL achieves phase lock. This is a read-only bit and cleared by reading the status 3 register. If the PLL remains in phase lock, the PHASE_LOCK bit is set again.

PHASE_LOCK	DECODE
0	The PLL is phase unlocked.
1	The PLL is phase locked.

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Status 4 (0x03)

BIT	7	6	5	4	3	2	1	0
Field	ECG_LON	-	ECG_FAST_REC	RLD_OOR	ECG_LOFF_PH	ECG_LOFF_PL	ECG_LOFF_NH	ECG_LOFF_NL
Reset	0	-	0	0	0	0	0	0
Access Type	Read Only	-	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

ECG_LON

ECG_LON is set to 1 when the an ECG lead-on condition is detected. This is a read-only bit and is cleared by reading the Status 4 register. If the DC lead-on state persists, the ECG_LON bit is set again.

ECG_LON	DECODE
0	ECG lead-on condition has not been detected.
1	ECG lead-on condition has been detected.

ECG_FAST_REC

ECG_FAST_REC is set to 1 when the ECG fast recovery mode is engaged (either manually or automatically). This is a read-only bit and cleared by reading the Status 4 register. If the ECG fast recovery mode persists for the next ECG sample, the ECG_FAST_REC bit is set again.

ECG_FAST_REC	DECODE
0	Normal operation
1	ECG channel is in fast recovery mode

RLD_OOR

RLD_OOR is set to 1 when the right leg drive voltage has been out of range (< 0.26V or > 1.26V) for more than 128 ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1.

The delay is bypassed if BYP_DLY[7](0x12) is set to 1.

This is a read-only bit and is cleared by reading the Status 4 register. If the right leg drive voltage out of range condition persists, the RLD_OOR bit is set again.

RLD_OOR	DECODE
0	Normal operation
1	Right leg drive voltage is out of range.

ECG_LOFF_PH

ECG_LOFF_PH is set to 1 when the ECGP voltage has been greater than V_{ECG_TH_H} for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1.

The delay is bypassed if BYP_DLY[7](0x12) is set to 1.

V_{ECG_TH_H} is set by ECG_LOFF_THRESH[3:0](0x89).

This is a read-only bit and it is cleared by reading the Status 4 register. If the lead-off condition for ECG_LOFF_PH persists, this bit is set again.

ECG_LOFF_PH	DECODE
0	Normal operation
1	The ECGP voltage is higher than V _{ECG_TH_H}

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ECG_LOFF_PL

ECG_LOFF_PL is set to 1 when the ECGP voltage has been less than $V_{ECG_TH_L}$ for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1.

The delay is bypassed if BYP_DLY[7](0x12) is set to 1.

$V_{ECG_TH_L}$ is set by ECG_LOFF_THRESH[3:0](0x89).

This is a read-only bit and it is cleared by reading the Status 4 register. If the lead-off condition for ECG_LOFF_PL persists, this bit is set again.

ECG_LOFF_PL	DECODE
0	Normal operation
1	The ECGP voltage is lower than $V_{ECG_TH_L}$

ECG_LOFF_NH

ECG_LOFF_NH is set to 1 when the ECGN voltage has been greater than $V_{ECG_TH_H}$ for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1.

The delay is bypassed if BYP_DLY is set to 1.

$V_{ECG_TH_H}$ is set by ECG_LOFF_THRESH[3:0](0x89).

This is a read-only bit and it is cleared by reading the Status 4 register. If the lead-off condition for ECG_LOFF_NH persists, this bit is set again.

ECH_LOFF_NH	DECODE
0	Normal operation
1	The ECGN voltage is higher than V_{LOFF_TH+}

ECG_LOFF_NL

ECG_LOFF_NL is set to 1 when the ECGN voltage has been less than $V_{ECG_TH_L}$ for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1.

The delay is bypassed if BYP_DLY[7](0x12) is set to 1.

$V_{ECG_TH_L}$ is set by ECG_LOFF_THRESH[3:0](0x89).

This is a read-only bit and it is cleared by reading the Status 4 register. If the lead-off condition for ECG_LOFF_NL persists, this bit is set again.

ECG_LOFF_NL	DECODE
0	Normal operation
1	The ECGN voltage is lower than $V_{ECG_TH_L}$

Status 5 (0x04)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_LON	BIOZ_OVER	BIOZ_UNDR	BIOZ_DRV_OOR	BIOZ_LOFF_PH	BIOZ_LOFF_PL	BIOZ_LOFF_NH	BIOZ_LOFF_NL
Reset	0	0	0	0	0	0	0	0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BIOZ_LON

BIOZ_LON is set to 1 when a BioZ lead-on condition is detected. This is a read-only bit and is cleared by reading the Status 5 register. If the BioZ lead-on condition persists, the BIOZ_LON bit is set again.

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BIOZ_LON	DECODE
0	BioZ lead-on condition has not been detected.
1	BioZ lead-on condition has been detected.

BIOZ_OVER

BIOZ_OVER is set to 1 when the absolute value of the BioZ ADC reading has exceeded the BioZ high threshold set by register BIOZ_HI_THRESH[7:0](0xA9) for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1. This bit is cleared when the Status 5 register is read. If the BIOZ_OVER condition persists at the end of next BioZ sample, the bit is set to 1 again.

BIOZ_OVER	DECODE
0	Normal operation
1	BIOZ_HI_THRESH has been exceeded

BIOZ_UNDR

BIOZ_UNDR is set to 1 when the absolute value of the BioZ ADC reading has been below the BIOZ Low Threshold set by register BIOZ_LO_THRESH[7:0](0xA8) for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1. This bit is cleared when the Status 5 register is read. If the BIOZ_UNDR condition persists at the end of the next BioZ sample, the bit is set to 1 again.

BIOZ_UNDER	DECODE
0	Normal operation
1	BIOZ_LO_THRESH has been exceeded

BIOZ_DRV_OOR

BIOZ_DRV_OOR is set to 1 when the BioZ DRVN voltage peaks have been out of range (< 0.2V or > (VAVDD - 0.2V)) for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1.

The delay is bypassed if BYP_DLY[7](0x12) is set to 1.

This bit is cleared when the Status 5 register is read. If the BioZ drive out-of-range condition persists, this bit continues to remain asserted.

BIOZ_DRV_OOR	DECODE
0	Normal operation
1	DRVN is out of range

BIOZ_LOFF_PH

BIOZ_LOFF_PH is set to 1 when the BIP voltage has been greater than V_{BIOZ_TH_H} for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1.

The delay is bypassed if BYP_DLY[7](0x12) is set to 1.

V_{BIOZ_TH_H} is set by BIOZ_LOFF_THRESH[3:0](0xB1).

This is a read-only bit and it is cleared by reading the Status 5 register. If the lead-off condition for BIOZ_LOFF_PH persists, this bit is set again.

BIOZ_LOFF_PH	DECODE
0	Normal operation
1	The BIP voltage is greater than V _{BIOZ_TH_H}

BIOZ_LOFF_PL

BIOZ_LOFF_PL is set to 1 when the BIP voltage has been less than V_{BIOZ_TH_L} for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1.

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The delay is bypassed if BYP_DLY[7](0x12) is set to 1.

$V_{BIOZ_TH_L}$ is set by BIOZ_LOFF_THRESH[3:0](0xB1).

This is a read-only bit and it is cleared by reading the Status 5 register. If the lead-off condition for BIOZ_LOFF_PL persists, this bit is set again.

		DECODE
0	Normal operation	
1	The BIP voltage is lower than $V_{BIOZ_TH_L}$	

BIOZ_LOFF_NH

BIOZ_LOFF_NH is set to 1 when the BIN voltage has been greater than $V_{BIOZ_TH_H}$ for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1.

The delay is bypassed if BYP_DLY[7](0x12) is set to 1.

$V_{BIOZ_TH_H}$ is set by BIOZ_LOFF_THRESH[3:0](0xB1).

This is a read-only bit and it is cleared by reading the Status 5 register. If the lead-off condition for BIOZ_LOFF_NH persists, this bit is set again.

		DECODE
0	Normal operation	
1	The BIN voltage is higher than $V_{BIOZ_TH_H}$	

BIOZ_LOFF_NL

BIOZ_LOFF_NL is set to 1 when the BIN voltage has been less than $V_{BIOZ_TH_L}$ for more than 128ms if CLK_FREQ_SEL = 0, or 125ms if CLK_FREQ_SEL = 1.

The delay is bypassed if BYP_DLY[7](0x12) is set to 1.

$V_{BIOZ_TH_L}$ is set by BIOZ_LOFF_THRESH[3:0](0xB1).

This is a read-only bit and it is cleared by reading the Status 5 register. If the lead-off condition for BIOZ_LOFF_NL persists, this bit is set again.

		DECODE
0	Normal operation	
1	The BIN voltage is lower than $V_{BIOZ_TH_L}$	

FIFO Write Pointer (0x08)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_WR_PTR[7:0]							
Reset	0x00							
Access Type	Read Only							

FIFO_WR_PTR

FIFO_WR_PTR points to the FIFO location where the next sample will be written. This pointer advances for each sample pushed on to the circular FIFO. The write pointer wraps around to count 0x00 as the next FIFO location after count 0xFF.

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BIT	7	6	5	4	3	2	1	0
Field	FIFO_RD_PTR[7:0]							
Reset	0x00							
Access Type	Write, Read, Dual							

FIFO_RD_PTR

FIFO_RD_PTR points to the FIFO location from which the next sample is to be read through the serial interface. This pointer advances each time a sample is read from the circular FIFO. The read pointer can be both read and written to. This allows rereading (or retrying) samples from the FIFO. However, writing to FIFO_RD_PTR can have adverse effects if it results in the FIFO being almost full. The read pointer wraps around to count 0x00 after count 0xFF.

FIFO Counter 1 (0x0A)

BIT	7	6	5	4	3	2	1	0	
Field	FIFO_DATA_COUNT[8]	OVF_COUNTER[6:0]							
Reset	0x0	0x00							
Access Type	Read Only	Read Only							

FIFO_DATA_COUNT

FIFO_DATA_COUNT[8](0x0A) is a read-only bit which holds the most significant bit of the number of items available in the FIFO for the host to read. The lower 8 bits are in the FIFO_DATA_COUNT[7:0](0x0B) register.

FIFO_DATA_COUNT[8:0] increments when a new item is pushed to the FIFO, and decrements when the host reads an item from the FIFO.

FIFO_DATA_COUNT[8:0] is useful for debug.

OVF_COUNTER

The overflow counter OVF_COUNTER logs the number of samples lost if the FIFO is not read in a timely fashion. When FIFO is full any new samples results in either new or old samples getting lost depending on the FIFO_RO[1](0x0E) setting.

This is a read-only register. When a complete sample is read from FIFO and the read pointer advances, the OVF_COUNTER is reset to zero. It should be read immediately before reading the FIFO in order to check if an overflow condition has occurred. This counter saturates at count value 0x7F.

FIFO Counter 2 (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA_COUNT[7:0]							
Reset	0x00							
Access Type	Read Only							

FIFO_DATA_COUNT

FIFO_DATA_COUNT[7:0] is a read-only register that holds the lower 8 bits of the number of items available in the FIFO for the host to read.

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See the FIFO_DATA_COUNT[8](0x0A) description for details.

FIFO Data Register (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA[7:0]							
Reset	0xFF							
Access Type	Read Only							

FIFO_DATA

FIFO_DATA is used to get data from the FIFO using burst reads only. When burst reading from this register, the register address pointer does not auto-increment, and the FIFO_RD_PTR[7:0](0x09) advances to provide subsequent samples. Each sample is three bytes, so burst reading three bytes in the FIFO_DATA register through the serial interface advances the FIFO_RD_PTR by one count. The format and data type of the data stored in the FIFO is determined by the tag associated with the data. For details and examples of various data types in some use cases, see the FIFO Description section. This is a read-only register.

FIFO Configuration 1 (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_A_FULL[7:0]							
Reset	0x7F							
Access Type	Write, Read							

FIFO_A_FULL

FIFO_A_FULL sets the high-water mark for the FIFO and determines when status bit A_FULL[7](0x00) is asserted. The A_FULL bit is asserted when the FIFO holds (256 - FIFO_A_FULL) samples. For example, if set to 0x0F, A_FULL is asserted when there are 15 empty spaces left (241 samples in FIFO). If A_FULL_EN1[7](0xC0) or A_FULL_EN2[7](0xC5) is set to 1, then A_FULL being asserted results in an interrupt on the corresponding interrupt pin (INT1 or INT2). This condition should prompt the processor to read samples from the FIFO before it fills and overflows. The A_FULL bit is cleared and the interrupt is deasserted when the Status 1 register (0x00) is read.

FIFO_A_FULL	Free Spaces Before Interrupt is Asserted	Number of Samples in FIFO
0x00	0	256
0x01	1	255
0x02	2	254
0x03	3	253
----	----	----
0xFE	254	2
0xFF	255	1

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FIFO Configuration 2 (0x0E)

BIT	7	6	5	4	3	2	1	0
Field	-	-	FIFO_MARK	FLUSH_FIFO	FIFO_STAT_CLR	A_FULL_TYPE	FIFO_RO	-
Reset	-	-	0	0	1	0	0	-
Access Type	-	-	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	-

FIFO_MARK

When FIFO_MARK is set to 1, a marker tag is pushed to the FIFO. FIFO_MARK is a self clearing bit. The marker tag is useful for differentiating the data in the FIFO before and after the tag.

See the FIFO Description section for the marker tag information.

Value	Decode
0	Normal data saved in FIFO
1	Marker saved in FIFO

FLUSH_FIFO

When the FLUSH_FIFO bit is set to 1, the FIFO is flushed, and FIFO_WR_PTR[7:0](0x08), FIFO_RD_PTR[7:0](0x09), FIFO_DATA_COUNT[8:0](0x0A, 0x0B) and OVF_COUNTER[6:0](0x0A) are reset to zero. The contents of the FIFO are lost. FLUSH_FIFO is a self-clearing bit.

Value	Decode
0	Normal mode
1	FIFO is flushed

FIFO_STAT_CLR

FIFO_STAT_CLR determines if a FIFO_DATA[7:0](0x0C) register read clears the status bits A_FULL[7](0x00), PPG_FRAME_RDY[6](0x00), FIFO_DATA_RDY[5](0x00), and their corresponding interrupts.

Value	Decode
0	A_FULL, PPG_FRAME_RDY, and FIFO_DATA_RDY status and interrupts do not get cleared by a FIFO_DATA[7:0](0x0C) register read. They get cleared by a Status 1 register read.
1	A_FULL, PPG_FRAME_RDY, and FIFO_DATA_RDY status and interrupts get cleared by a FIFO_DATA[7:0](0x0C) register read or a Status 1 register read.

A_FULL_TYPE

A_FULL_TYPE defines the behavior of status bit A_FULL[7](0x00) and its corresponding interrupt. When A_FULL_TYPE is set to 0, A_FULL is asserted every time the FIFO almost-full condition is detected. When A_FULL_TYPE is set to 1, A_FULL is asserted only for any new almost full condition.

Value	Decode
0	A_FULL interrupt gets asserted when the almost full condition is detected. It is cleared by a Status 1 register read, but reasserts for every sample if the almost-full condition persists.
1	A_FULL interrupt gets asserted when the almost-full condition is detected. The interrupt gets cleared by a Status 1 register read, and does not reassert until the FIFO is read and then a new almost-full condition is detected.

FIFO_RO

FIFO_RO bit controls the behavior of the FIFO when the FIFO becomes completely filled with data. Push to FIFO is enabled when FIFO is full if FIFO_RO is set to 1 and old samples are lost. Both FIFO Write Pointer (0x08) and FIFO Read Pointer (0x09) increment for each sample after the FIFO is full. If FIFO_RO is set to 0, new samples are lost and

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the FIFO is not updated. FIFO Write Pointer and FIFO Read Pointer do not increment until a sample is read from the FIFO.

Value	Decode
0	The FIFO stops on full.
1	The FIFO automatically rolls over on full.

System Sync (0x10)

BIT	7	6	5	4	3	2	1	0
Field	TIMING_SYS_RESET	–	–	–	–	–	–	–
Reset	0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

TIMING_SYS_RESET

TIMING_SYS_RESET works together with the TRIG_FCFG[7:5](0x13) bit to synchronize the timing subsystems of multiple AFEs.

Setting the TIMING_SYS_RESET to 1 resets the BIOZ_NDIV[7:6](0x1A), ECG_NDIV[10:0](0x1B, 0x1C), and ECG_FDIV[2:0](0x1B) dividers.

See the PLL Synchronization section for a description of how to configure the PLL master-slave operation.

TIMING_SYS_RESET is a self clearing bit.

TIMING_SYS_RESET	DECODE
0	Normal mode
1	Reset pulse is sent on TRIG if PLL is locked, and TRIG_FCFG = 0x2.

System Configuration 1 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	–	DISABLE_I2C	ECG_PPG_TIMING_DATA	BIOZ_PPG_TIMING_DATA	ECG_BIOZ_TIMING_DATA	–	SHDN	RESET
Reset	–	0	0	0	0	–	0	0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read

DISABLE_I2C

When DISABLE_I2C is set to 0 (default), the part uses the I²C or SPI serial interface depending on the state of the CSB/I2C_SEL pin. When DISABLE_I2C is set to 1, the part uses the SPI serial interface.

For SPI interface, users must set this DISABLE_I2C to 1 during initialization after powerup. See the Digital Interface section for more information.

DISABLE_I2C	DECODE
0	CSB/I2C_SEL pin selects interface
1	Part uses SPI interface only

ECG_PPG_TIMING_DATA

ECG_PPG_TIMING_DATA enables saving the time delay between the ECG sample pushed to the FIFO and the start

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of the next PPG measurement. ECG-to-PPG timing data is identified by a specific tag. For information on PPG timing data format and tag, see the FIFO Description section. For details on ECG-to-PPG timing data and some examples, see the ECG-to-PPG Timing Data section.

When both ECG and PPG are enabled and ECG_PPG_TIMING_DATA is set to 1, the PPG frame rate uses the ECG ADC clock. Since ECG_PPG_TIMING_DATA changes the PPG frame-rate clock selection, this bit should be modified before enabling PPG using the MEAS_x_EN (x = 1 to 6) registers.

If ECG is not enabled, the ECG-to-PPG timing data is not saved in the FIFO.

ECG_PPG_TIMING_DATA	DECODE
0	ECG-to-PPG timing data is not saved in the FIFO.
1	ECG-to-PPG timing data is saved in FIFO if both PPG and ECG are enabled.

BIOZ_PPG_TIMING_DATA

BIOZ_PPG_TIMING_DATA enables saving timing delay between the BioZ sample pushed to the FIFO and the start of the next PPG measurement. BioZ-to-PPG timing data is identified by a specific tag. For information on data format and tag, see the FIFO Description section. For details on BioZ-to-PPG timing data and some examples, see the BioZ-to-PPG Timing Data section.

When both BioZ and PPG are enabled and BIOZ_PPG_TIMING_DATA is set to 1, the PPG frame rate uses the BioZ-ADC clock. Since BIOZ_PPG_TIMING_DATA changes the PPG frame-rate clock selection, this bit should be modified before enabling PPG using the MEAS_x_EN (x = 1 to 6) registers. If BioZ is not enabled, the BioZ-to-PPG timing data is not saved in the FIFO.

When ECG, BioZ, and PPG are all enabled and both ECG_PPG_TIMING_DATA and BIOZ_PPG_TIMING_DATA are set to 1, the PPG frame rate uses the ECG-ADC clock.

BIOZ_PPG_TIMING_DATA	DECODE
0	BioZ-to-PPG timing data is not saved in the FIFO.
1	BioZ-to-PPG timing data is saved in the FIFO if both PPG and BioZ are enabled.

ECG_BIOZ_TIMING_DATA

ECG_BIOZ_TIMING_DATA enables saving the time delay between the ECG sample being pushed to the FIFO and the next BioZ sample being pushed to the FIFO. ECG to BioZ timing data is identified by a specific tag. For information on data format and tag, see FIFO Description. For details on ECG to BioZ timing data and some examples, see ECG to BIOZ Timing Data.

If ECG or BioZ is not enabled, the ECG to BioZ timing data is not saved in the FIFO.

ECG_BIOZ_TIMING_DATA	DECODE
0	ECG to BioZ timing data is not saved in FIFO
1	ECG to BioZ timing data is saved in FIFO if both ECG and BioZ are enabled.

SHDN

Setting SHDN to 1 puts the MAX86178 into shutdown mode. While in shutdown mode, all configuration registers retain their values and write/read operations function normally. All interrupts are cleared to zero in this mode. Also in this mode, the oscillator is shut down and the part draws minimum current. If this bit is asserted during an active conversion, then the conversion is aborted. Set SHDN to 0 to put the part back in normal mode. See the Shutdown Sequence section for more details.

SHDN	DECODE
0	Normal mode
1	Shutdown mode

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RESET

Setting RESET to 1 resets all registers to their power-on-reset state. This is a self-clearing bit and resets to 0 after the reset sequence is completed.

RESET	DECODE
0	Normal mode
1	All registers restored to power-on-reset state

System Configuration 2 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	BYP_DLY	–	–		ECG_SAMP_SYNC_FREQ[4:0]			
Reset	0	–	–			0x00		
Access Type	Write, Read	–	–			Write, Read		

BYP_DLY

BYP_DLY bypasses the delays associated with the status bits in the Status 4 (0x03) and Status 5 (0x04) registers. These status bits are the threshold, lead-on, and lead-off features of the ECG and BioZ channels.

BYP_DLY	DECODE
0	Normal operation
1	ECG and BioZ status delays bypassed

ECG_SAMP_SYNC_FREQ

ECG_SAMP_SYNC_FREQ divides the ECG sample rate by the ratio shown in the decode table and outputs a sample sync pulse on TRIG when TRIG_FCFG = 0x3. The sample sync pulse width is equal to a quarter of the original ECG sample-rate period.

ECG_SAMP_SYNC_FREQ	DIVIDER
0x00	1
0x01	2
0x02	3
...	...
0x1C	29
0x1D	30
0x1E	31
0x1F	32

Pin Functional Configuration (0x13)

BIT	7	6	5	4	3	2	1	0	
Field	TRIG_FCFG[2:0]				TRIG_ICFG	INT2_FCFG[1:0]			
Reset	0x0				0	0x0			
Access Type	Write, Read				Write, Read	Write, Read			

TRIG_FCFG

TRIG_FCFG controls the function of the TRIG pin. (See the PLL Synchronization Using TRIG Pin section in the detailed

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description.)

When TRIG_FCFG is set to 0x0 and PPG_SYNC_MODE[5](0x21) = 1, the TRIG input pin is used for external PPG frame sync. In this mode the device is in one-shot mode for PPG measurements. A frame cycle begins upon receipt of an active edge on the TRIG input (see TRIG_ICFG[1](0x13)).

When TRIG_FCFG is set to 0x1, the device is a slave for PLL synchronization. When PLL_EN is set to 1, the TRIG signal is used to receive a timing-system reset pulse to synchronize the PLLs on one or more AFEs. The master and slave reset the ECG_NDIV, ECG_FDIV, and BIOZ_NDIV counters on the next rising edge of FCLK after the reset pulse rising edge.

When TRIG_FCFG is set to 0x2, the device is a master for PLL synchronization and together with the TIMING_SYS_RESET bit it is used to synchronize the timing subsystems of multiple AFEs.

When TRIG_FCFG is set to 0x3, the device outputs the ECG Sample Sync pulse on the TRIG pin at the frequency programmed in ECG_SAMP_SYNC_FREQ. These pulses can be used for synchronizing other devices to the ECG sample rate. The width of the sync pulse is 1/4 of the ECG sample period.

When TRIG_FCFG is set to 0x4, the device outputs the LED_TX pulse on the TRIG pin. LED_TX is asserted 500ns before any of the six LED Driver pins, LEDn_DRV (n = 1 to 6) gets asserted. This feature is useful in combination with the MAX20345 boost converter to switch it from a fully "off" state to a fully "on" state; thus, reducing the boost quiescent power and the effects of boost ripple on the MAX86178.

If the broadcast feature is used for synchronizing timing subsystems of multiple AFEs, TRIG_FCFG = 0x2 or 0x3 is ignored, and the TRIG pin can be used for other purposes mentioned above.

TRIG_FCFG[2:0]	Pin Direction	Description
0b000	Input	The TRIG pin is used for external frame synchronization for PPG. See the PPG_SYNC_MODE description
0b001	Input	The TRIG pin is used for PLL synchronization in the slave device
0b010	Output	The TRIG pin is used for PLL synchronization in the master device
0b011	Output	The TRIG pin is used for ECG sample-sync pulses
0b100	Output	The TRIG pin outputs the LED_TX pulse

TRIG_ICFG

TRIG_ICFG sets the input active edge of the TRIG pin.

TRIG_ICFG	DECODE
0	The TRIG pin active edge is falling.
1	The TRIG pin active edge is rising.

INT2_FCFG

INTx_FCFG (x = 1, 2) controls the function of the corresponding INTx pin.

INTx_FCFG (x = 1, 2)	DECODE
0x0	INTx is disabled
0x1	INTx is enabled and is cleared by reading the corresponding status register or FIFO as applicable.
0x2	INTx is enabled and gets cleared automatically after 30.5µs, or by reading the corresponding status register or FIFO as applicable.
0x3	INTx is enabled and gets cleared automatically after 244µs, or by reading the corresponding status register or FIFO as applicable.

INT1_FCFG

See INT2_FCFG for details.

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Output Pin Configuration (0x14)

BIT	7	6	5	4	3	2	1	0
Field	TRIG_OCFG[1:0]	–	–	INT2_OCFG[1:0]	INT1_OCFG[1:0]	–	–	–
Reset	0x0	–	–	0x0	0x0	–	–	–
Access Type	Write, Read	–	–	Write, Read	Write, Read	–	–	–

TRIG_OCFG

TRIG_OCFG selects the output drive type for the TRIG pin.

TRIG_OCFG	TRIG OUTPUT DRIVE TYPE
0x0	Open-drain, active-low output.
0x1	Active drive to IOVDD and DGND; the active level is a high output.
0x2	Active drive to IOVDD and DGND; the active level is a low output.
0x3	Do not use.

INT2_OCFG

INTx_OCFG ($x = 1, 2$) selects the output drive type for the corresponding INTx pin.

INTx_OCFG ($x = 1, 2$)	INTx OUTPUT DRIVE TYPE
0x0	Open-drain, active-low output.
0x1	Active drive to IOVDD and DGND; the active level is a high output.
0x2	Active drive to IOVDD and DGND; the active level is a low output.
0x3	Do not use.

INT1_OCFG

See INT2_OCFG for details.

I2C Broadcast Address (0x15)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	I2C_BCAST_ADDR[6:0]	–	–	I2C_BCAST_EN
Reset	–	–	–	–	0x00	–	–	0
Access Type	–	–	–	–	Write, Read	–	–	Write, Read

I2C_BCAST_ADDR

I2C_BCAST_ADDR is used to define the upper 7 bits of the I²C address in I²C broadcast mode (I2C_BCAST_EN = 1) when writing to multiple devices simultaneously using the I²C serial interface. I2C_BCAST_ADDR is ignored in SPI mode.

See the I²C Broadcast section for more details.

I2C_BCAST_EN

I2C_BCAST_EN enables write transactions to multiple devices using the broadcast address programmed in I2C_BCAST_ADDR in I²C mode. I²C read transactions are not supported when I2C_BCAST_ADDR is used.

Note that for devices using SPI for serial interface, broadcast write transactions can be achieved by driving the CSB

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pins low on multiple devices at the same time.

I2C_BCAST_EN	DECODE
0	Normal mode. I ² C transactions are for one device only.
1	I ² C broadcast mode. Write transactions to multiple devices are enabled.

PLL Configuration 1 (0x18)

BIT	7	6	5	4	3	2	1	0
Field	MDIV[9:8]	–	–	–	–	–	PLL_LOCK_WNDW	PLL_EN
Reset	0x1	–	–	–	–	–	0	0
Access Type	Write, Read	–	–	–	–	–	Write, Read	Write, Read

MDIV

MDIV[9:0] multiplies the REF_CLK by MDIV + 1 to set the frequency of the PLL. MDIV[9:8] are the 2 MSBs of MDIV[9:0]. The lower 8 bits are in MDIV[7:0].

MDIV must be set such that PLL_CLK is between 4.0MHz and 28.0MHz.

For information on how to set MDIV[9:0] see the Timing Subsystem section.

PLL_LOCK_WNDW

PLL_LOCK_WNDW selects the time window for the PLL phase lock detector. The PLL lock detector compares the rising edges of FCLK and the output of the M divider, and determines the PLL to be locked if the difference between the two is less than PLL_LOCK_WNDW. Setting PLL_LOCK_WNDW = 1 helps to avoid false PHASE_UNLOCK interrupts when the FCLK reference has high jitter.

PLL_LOCK_WNDW	PLL PHASE LOCK WINDOW
0	1 PLL clock period
1	2 PLL clock periods (recommended when using high-jitter FCLK input)

PLL_EN

PLL_EN enables the internal PLL, which multiplies the reference clock to a frequency between 4MHz and 28MHz. For details on the timing subsystem with PLL enabled, see the Timing Subsystem section. PLL_EN must be set to 1 before enabling ECG or BioZ measurements.

PLL_EN	DECODE
0	PLL is disabled
1	PLL is enabled

PLL Configuration 2 (0x19)

BIT	7	6	5	4	3	2	1	0
Field	MDIV[7:0]	–	–	–	–	–	–	–
Reset	0xBB	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

MDIV

MDIV[7:0] are the 8 LSBs of MDIV[9:0]

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See the MDIV[9:8] register for details.

PLL Configuration 3 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_NDIV[1:0]		—	—		BIOZ_KDIV[3:0]		
Reset	0x0		—	—		0x0		
Access Type	Write, Read		—	—		Write, Read		

BIOZ_NDIV

BIOZ_NDIV divides down the PLL clock as shown in the table below and sets the clock for the BioZ ADC.

For information on how to set BIOZ_NDIV see the Timing Subsystem section.

BIOZ_NDIV	BioZ N-Divider
0x0	256
0x1	512
0x2	1024
0x3	1024

BIOZ_KDIV

BIOZ_KDIV divides down the PLL clock as shown in the table below and sets the clock for the DDS DAC.

For information on how to set BIOZ_KDIV see the Timing Subsystem section.

BIOZ_KDIV	BIOZ K DIVIDER
0x0	1
0x1	2
0x2	4 (See Note)
0x3	8
0x4	16
0x5	32
0x6	64
0x7	128
0x8	256
0x9	512
0xA	1024
0xB	2048
0xC	4096
0xD	8192
0xE	8192
0xF	8192

Note: this setting results in a larger offset in the receive channel. If a calibration is applied to the measurement, this effect is negated by the offset measurement and subtraction. If no calibration is applied and accurate impedance is desired, it is recommended to avoid using this setting, and instead adjusting MDIV by a factor of two to achieve the desired frequency with a different BIOZ_KDIV setting.

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BIT	7	6	5	4	3	2	1	0
Field	ECG_NDIV[10:8]				–	–	ECG_FDIV[2:0]	
Reset	0x1				–	–	0x0	
Access Type	Write, Read, Dual				–	–	Write, Read	

ECG_NDIV

ECG_NDIV[10:0] divides the PLL clock according to the table below, and together with ECG_FDIV[2:0] sets the clock for the ECG ADC.

ECG_NDIV[10:8] are the most significant bits of 11-bit ECG_NDIV[10:0]. The lower 8 bits are in ECG_NDIV[7:0](0x1C). ECG_NDIV[10:0] can be set to any value between 16 and 2047. If a value smaller than 16 is written, it is automatically overwritten to 16.

For information on how to set ECG_NDIV[10:0] see the Timing Subsystem section.

ECG_NDIV[10:0]	ECG N DIVIDER
0x000 to 0x00F	16
0x010	16
0x011	17
0x012	18
...	...
0x7FE	2046
0x7FF	2047

ECG_FDIV

ECG_FDIV along with ECG_NDIV divide the PLL clock to provide an ECG ADC clock. When respiration mode is enabled (RESP_EN = 1), ECG_FDIV also divides the respiration sampling rate.

When ECG_EN = 1 or RESP_EN = 1, ECG_FDIV must be non-zero.

For information on how to set ECG_FDIV see the Timing Subsystem section.

ECG_FDIV	ECG F DIVIDER
0x0	ECG_ADC_CLK disabled
0x1	1
0x2	2
0x3	4
0x4	8
0x5	16
0x6	16
0x7	16

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PLL Configuration 5 (0x1C)

BIT	7	6	5	4	3	2	1	0
Field	ECG_NDIV[7:0]							
Reset	0x3F							
Access Type	Write, Read, Dual							

ECG_NDIV

ECG_NDIV[7:0] has the lower 8 bits of 11-bit ECG_NDIV[10:0].

See ECG_NDIV[10:8] for details.

PLL Configuration 6 (0x1D)

BIT	7	6	5	4	3	2	1	0			
Field	-	REF_CLK_SEL	CLK_FREQ_SEL	CLK_FINE_TUNE[4:0]							
Reset	-	0	1	0x00							
Access Type	-	Write, Read	Write, Read	Write, Read							

REF_CLK_SEL

REF_CLK_SEL selects the reference clock (REF_CLK) for the PLL. The reference clock is either external on FCLK (REF_CLK_SEL = 1) or an internal oscillator (REF_CLK_SEL = 0).

REF_CLK_SEL	DECODE
0	Internal 32.0kHz or 32.768kHz oscillator used for REF_CLK
1	External oscillator used for REF_CLK

CLK_FREQ_SEL

CLK_FREQ_SEL selects the PLL reference-clock frequency. When using the internal oscillator (REF_CLK_SEL = 0), this bit sets the frequency of the internal oscillator. When using an external clock on the FCLK pin (REF_CLK_SEL = 1), this bit must match the frequency of the external clock. This bit sets the internal timing durations according to the clock frequency.

CLK_FREQ_SEL	DECODE
0	PLL reference clock is 32.0kHz
1	PLL reference clock is 32.768kHz

CLK_FINE_TUNE

CLK_FINE_TUNE is used to fine-tune the internal slow oscillator. This is accomplished by measuring the time between interrupts using a microcontroller, crystal-based real-time oscillator as a reference and computing the error in the time between interrupts. CLK_FINE_TUNE is a 2's complement code with a resolution of 0.2% per LSB. The total range is +3.0% to -3.2% around the factory trimmed value.

CLK_FINE_TUNE	SHIFT IN FREQUENCY (%)	CLK_FINE_TUNE	SHIFT IN FREQUENCY(%)
0x00	0.0	0x10	-3.2
0x01	0.2	0x11	-3.0
0x02	0.4	0x12	-2.8
0x03	0.6	0x13	-2.6

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CLK_FINE_TUNE	SHIFT IN FREQUENCY (%)	CLK_FINE_TUNE	SHIFT IN FREQUENCY(%)
0x04	0.8	0x14	-2.4
0x05	1.0	0x15	-2.2
0x06	1.2	0x16	-2.0
0x07	1.4	0x17	-1.8
0x08	1.6	0x18	-1.6
0x09	1.8	0x19	-1.4
0x0A	2.0	0x1A	-1.2
0x0B	2.2	0x1B	-1.0
0x0C	2.4	0x1C	-0.8
0x0D	2.6	0x1D	-0.6
0x0E	2.8	0x1E	-0.4
0x0F	3.0	0x1F	-0.2

PPG Configuration 1 (0x20)

BIT	7	6	5	4	3	2	1	0
Field	—	—	MEAS6_EN	MEAS5_EN	MEAS4_EN	MEAS3_EN	MEAS2_EN	MEAS1_EN
Reset	—	—	0	0	0	0	0	0
Access Type	—	—	Write, Read					

MEAS6_EN

See MEAS1_EN for details.

MEAS5_EN

See MEAS1_EN for details.

MEAS4_EN

See MEAS1_EN for details.

MEAS3_EN

See MEAS1_EN for details.

MEAS2_EN

See MEAS1_EN for details.

MEAS1_EN

MEAS_x_EN (x = 1 to 6) enables or disables the PPG measurement programmed in the corresponding PPG MEAS_x Setup registers.

MEAS_x_EN (x = 1 to 6)	Decode
0	Measurement x is disabled
1	Measurement x is enabled

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PPG Configuration 2 (0x21)

BIT	7	6	5	4	3	2	1	0
Field	-	-	PPG_SYNC_MODE	-	PPG2_PWRDN	PPG1_PWRDN	-	-
Reset	-	-	0	-	0	0	-	-
Access Type	-	-	Write, Read	-	Write, Read	Write, Read	-	-

PPG_SYNC_MODE

PPG_SYNC_MODE selects the PPG frame synchronization mode.

PPG_SYNC_MODE	Operating Modes	Description
0	Internal frame sync	The device is in free-running mode. Frame-sync pulses are generated internally by PPG_FR_CLK and the frame rate divider set by FR_CLK_DIV[14:0](0x28, 0x29).
1	External frame sync	The device is in one-shot mode for PPG measurements. A frame cycle begins upon receipt of an active edge on the TRIG input. A frame cycle consists of a powerup cycle and the execution of each enabled measurement. In this mode, TRIG_FCFG[7:5](0x13) must be set to 0x0.

PPG2_PWRDN

PPG2_PWRDN enables or disables PPG channel 2.

PPG2_PWRDN	Decode
0	PPG channel 2 is enabled.
1	PPG channel 2 is powered down.

PPG1_PWRDN

PPG1_PWRDN enables or disables PPG channel 1.

PPG1_PWRDN	Decode
0	PPG channel 1 is enabled
1	PPG channel 1 is powered down

PPG Configuration 3 (0x22)

BIT	7	6	5	4	3	2	1	0
Field	-	SMP_AVE[2:0]		ALC_DISABLE	-	COLLECT_RAW_DATA		MEAS1_CONFIG_SEL
Reset	-	0x0		0	-	0	-	0
Access Type	-	Write, Read		Write, Read	-	Write, Read	Write, Read	

SMP_AVE

SMP_AVE sets the number of adjacent samples from each individual PPG channel that are averaged on-chip before being written to the FIFO. SMP_AVE must be programmed to 0 when Threshold Interrupts are enabled or when External Frame Sync is used.

SMP_AVE	Number of Samples Averaged
0x0	1 (No averaging)

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SMP_AVE	Number of Samples Averaged
0x1	2
0x2	4
0x3	8
0x4 to 0x7	16

ALC_DISABLE

ALC_DISABLE disables the front-end analog ambient-light cancelation circuit for PPG measurements. This bit does not alter the digital ambient-light cancelation.

ALC_DISABLE	Decode
0	Normal operation
1	Front-end analog ambient-light cancelation is disabled.

COLLECT_RAW_DATA

COLLECT_RAW_DATA pushes each ambient conversion and exposure conversion within a PPG measurement to the FIFO, separately. Setting COLLECT_RAW_DATA to 1 inhibits the digital ambient cancelation. This allows for a customized ambient rejection algorithm to be run in a host processor.

When COLLECT_RAW_DATA is set to 1, PROX_AUTO[3](0x23), THRESH1_MEAS_SEL[3:0](0x70), and THRESH2_MEAS_SEL[7:4](0x70) should be set to zero.

COLLECT_RAW_DATA	Decode
0	Computed data for each measurement is saved in the FIFO.
1	Raw data for all ambient conversions and LED conversions in each measurement is saved in the FIFO.

MEAS1_CONFIG_SEL

MEAS1_CONFIG_SEL selects whether all enabled PPG measurements use a unique configuration or use the configuration settings defined in the MEAS1 setup registers (0x20 to 0x26). The unique configuration for each measurement is defined in each MEASx setup register. Setting MEAS1_CONFIG_SEL = 1 allows for reduced setup configuration writes. When MEAS1_CONFIG_SEL = 1, the configuration settings used by all enabled measurements are as follows:

MEAS1_SINC3_SEL
 MEAS1_FILT2_SEL
 MEAS1_FILT_SEL
 MEAS1_TINT
 MEAS1_AVER
 MEAS1_PPG1_ADC_RGE
 MEAS1_PPG2_ADC_RGE
 MEAS1_PD_SETLNG
 MEAS1_LED_SETLNG
 MEAS1_LED_RGE
 MEAS1_PD1_SEL
 MEAS1_PD2_SEL
 MEAS1_PD3_SEL
 MEAS1_PD4_SEL

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MEAS1_CONFIG_SEL	Decode
0	Specific configuration defined in each measurement setup registers is used.
1	MEAS1 configuration is used for all enabled measurements.

PPG Configuration 4 (0x23)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	PROX_DAT_A_EN	PROX_AUTO	-	-	-
Reset	-	-	-	0	0	-	-	-
Access Type	-	-	-	Write, Read	Write, Read	-	-	-

PROX_DATA_EN

PROX_DATA_EN enables MEAS6 data to be saved in the FIFO when PROX_AUTO = 1. If PROX_AUTO is set to 0, PROX_DATA_EN is ignored.

PROX_DATA_EN	Decode
0	MEAS6 data is not saved in FIFO when PROX_AUTO = 1
1	MEAS6 data is saved in FIFO when PROX_AUTO = 1

PROX_AUTO

PROX_AUTO enables automatic proximity detect mode. For details, see the Automatic Proximity-Detect Mode section.

PROX_AUTO	Decode
0	Normal mode
1	Automatic proximity detect mode.

Photodiode Bias (0x24)

BIT	7	6	5	4	3	2	1	0
Field	PD4_BIAS[1:0]	PD3_BIAS[1:0]	PD2_BIAS[1:0]	PD1_BIAS[1:0]				
Reset	0x1	0x1	0x1	0x1				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

PD4_BIAS

PDm_BIAS ($m = 1$ to 4) selects the photodiode-bias current for the photodiode connected to the corresponding PDm_IN pin. PDm_BIAS should be adjusted according to the photodiode capacitance on the PDm_IN pin. See the Photodiode Biasing section for more information.

PDm_BIAS ($m = 1$ to 4)	Range of Photodiode Capacitance (pF)
0x0	Not recommended
0x1	0 to 125
0x2	125 to 250
0x3	250 to 500

PD3_BIAS

See PD4_BIAS for details.

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PD2_BIAS

See PD4_BIAS for details.

PD1_BIAS

See PD4_BIAS for details.

FR Clock Divider MSB (0x28)

BIT	7	6	5	4	3	2	1	0
Field	—	FR_CLK_DIV[14:8]						
Reset	—	0x01						
Access Type	—	Write, Read						

FR_CLK_DIV

FR_CLK_DIV[14:8] has the upper 7 bits of the 15-bit FR_CLK_DIV[14:0] clock divider, which defines the PPG frame rate.

For more information on PPG frame rate see the Timing Subsystem section.

FR_CLK_DIV[14:0]	Frame Rate with REF_CLK_SEL = 0 (fps)	Frame Rate with RED_CLK_SEL = 1 (fps)
0x7FFF	Reserved	Reserved
0x7FFE	0.976622	1.000061
0x7FFD	0.976652	1.000092
....		
0x0100	125	128 (default)
....		
0x0012	1777.78	1820.44
0x0011	1882.35	1927.53
0x0010	2000.00	2048.00
0x000F - 0x0000	2000.00	2048.00

FR Clock Divider LSB (0x29)

BIT	7	6	5	4	3	2	1	0
Field	FR_CLK_DIV[7:0]							
Reset	0x00							
Access Type	Write, Read							

FR_CLK_DIV

FR_CLK_DIV[7:0] has the lower byte of the 15-bit FR_CLK_DIV clock divider that defines the PPG frame rate.

See FR_CLK_DIV[14:8] for more details.

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MEAS1 Selects (0x30)

BIT	7	6	5	4	3	2	1	0
Field	-	MEAS1_AMB	MEAS1_DRVB[2:0]				MEAS1_DRVA[2:0]	
Reset	-	0	0x0				0x0	
Access Type	-	Write, Read	Write, Read				Write, Read	

MEAS1_AMB

MEASx_AMB (x = 1 to 6) enables or disables direct ambient measurement. When MEASx_AMB is set to 1, MEASx_DRVA and MEASx_DRVB are ignored.

The direct ambient measurement should always be the last enabled measurement in the frame.

MEASx_AMB (x = 1 to 6)	Decode
0	Normal mode
1	Direct ambient conversion

MEAS1_DRVB

MEASx_DRVB (x = 1 to 6) selects the LEDn_DRV pin (n = 1 to 6) driven by LED driver B.

MEASx_DRVB (x = 1 to 6)	Pin driven by LED driver B
0x0	LED1_DRV
0x1	LED2_DRV
0x2	LED3_DRV
0x3	LED4_DRV
0x4	LED5_DRV
0x5	LED6_DRV
0x6	Do not use
0x7	Do not use

MEAS1_DRVA

MEASx_DRVA (x = 1 to 6) selects the LEDn_DRV pin (n = 1 to 6) driven by LED driver A.

MEASx_DRVA (x = 1 to 6)	Pin driven by LED driver A
0x0	LED1_DRV
0x1	LED2_DRV
0x2	LED3_DRV
0x3	LED4_DRV
0x4	LED5_DRV
0x5	LED6_DRV
0x6	Do not use
0x7	Do not use

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MEAS1 Configuration 1 (0x31)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_SI NC3_SEL	MEAS1_FIL T2_SEL	MEAS1_FIL T_SEL	MEAS1_TINT[1:0]			MEAS1_AVER[2:0]	
Reset	0	1	0	0x3			0x0	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read			Write, Read	

MEAS1_SINC3_SEL

MEASx_SINC3_SEL (x = 1 to 6) enables the SINC3 decimation filter for the PPG ADC. If MEASx_SINC3_SEL is set to 1, MEASx_TINT must be set to 3 and MEASx_FILT2_SEL must be set to 0.

MEASx_SINC3_SEL (x = 1 to 6)	Decode
0	SINC3 filter is not used. Either a second-order or third-order decimation filter is used depending on the MEASx_FILT2_SEL, MEASx_FILT_SEL, and MEASx_TINT settings.
1	SINC3 decimation filter is used (if MEASx_TINT = 3 (117.1μs))

MEAS1_FILT2_SEL

MEASx_FILT2_SEL enables either a second-order decimation filter or a third order decimation filter. When MEASx_FILT2_SEL = 1 (second-order decimation filter), MEASx_SINC3_SEL must be set to 0 and MEASx_TINT must be 0x3.

MEASx_FILT2_SEL	Decode
0	3rd order decimation filter is used.
1	2nd order decimation filter is used if MEASx_SINC3_SEL = 0 and MEASx_TINT = 3

MEAS1_FILT_SEL

MEASx_FILT_SEL (x = 1 to 6) selects the digital ambient light rejection method to be used. See the Ambient Rejection section for details.

MEASx_FILT_SEL (x = 1 to 6)	Decode
0	Central difference method (CDM) is enabled.
1	Forward difference method (FDM) is enabled.

MEAS1_TINT

MEASx_TINT (x = 1 to 6) selects the integration time of PPG ADCs.

MEASx_TINT (x = 1 to 6)	Integration Time with 3rd-Order Decimation Filter (μs)	Integration Time with 2nd-Order Decimation Filter (μs)
0x0	14.6	Not applicable
0x1	29.2	Not applicable
0x2	58.6	Not applicable
0x3	117.0	118.2

MEAS1_AVER

MEASx_AVER (x = 1 to 6) selects the number of exposures to be averaged in order to get one measurement sample in the FIFO. When setting MEASx_AVER to any value other than 0, MEASx_FILT_SEL must be 0. With MEASx_AVER, each sample in FIFO is a computed average of $(2 \times 2^{\text{MEASx_AVER}} + 1)$ ADC conversions of interleaved ambient and

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exposure measurements. When MEASx_FILT_SEL = 1, MEASx_AVER is ignored.

MEASx_AVER (x = 1 to 6)	Number of LED Pulses
0x0	1
0x1	2
0x2	4
0x3	8
0x4	16
0x5	32
0x6	64
0x7	128

MEAS1 Configuration 2 (0x32)

BIT	7	6	5	4	3	2	1	0
Field	–	–	MEAS1_PPG2_ADC_RGE [1:0]	–	–	–	MEAS1_PPG1_ADC_RGE [1:0]	–
Reset	–	–	0x2	–	–	–	0x2	–
Access Type	–	–	Write, Read	–	–	–	Write, Read	–

MEAS1_PPG2_ADC_RGE

MEASx_PPG2_ADC_RGE (x = 1 to 6) selects the positive full-scale range of the PPG ADC on channel 2 for measurement x.

MEASx_PPG2_ADC_RGE (x = 1 to 6)	Full-Scale Range for ADC2 (µA)
0x0	4.0
0x1	8.0
0x2	16.0
0x3	32.0

MEAS1_PPG1_ADC_RGE

MEASx_PPG1_ADC_RGE (x = 1 to 6) selects the positive full-scale range of the PPG ADC on channel 1 for measurement x.

MEASx_PPG1_ADC_RGE (x = 1 to 6)	Full-Scale Range for ADC1 (µA)
0x0	4.0
0x1	8.0
0x2	16.0
0x3	32.0

MEAS1 Configuration 3 (0x33)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_PPG2_DACOFF[3:0]						MEAS1_PPG1_DACOFF[3:0]	
Reset	0x0						0x0	
Access Type	Write, Read						Write, Read	

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MEASx_PPG2_DACOFF (x = 1 to 6) selects the offset DAC current added to the ADC on PPG channel 2 during the exposure interval. This allows for a larger convertible exposure range for ADC2 by sourcing some of the photodiode DC exposure current from the offset DAC.

MEASx_PPG2_DACOFF (x = 1 to 6)	Injected Offset Current to ADC2 (μ A)
0x0	0
0x1	2
0x2	4
0x3	6
0x4	8
0x5	10
0x6	12
0x7	14
0x8	16
0x9	18
0xA	20
0xB	22
0xC	24
0xD	26
0xE	28
0xF	30

MEAS1_PPG1_DACOFF

MEASx_PPG1_DACOFF (x = 1 to 6) selects the offset DAC current added to ADC on PPG channel 1 during the exposure interval. This allow for a larger convertible exposure range for ADC1 by sourcing some of the photodiode DC exposure current from the offset DAC.

MEASx_PPG1_DACOFF (x = 1 to 6)	Injected Offset Current to ADC1 (μ A)
0x0	0
0x1	2
0x2	4
0x3	6
0x4	8
0x5	10
0x6	12
0x7	14
0x8	16
0x9	18
0xA	20
0xB	22
0xC	24
0xD	26
0xE	28
0xF	30

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MEAS1 Configuration 4 (0x34)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_PD_SETLNG[1:0]				MEAS1_LED_SETLNG[1:0]		MEAS1_LED_RGE[1:0]	
Reset	0x1				0x1		0x3	
Access Type	Write, Read				Write, Read		Write, Read	

MEAS1_PD_SETLNG

MEASx_PD_SETLNG ($x = 1$ to 6) selects the time between dark and exposure samples for measurement x. This accommodates photodiodes with longer settling time.

PD settling time should always be more than LED settling time selected in MEASx_LED_SETLNG. Note that for the same setting of both MEASx_PD_SETLNG and MEASx_LED_SETLNG, the photodiode settling time is $0.1\mu s$ higher than the LED settling time, and thus, satisfies the requirement of the higher PD settling time.

MEASx_PD_SETLNG ($x = 1$ to 6)	Photodiode Settling Time (μs)
0x0	7.8
0x1	11.8
0x2	15.8
0x3	23.8

MEAS1_LED_SETLNG

MEASx_LED_SETLNG ($x = 1$ to 6) selects the delay from the rising edge of LED to the start of the exposure ADC integration. This allows for the LED current to settle before the start of ADC integration. LED settling time for a measurement must always be less than the photodiode settling time for the same measurement.

MEASx_LED_SETLNG ($x = 1$ to 6)	LED Settling Time (μs)
0x0	7.7
0x1	11.7
0x2	15.7
0x3	23.7

MEAS1_LED_RGE

MEASx_LED_RGE ($x = 1$ to 6) selects the drive current range for both LED current drivers, DRVA and DRVB, for measurement x.

MEASx_LED_RGE ($x = 1$ to 6)	LED Full-Scale Range (mA)
0x0	32
0x1	64
0x2	96
0x3	128

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MEAS1 Configuration 5 (0x35)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_PD4_SEL[1:0]		MEAS1_PD3_SEL[1:0]		MEAS1_PD2_SEL[1:0]		MEAS1_PD1_SEL[1:0]	
Reset	0x0		0x0		0x3		0x2	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

MEAS1_PD4_SEL

MEASx_PD4_SEL (x = 1 to 6) connects the PD4 input to the selected optical channel.

MEASx_PD4_SEL (x = 1 to 6)	Decode
0x0, 0x1	PD4 not selected
0x2	PD4 is connected to PPG channel 1
0x3	PD4 is connected to PPG channel 2

MEAS1_PD3_SEL

MEASx_PD3_SEL (x = 1 to 6) selects the PD3 input to each of the optical channels.

MEASx_PD3_SEL (x = 1 to 6)	Decode
0x0, 0x1	PD3 not selected
0x2	PD3 is connected to PPG channel 1
0x3	PD3 is connected to PPG channel 2

MEAS1_PD2_SEL

MEASx_PD2_SEL (x = 1 to 6) selects the PD2 input to each of the optical channels.

MEASx_PD2_SEL (x = 1 to 6)	Decode
0x0, 0x1	PD2 not selected
0x2	PD2 is connected to PPG channel 1
0x3	PD2 is connected to PPG channel 2

MEAS1_PD1_SEL

MEASx_PD1_SEL (x = 1 to 6) selects the PD1 input to each of the optical channels.

MEASx_PD1_SEL (x = 1 to 6)	Decode
0x0, 0x1	PD1 not selected
0x2	PD1 is connected to PPG channel 1
0x3	PD1 is connected to PPG channel 2

MEAS1 LEDA Current (0x36)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_DRVA_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

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MEAS_x_DRVA_PA ($x = 1$ to 6) selects the LED drive current on LED driver A for measurement x . If MEAS_n_DRVA_PA is set to 0x00, LED Driver A is disabled for measurement x . The full-scale range selected by MEAS_x_LED_RGE[4:5](0x22) determines the LED current for each LSB of MEAS_x_DRVA_PA setting. For example, when MEAS_x_LED_RGE = 0, one LSB of MEAS_x_DRVA_PA is 0.125mA of the LED driver current on DRVA, but when MEAS_x_LED_RGE = 3, each LSB of MEAS_x_DRVA_PA setting is 0.5mA of the LED driver current on DRVA.

MEAS _x _LED_RGE ($x = 1$ to 6)	0	1	2	3
MEAS _x _DRVA_PA ($x = 1$ to 6)	LED Current (mA)	LED Current (mA)	LED Current (mA)	LED Current (mA)
0x00	0.000	0.000	0.000	0.000
0x01	0.125	0.250	0.375	0.500
0x02	0.250	0.500	0.750	1.000
0x03	0.375	0.750	1.125	1.500
.....				
0xFC	31.500	63.000	94.500	126.000
0xFD	31.625	63.250	94.875	126.500
0xFE	31.750	63.500	95.250	127.000
0xFF	31.875	63.750	95.625	127.500
LSB	0.125	0.250	0.375	0.500

MEAS1 LEDB Current (0x37)

BIT	7	6	5	4	3	2	1	0
Field	MEAS1_DRVB_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

MEAS1_DRVB_PA

MEAS_x_DRV_B_PA ($x = 1$ to 6) selects the LED drive current on LED driver B for measurement x . If MEAS_x_DRV_B_PA is set to 0x00, LED Driver B is disabled for measurement x . The full-scale range selected by MEAS_x_LED_RGE[4:5](0x22) determines the LED current for each LSB of the MEAS_x_DRV_B_PA setting. For example, when MEAS_x_LED_RGE = 0, one LSB of MEAS_x_DRV_B_PA is 0.125mA of the LED driver current on DRVB, but when MEAS_x_LED_RGE = 3, each LSB of MEAS_x_DRV_B_PA setting is 0.5mA of the LED driver current on DRVB.

MEAS _x _LED_RGE ($x = 1$ to 6)	0	1	2	3
MEAS _x _DRV _B _PA ($x = 1$ to 6)	LED Current (mA)	LED Current (mA)	LED Current (mA)	LED Current (mA)
0x00	0.000	0.000	0.000	0.000
0x01	0.125	0.250	0.375	0.500
0x02	0.250	0.500	0.750	1.000
0x03	0.375	0.750	1.125	1.500
.....				
0xFC	31.500	63.000	94.500	126.000
0xFD	31.625	63.250	94.875	126.500
0xFE	31.750	63.500	95.250	127.000

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MEASx_LED_RGE (x = 1 to 6)	0	1	2	3
0xFF	31.875	63.750	95.625	127.500
Each LSB	0.125	0.250	0.375	0.500

MEAS2 Selects (0x38)

BIT	7	6	5	4	3	2	1	0
Field	-	MEAS2_AMB	MEAS2_DRVB[2:0]					MEAS2_DRVA[2:0]
Reset	-	0	0x0					0x0
Access Type	-	Write, Read	Write, Read					Write, Read

MEAS2_AMB

See MEAS1_AMB[6](0x30) for details.

MEAS2_DRVB

See MEAS1_DRVB[3:5](0x30) for details.

MEAS2_DRVA

See MEAS1_DRVA[2:0](0x30) for details.

MEAS2 Configuration 1 (0x39)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_SI NC3_SEL	MEAS2_FILT2_SEL	MEAS2_FILT2_SEL	MEAS2_TINT[1:0]			MEAS2_AVER[2:0]	
Reset	0	1	0	0x3			0x0	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read			Write, Read	

MEAS2_SINC3_SEL

See MEAS1_SINC3_SEL[7](0x31) for details

MEAS2_FILT2_SEL

See MEAS1_FILT2_SEL[6](0x31) for details.

MEAS2_FILT_SEL

See MEAS1_FILT_SEL[5](0x31) for details.

MEAS2_TINT

See MEAS1_TINT[4:3](0x31) for details.

MEAS2_AVER

See MEAS1_AVER[2:0](0x31) for details.

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MEAS2 Configuration 2 (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	MEAS2_PPG2_ADC_RGE [1:0]	–	–	–	MEAS2_PPG1_ADC_RGE [1:0]	–
Reset	–	–	0x2	–	–	–	0x2	–
Access Type	–	–	Write, Read	–	–	–	Write, Read	–

MEAS2_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[5:4](0x32) for details.

MEAS2_PPG1_ADC_RGE

See MEAS1_PPG1_ADC_RGE[1:0](0x32) for details.

MEAS2 Configuration 3 (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS2_PPG2_DACOFF[3:0]	–	–	MEAS2_PPG1_DACOFF[3:0]	–	–	–
Reset	–	0x0	–	–	–	0x0	–	–
Access Type	–	Write, Read	–	–	–	–	Write, Read	–

MEAS2_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[7:4](0x33) for details.

MEAS2_PPG1_DACOFF

See MEAS1_PPG1_DACOFF[3:0](0x33) for details.

MEAS2 Configuration 4 (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_PD_SETLNG[1:0]	–	–	–	MEAS2_LED_SETLNG[1:0]	–	MEAS2_LED_RGE[1:0]	–
Reset	0x1	–	–	–	0x1	–	0x3	–
Access Type	Write, Read	–	–	–	Write, Read	–	Write, Read	–

MEAS2_PD_SETLNG

See MEAS1_PD_SETLNG[7:6](0x34) for details.

MEAS2_LED_SETLNG

See MEAS1_LED_SETLNG[3:2](0x34) for details.

MEAS2_LED_RGE

See MEAS1_LED_RGE[1:0](0x34) for details.

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MEAS2 Configuration 5 (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS2_PD4_SEL[1:0]		MEAS2_PD3_SEL[1:0]		MEAS2_PD2_SEL[1:0]		MEAS2_PD1_SEL[1:0]	
Reset	0x0		0x0		0x3		0x2	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

MEAS2_PD4_SEL

See MEAS1_PD4_SEL[7:6](0x35) for details.

MEAS2_PD3_SEL

See MEAS1_PD3_SEL[5:4](0x35) for details.

MEAS2_PD2_SEL

See MEAS1_PD2_SEL[3:2](0x35) for details.

MEAS2_PD1_SEL

See MEAS1_PD1_SEL[1:0](0x35) for details.

MEAS2 LEDA Current (0x3E)

BIT	7	6	5	4	3	2	1	0
Field				MEAS2_DRVA_PA[7:0]				
Reset				0x00				
Access Type				Write, Read				

MEAS2_DRVA_PA

See MEAS1_DRVA_PA[7:0](0x36) for details.

MEAS2 LEDB Current (0x3F)

BIT	7	6	5	4	3	2	1	0
Field				MEAS2_DRVB_PA[7:0]				
Reset				0x00				
Access Type				Write, Read				

MEAS2_DRVB_PA

See MEAS1_DRVB_PA[7:0](0x37) for details.

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MEAS3 Selects (0x40)

BIT	7	6	5	4	3	2	1	0
Field	-	MEAS3_AMB	MEAS3_DRVB[2:0]				MEAS3_DRVA[2:0]	
Reset	-	0	0x0				0x0	
Access Type	-	Write, Read	Write, Read				Write, Read	

MEAS3_AMB

See MEAS1_AMB[6](0x30) for details.

MEAS3_DRVB

See MEAS1_DRVB[3:5](0x30) for details.

MEAS3_DRVA

See MEAS1_DRVA[2:0](0x30) for details.

MEAS3 Configuration 1 (0x41)

BIT	7	6	5	4	3	2	1	0	
Field	MEAS3_SI NC3_SEL	MEAS3_FIL T2_SEL	MEAS3_FIL T_SEL	MEAS3_TINT[1:0]		MEAS3_AVER[2:0]			
Reset	0	1	0	0x3			0x0		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read			Write, Read		

MEAS3_SINC3_SEL

See MEAS1_SINC3_SEL[7](0x30) for details

MEAS3_FILT2_SEL

See MEAS1_FILT2_SEL for details.

MEAS3_FILT_SEL

See MEAS1_FILT_SEL[5](0x31) for details.

MEAS3_TINT

See MEAS1_TINT[4:3](0x31) for details.

MEAS3_AVER

See MEAS1_AVER[2:0](0x31) for details.

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MEAS3 Configuration 2 (0x42)

BIT	7	6	5	4	3	2	1	0
Field	–	–	MEAS3_PPG2_ADC_RGE [1:0]	–	–	–	MEAS3_PPG1_ADC_RGE [1:0]	–
Reset	–	–	0x2	–	–	–	0x2	–
Access Type	–	–	Write, Read	–	–	–	Write, Read	–

MEAS3_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[5:4](0x32) for details.

MEAS3_PPG1_ADC_RGE

See MEAS1_PPG1_ADC_RGE[1:0](0x32) for details.

MEAS3 Configuration 3 (0x43)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS3_PPG2_DACOFF[3:0]	–	–	MEAS3_PPG1_DACOFF[3:0]	–	–	–
Reset	–	0x0	–	–	–	0x0	–	–
Access Type	–	Write, Read	–	–	–	–	Write, Read	–

MEAS3_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[7:4](0x33) for details.

MEAS3_PPG1_DACOFF

See MEAS1_PPG1_DACOFF[3:0](0x33) for details.

MEAS3 Configuration 4 (0x44)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_PD_SETLNG[1:0]	–	–	–	MEAS3_LED_SETLNG[1:0]	–	MEAS3_LED_RGE[1:0]	–
Reset	0x1	–	–	–	0x1	–	0x3	–
Access Type	Write, Read	–	–	–	Write, Read	–	Write, Read	–

MEAS3_PD_SETLNG

See MEAS1_PD_SETLNG[7:6](0x34) for details.

MEAS3_LED_SETLNG

See MEAS1_LED_SETLNG[3:2](0x34) for details.

MEAS3_LED_RGE

See MEAS1_LED_RGE[1:0](0x34) for details.

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MEAS3 Configuration 5 (0x45)

BIT	7	6	5	4	3	2	1	0
Field	MEAS3_PD4_SEL[1:0]		MEAS3_PD3_SEL[1:0]		MEAS3_PD2_SEL[1:0]		MEAS3_PD1_SEL[1:0]	
Reset	0x0		0x0		0x3		0x2	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

MEAS3_PD4_SEL

See MEAS1_PD4_SEL[7:6](0x35) for details.

MEAS3_PD3_SEL

See MEAS1_PD3_SEL[5:4](0x35) for details.

MEAS3_PD2_SEL

See MEAS1_PD2_SEL[3:2](0x35) for details.

MEAS3_PD1_SEL

See MEAS1_PD1_SEL[1:0](0x35) for details.

MEAS3 LEDA Current (0x46)

BIT	7	6	5	4	3	2	1	0
Field				MEAS3_DRVA_PA[7:0]				
Reset				0x00				
Access Type				Write, Read				

MEAS3_DRVA_PA

See MEAS1_DRVA_PA[7:0](0x36) for details.

MEAS3 LEDB Current (0x47)

BIT	7	6	5	4	3	2	1	0
Field				MEAS3_DRVB_PA[7:0]				
Reset				0x00				
Access Type				Write, Read				

MEAS3_DRVB_PA

See MEAS1_DRVB_PA[7:0](0x37) for details.

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MEAS4 Selects (0x48)

BIT	7	6	5	4	3	2	1	0
Field	-	MEAS4_AMB	MEAS4_DRVB[2:0]				MEAS4_DRVA[2:0]	
Reset	-	0	0x0				0x0	
Access Type	-	Write, Read	Write, Read				Write, Read	

MEAS4_AMB

See MEAS1_AMB[6](0x30) for details.

MEAS4_DRVB

See MEAS1_DRVB[3:5](0x30) for details.

MEAS4_DRVA

See MEAS1_DRVA[2:0](0x30) for details.

MEAS4 Configuration 1 (0x49)

BIT	7	6	5	4	3	2	1	0	
Field	MEAS4_SI NC3_SEL	MEAS4_FIL T2_SEL	MEAS4_FIL T_SEL	MEAS4_TINT[1:0]		MEAS4_AVER[2:0]			
Reset	0	1	0	0x3			0x0		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read			Write, Read		

MEAS4_SINC3_SEL

See MEAS1_SINC3_SEL[7](0x31) for details.

MEAS4_FILT2_SEL

See MEAS1_FILT2_SEL[6](0x31) for details.

MEAS4_FILT_SEL

See MEAS1_FILT_SEL[5](0x31) for details.

MEAS4_TINT

See MEAS1_TINT[4:3](0x31) for details.

MEAS4_AVER

See MEAS1_AVER[2:0](0x31) for details.

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MEAS4 Configuration 2 (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	MEAS4_PPG2_ADC_RGE [1:0]	–	–	–	MEAS4_PPG1_ADC_RGE [1:0]	–
Reset	–	–	0x2	–	–	–	0x2	–
Access Type	–	–	Write, Read	–	–	–	Write, Read	–

MEAS4_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[5:4](0x32) for details.

MEAS4_PPG1_ADC_RGE

See MEAS1_PPG1_ADC_RGE[1:0](0x32) for details.

MEAS4 Configuration 3 (0x4B)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS4_PPG2_DACOFF[3:0]	–	–	MEAS4_PPG1_DACOFF[3:0]	–	–	–
Reset	–	0x0	–	–	–	0x0	–	–
Access Type	–	Write, Read	–	–	–	–	Write, Read	–

MEAS4_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[7:4](0x33) for details.

MEAS4_PPG1_DACOFF

See MEAS1_PPG1_DACOFF[3:0](0x33) for details.

MEAS4 Configuration 4 (0x4C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_PD_SETLNG[1:0]	–	–	–	MEAS4_LED_SETLNG[1:0]	–	MEAS4_LED_RGE[1:0]	–
Reset	0x1	–	–	–	0x1	–	0x3	–
Access Type	Write, Read	–	–	–	Write, Read	–	Write, Read	–

MEAS4_PD_SETLNG

See MEAS1_PD_SETLNG[7:6](0x34) for details.

MEAS4_LED_SETLNG

See MEAS1_LED_SETLNG[3:2](0x34) for details.

MEAS4_LED_RGE

See MEAS1_LED_RGE[1:0](0x34) for details.

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MEAS4 Configuration 5 (0x4D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS4_PD4_SEL[1:0]		MEAS4_PD3_SEL[1:0]		MEAS4_PD2_SEL[1:0]		MEAS4_PD1_SEL[1:0]	
Reset	0x0		0x0		0x3		0x2	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

MEAS4_PD4_SEL

See MEAS1_PD4_SEL[7:6](0x35) for details.

MEAS4_PD3_SEL

See MEAS1_PD3_SEL[5:4](0x35) for details.

MEAS4_PD2_SEL

See MEAS1_PD2_SEL[3:2](0x35) for details.

MEAS4_PD1_SEL

See MEAS1_PD1_SEL[1:0](0x35) for details.

MEAS4 LEDA Current (0x4E)

BIT	7	6	5	4	3	2	1	0
Field				MEAS4_DRVA_PA[7:0]				
Reset				0x00				
Access Type				Write, Read				

MEAS4_DRVA_PA

See MEAS1_DRVA_PA[7:0](0x36) for details.

MEAS4 LEDB Current (0x4F)

BIT	7	6	5	4	3	2	1	0
Field				MEAS4_DRVB_PA[7:0]				
Reset				0x00				
Access Type				Write, Read				

MEAS4_DRVB_PA

See MEAS1_DRVB_PA[7:0](0x37) for details.

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MEAS5 Selects (0x50)

BIT	7	6	5	4	3	2	1	0
Field	-	MEAS5_AMB	MEAS5_DRVB[2:0]				MEAS5_DRVA[2:0]	
Reset	-	0	0x0				0x0	
Access Type	-	Write, Read	Write, Read				Write, Read	

MEAS5_AMB

See MEAS1_AMB[6](0x30) for details.

MEAS5_DRVB

See MEAS1_DRVB[3:5](0x30) for details.

MEAS5_DRVA

See MEAS1_DRVA[2:0](0x30) for details.

MEAS5 Configuration 1 (0x51)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_SI NC3_SEL	MEAS5_FILT2_SEL	MEAS5_FILT_T_SEL	MEAS5_TINT[1:0]		MEAS5_AVER[2:0]		
Reset	0	1	0	0x3			0x0	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read			Write, Read	

MEAS5_SINC3_SEL

See MEAS1_SINC3_SEL[7](0x31) for details.

MEAS5_FILT2_SEL

See MEAS1_FILT2_SEL[6](0x31) for details.

MEAS5_FILT_SEL

See MEAS1_FILT_SEL[5](0x31) for details.

MEAS5_TINT

See MEAS1_TINT[4:3](0x31) for details.

MEAS5_AVER

See MEAS1_AVER[2:0](0x31) for details.

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MEAS5 Configuration 2 (0x52)

BIT	7	6	5	4	3	2	1	0
Field	–	–	MEAS5_PPG2_ADC_RGE [1:0]	–	–	–	MEAS5_PPG1_ADC_RGE [1:0]	–
Reset	–	–	0x2	–	–	–	0x2	–
Access Type	–	–	Write, Read	–	–	–	Write, Read	–

MEAS5_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[5:4](0x32) for details.

MEAS5_PPG1_ADC_RGE

See MEAS1_PPG1_ADC_RGE[1:0](0x32) for details.

MEAS5 Configuration 3 (0x53)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS5_PPG2_DACOFF[3:0]	–	–	MEAS5_PPG1_DACOFF[3:0]	–	–	–
Reset	–	0x0	–	–	–	0x0	–	–
Access Type	–	Write, Read	–	–	–	–	Write, Read	–

MEAS5_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[7:4](0x33) for details.

MEAS5_PPG1_DACOFF

See MEAS1_PPG1_DACOFF[3:0](0x33) for details.

MEAS5 Configuration 4 (0x54)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_PD_SETLNG[1:0]	–	–	–	MEAS5_LED_SETLNG[1:0]	–	MEAS5_LED_RGE[1:0]	–
Reset	0b01	–	–	–	0x1	–	0x3	–
Access Type	Write, Read	–	–	–	Write, Read	–	Write, Read	–

MEAS5_PD_SETLNG

See MEAS1_PD_SETLNG[7:6](0x34) for details.

MEAS5_LED_SETLNG

See MEAS1_LED_SETLNG[3:2](0x34) for details.

MEAS5_LED_RGE

See MEAS1_LED_RGE[1:0](0x34) for details.

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MEAS5 Configuration 5 (0x55)

BIT	7	6	5	4	3	2	1	0
Field	MEAS5_PD4_SEL[1:0]		MEAS5_PD3_SEL[1:0]		MEAS5_PD2_SEL[1:0]		MEAS5_PD1_SEL[1:0]	
Reset	0x0		0x0		0x3		0x2	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

MEAS5_PD4_SEL

See MEAS1_PD4_SEL[7:6](0x35) for details.

MEAS5_PD3_SEL

See MEAS1_PD3_SEL[5:4](0x35) for details.

MEAS5_PD2_SEL

See MEAS1_PD2_SEL[3:2](0x35) for details.

MEAS5_PD1_SEL

See MEAS1_PD1_SEL[1:0](0x35) for details.

MEAS5 LEDA Current (0x56)

BIT	7	6	5	4	3	2	1	0
Field				MEAS5_DRVA_PA[7:0]				
Reset				0x00				
Access Type				Write, Read				

MEAS5_DRVA_PA

See MEAS1_DRVA_PA[7:0](0x36) for details.

MEAS5 LEDB Current (0x57)

BIT	7	6	5	4	3	2	1	0
Field				MEAS5_DRVB_PA[7:0]				
Reset				0x00				
Access Type				Write, Read				

MEAS5_DRVB_PA

See MEAS1_DRVB_PA[7:0](0x37) for details.

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MEAS6 Selects (0x58)

BIT	7	6	5	4	3	2	1	0
Field	-	MEAS6_AMB	MEAS6_DRVB[2:0]				MEAS6_DRVA[2:0]	
Reset	-	0	0x0				0x0	
Access Type	-	Write, Read	Write, Read				Write, Read	

MEAS6_AMB

See MEAS1_AMB[6](0x30) for details.

MEAS6_DRVB

See MEAS1_DRVB[3:5](0x30) for details.

MEAS6_DRVA

See MEAS1_DRVA[2:0](0x30) for details.

MEAS6 Configuration 1 (0x59)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_SI NC3_SEL	MEAS6_FIL T2_SEL	MEAS6_FIL T_SEL	MEAS6_TINT[1:0]		MEAS6_AVER[2:0]		
Reset	0	1	0	0x3			0x0	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read			Write, Read	

MEAS6_SINC3_SEL

See MEAS1_SINC3_SEL[7](0x31) for details.

MEAS6_FILT2_SEL

See MEAS1_FILT2_SEL[6](0x31) for details.

MEAS6_FILT_SEL

See MEAS1_FILT_SEL[5](0x31) for details.

MEAS6_TINT

See MEAS1_TINT[4:3](0x31) for details.

MEAS6_AVER

See MEAS1_AVER[2:0](0x31) for details.

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MEAS6 Configuration 2 (0x5A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	MEAS6_PPG2_ADC_RGE [1:0]	–	–	–	MEAS6_PPG1_ADC_RGE [1:0]	–
Reset	–	–	0x2	–	–	–	0x2	–
Access Type	–	–	Write, Read	–	–	–	Write, Read	–

MEAS6_PPG2_ADC_RGE

See MEAS1_PPG2_ADC_RGE[5:4](0x32) for details.

MEAS6_PPG1_ADC_RGE

See MEAS1_PPG1_ADC_RGE[1:0](0x32) for details.

MEAS6 Configuration 3 (0x5B)

BIT	7	6	5	4	3	2	1	0
Field	–	MEAS6_PPG2_DACOFF[3:0]	–	–	MEAS6_PPG1_DACOFF[3:0]	–	–	–
Reset	–	0x0	–	–	–	0x0	–	–
Access Type	–	Write, Read	–	–	–	–	Write, Read	–

MEAS6_PPG2_DACOFF

See MEAS1_PPG2_DACOFF[7:4](0x33) for details.

MEAS6_PPG1_DACOFF

See MEAS1_PPG1_DACOFF[3:0](0x33) for details.

MEAS6 Configuration 4 (0x5C)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_PD_SETLNG[1:0]	–	–	–	MEAS6_LED_SETLNG[1:0]	–	MEAS6_LED_RGE[1:0]	–
Reset	0b01	–	–	–	0x1	–	0x3	–
Access Type	Write, Read	–	–	–	Write, Read	–	Write, Read	–

MEAS6_PD_SETLNG

See MEAS1_PD_SETLNG[7:6](0x34) for details.

MEAS6_LED_SETLNG

See MEAS1_LED_SETLNG[3:2](0x34) for details.

MEAS6_LED_RGE

See MEAS1_LED_RGE[1:0](0x34) for details.

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MEAS6 Configuration 5 (0x5D)

BIT	7	6	5	4	3	2	1	0
Field	MEAS6_PD4_SEL[1:0]		MEAS6_PD3_SEL[1:0]		MEAS6_PD2_SEL[1:0]		MEAS6_PD1_SEL[1:0]	
Reset	0x0		0x0		0x3		0x2	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

MEAS6_PD4_SEL

See MEAS1_PD4_SEL[7:6](0x35) for details.

MEAS6_PD3_SEL

See MEAS1_PD3_SEL[5:4](0x35) for details.

MEAS6_PD2_SEL

See MEAS1_PD2_SEL[3:2](0x35) for details.

MEAS6_PD1_SEL

See MEAS1_PD1_SEL[1:0](0x35) for details.

MEAS6 LEDA Current (0x5E)

BIT	7	6	5	4	3	2	1	0
Field				MEAS6_DRVA_PA[7:0]				
Reset				0x00				
Access Type				Write, Read				

MEAS6_DRVA_PA

See MEAS1_DRVA_PA[7:0](0x36) for details.

MEAS6 LEDB Current (0x5F)

BIT	7	6	5	4	3	2	1	0
Field				MEAS6_DRVB_PA[7:0]				
Reset				0x00				
Access Type				Write, Read				

MEAS6_DRVB_PA

See MEAS1_DRVB_PA[7:0](0x37) for details.

THRESHOLD MEAS SEL (0x70)

BIT	7	6	5	4	3	2	1	0
Field	-		THRESH2_MEAS_SEL[2:0]		-		THRESH1_MEAS_SEL[2:0]	
Reset	-		0x0		-		0x0	
Access Type	-		Write, Read		-		Write, Read	

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Vital-Sign AFE**THRESH2_MEAS_SEL**

THRESH2_MEAS_SEL enables the threshold detect function and selects the PPG measurement for the second instance of the threshold function. For details see the Threshold Detect Function section.

If the threshold detect function is enabled, COLLECT_RAW_DATA[1](0x22) and SMP_AVE[5:3](0x22) must be set to zero.

THRESH2_MEAS_SEL	Measurement Selected for Threshold 2
0x0	Threshold 2 is disabled
0x1	MEAS1
0x2	MEAS2
0x3	MEAS3
0x4	MEAS4
0x5	MEAS5
0x6	MEAS6
0x7	Do not use

THRESH1_MEAS_SEL

THRESH1_MEAS_SEL enables the threshold detect function and selects the PPG measurement for the first instance of the threshold function. For details see the Threshold Detect Function section.

If the threshold detect function is enabled, COLLECT_RAW_DATA[1](0x22) and SMP_AVE[5:3](0x22) must be set to zero.

THRESH1_MEAS_SEL	Measurement Selected for Threshold 1
0x0	Threshold 1 is disabled
0x1	MEAS1
0x2	MEAS2
0x3	MEAS3
0x4	MEAS4
0x5	MEAS5
0x6	MEAS6
0x7	Do not use

THRESHOLD HYST (0x71)

BIT	7	6	5	4	3	2	1	0	
Field	THRESH2_PPG_SEL	THRESH1_PPG_SEL	—	TIME_HYST[1:0]		LEVEL_HYST[2:0]			
Reset	0	0	—	0x0		0x0			
Access Type	Write, Read	Write, Read	—	Write, Read		Write, Read			

THRESH2_PPG_SEL

THRESH2_PPG_SEL selects the optical channel for THRESHOLD 2.

THRESH2_PPG_SEL	Optical Channel for Threshold 2
0	PPG1
1	PPG2

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THRESH1_PPG_SEL selects the optical channel for THRESHOLD 1.

THRESH1_PPG_SEL	Optical Channel for Threshold 1
0	PPG1
1	PPG2

TIME_HYST

Time hysteresis selects the number of consecutive samples outside the limits defined by THRESHOLDx_UPPER and THRESHOLDx_LOWER in order to trigger the threshold interrupt THRESHx_HILO. TIME_HYST applies to both instances of threshold interrupts. For details, see the Threshold Detect Function section.

TIME_HYST	Number of Samples before Interrupt is Set
0x0	Time hysteresis is disabled
0x1	2
0x2	4
0x3	8

LEVEL_HYST

LEVEL_HYST sets the variation in ADC counts permitted when the THRESHx_HILO interrupt is triggered. This value is in ADC counts and is applied at $\pm 0.5 \times$ LEVEL_HYST around the THRESHOLDx_UPPER and THRESHOLDx_LOWER. LEVEL_HYST applies to both instances of threshold interrupts. For details, see the Threshold Detect Function section.

Level_HYST	Magnitude of Hysteresis (LSBs)
0x0	Level Hysteresis is disabled
0x1	2
0x2	4
0x3	8
0x4	16
0x5	32
0x6	64
0x7	128

PPG HI THRESHOLD1 (0x72)

BIT	7	6	5	4	3	2	1	0
Field	THRESHOLD1_UPPER[7:0]							
Reset	0xFF							
Access Type	Write, Read							

THRESHOLD1_UPPER

Defines the upper threshold limit for THRESHOLD x ($x = 1, 2$). Each LSB of THRESHOLDx_UPPER represents 2048 LSBs of the corresponding selected measurement (THRESHx_MEAS_SEL) ADC code.

THRESHOLDx_UPPER must be programmed to be greater than THRESHOLDx_LOWER; otherwise, the interrupt behavior is undefined.

THRESHOLDx_UPPER ($x = 1, 2$)	Upper Limit for THRESHOLD x
0x00	0, upper threshold is disabled

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THRESHOLDx_UPPER ($x = 1, 2$)	Upper Limit for THRESHOLD x
0x01	2048
0x02	4096
0x03	6144
•	•
•	•
•	•
0xFD	518144
0xFE	520192
0xFF	522240

PPG LO THRESHOLD1 (0x73)

BIT	7	6	5	4	3	2	1	0
Field	THRESHOLD1_LOWER[7:0]							
Reset	0x00							
Access Type	Write, Read							

THRESHOLD1_LOWER

Defines the lower threshold limit for THRESHOLD x ($x = 1, 2$). Each LSB of THRESHOLDx_LOWER represents 2048 LSBs of the selected measurement (THRESHx_MEAS_SEL) ADC code.

THRESHOLDx_LOWER	Lower Limit for THRESHOLDx
0x00	0
0x01	2048
0x02	4096
0x03	6144
•	•
•	•
•	•
0xFD	518144
0xFE	520192
0xFF	522240

PPG HI THRESHOLD2 (0x74)

BIT	7	6	5	4	3	2	1	0
Field	THRESHOLD2_UPPER[7:0]							
Reset	0xFF							
Access Type	Write, Read							

THRESHOLD2_UPPER

See THRESHOLD1_UPPER for details.

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PPG LO THRESHOLD2 (0x75)

BIT	7	6	5	4	3	2	1	0
Field	THRESHOLD2_LOWER[7:0]							
Reset	0x00							
Access Type	Write, Read							

THRESHOLD2_LOWER

See THRESHOLD1_LOWER for details.

ECG Configuration 1 (0x80)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	ECG_DEC_RATE[2:0]			ECG_EN
Reset	—	—	—	—	0x0			0
Access Type	—	—	—	—	Write, Read			Write, Read

ECG_DEC_RATE

ECG_DEC_RATE sets the decimation ratio for the ECG_ADC as detailed in the table below.

For information on how to set ECG_DEC_RATE see the Timing Subsystem section

ECG_DEC_RATE	DECIMATION RATIO
0x0	16
0x1	32
0x2	64
0x3	128
0x4	256
0x5	512
0x6	512
0x7	512

ECG_EN

ECG_EN enables the ECG channel and ECG data conversions.

ECG_EN	DECODE
0	ECG is disabled.
1	ECG is enabled.

ECG Configuration 2 (0x81)

BIT	7	6	5	4	3	2	1	0
Field	ECG_IPOL	ECG_PGA_GAIN[2:0]				ECG_INA_RGE[1:0]		ECG_INA_GAIN[1:0]
Reset	0	0x0				0x0		0x1
Access Type	Write, Read	Write, Read			Write, Read		Write, Read	

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ECG_IPOL

ECG_IPOL selects the ECG input polarity.

ECG_IPOL	ECG INPUT POLARITY
0	Non-Inverted
1	Inverted

ECG_PGA_GAIN

ECG_PGA_GAIN selects the gain for the PGA in the ECG channel. The total ECG channel gain is the product of INA gain and PGA gain.

ECG_PGA_GAIN	PGA GAIN (V/V)
0x0	1
0x1	2
0x2	4
0x3	8
0x4	Do not use
0x5	Do not use
0x6	Do not use
0x7	16

ECG_INA_RGE

ECG_INA_RGE selects the gain range of the ECG input amplifier.

See ECG_INA_GAIN for details.

ECG_INA_GAIN

ECG_INA_GAIN selects the gain of the ECG input amplifier. See the ECG Noise Measurements section for typical noise performance at each gain setting.

ECG_INA_GAIN	INA GAIN (V/V)				
	ECG_INA_RGE = 0x0	ECG_INA_RGE = 0x1	ECG_INA_RGE = 0x2	ECG_INA_RGE = 0x3	
0x0	10	7.5	5	2.5	
0x1	20	15	10	5	
0x2	40	30	20	10	
0x3	60	45	30	15	

ECG Configuration 3 (0x82)

BIT	7	6	5	4	3	2	1	0
Field	—	—	—	—	ECG_IMP_HI	ECG_AUTO_REC	ECG_MUX_SEL[1:0]	
Reset	—	—	—	—	0	0	0x0	
Access Type	—	—	—	—	Write, Read	Write, Read	Write, Read	

ECG_IMP_HI

ECG_IMP_HI selects the combined output impedance of CAPP and CAPN. This impedance together with the value of the external capacitor connected between CAPP and CAPN sets the HPF corner frequency of the ECG channel.

If ECG_IMP_HI is set to 0 then the input impedance is independent of the ECG_INA_RGE setting.

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If ECG_IMP_HI is set to 1 then the input impedance is dependent on the ECG_INA_RGE setting.

ECG_INA_RGE	CAPP AND CAPN COMBINED OUTPUT IMPEDANCE (kΩ)	
	ECG_IMP_HI = 0	ECG_IMP_HI = 1
0x0	400	400
0x1	400	533
0x2	400	800
0x3	400	1600

ECG_AUTO_REC

ECG_AUTO_REC enables analog automatic recovery mode in the ECG INA. When enabled, the INA automatically enables the fast recovery buffers when the INA is saturated.

ECG_AUTO_REC	DECODE
0	Analog automatic fast recovery disabled
1	Analog automatic fast recovery enabled

ECG_MUX_SEL

ECG_MUX_SEL[1:0] defines how ECGP/ECGN inputs and RLD output are routed to the ECG_EL1/2/3 pins. The selection table is shown below. The pins are disconnected from the ECG/RLD circuit blocks by default. ECG_OPEN_P and ECG_OPEN_N must also be set to 0 to connect the ECG inputs.

ECGP and ECGN connections can be swapped by the ECG_IPOL bit. For example, ECG_EL1 is routed to the ECGP input, and ECG_EL2 is routed to the ECGN input when ECG_RLD_MUX_SEL = 0x1 if ECG_IPOL = 0. ECG_EL1 is routed to ECGN input, and vice versa, if ECG_IPOL = 1.

ECG_MUX_SEL	ECGP	ECGN	RLD
0x0	N/C	N/C	N/C
0x1	ECG_EL1	ECG_EL2	ECG_EL3
0x2	ECG_EL3	ECG_EL1	ECG_EL2
0x3	ECG_EL2	ECG_EL3	ECG_EL1

ECG Configuration 4 (0x83)

BIT	7	6	5	4	3	2	1	0		
Field	EN_ECG_FAST_REC[1:0]			ECG_FAST_REC_THRESHOLD[5:0]						
Reset	0x0			0x3F						
Access Type	Write, Read			Write, Read						

EN_ECG_FAST_REC

EN_ECG_FAST_REC enables digital automatic fast recovery mode or manual mode in the ECG INA. Manual fast recovery mode remains active once it is enabled until it is manually disabled by setting EN_ECG_FAST_REC to 0x0. Automatic fast recovery mode is activated when the ECG ADC count is outside of the threshold set by ECG_FAST_REC_THRESHOLD for approximately 125ms, and remains active for approximately 500ms.

EN_ECG_FAST_REC	DECODE
0x0	Normal mode
0x1	Manual fast recovery mode enabled
0x2	Digital automatic fast recovery mode enabled
0x3	Do not use

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Vital-Sign AFE****ECG_FAST_REC_THRESHOLD**

If EN_ECG_FAST_REC is set to 0x2 (digital automatic fast-recovery mode) and the output of an ECG measurement exceeds the symmetric thresholds defined by $\pm(2048 \times \text{ECG_FAST_REC_THRESHOLD})$ for more than 125ms, the fast recovery mode is automatically engaged and remains active for 500ms. The default value (ECG_FAST_REC_THRESHOLD = 0x3F) corresponds to an ECG output upper threshold of 0x1F800 and an ECG output lower threshold of 0x20800, or $\pm 98.4\%$ of full-scale.

ECG CAL Configuration 1 (0x84)

BIT	7	6	5	4	3	2	1	0
Field	ECG_CAL_HIGH[10:8]			ECG_CAL_FREQ[2:0]			ECG_CAL_DUTY	ECG_CAL_EN
Reset	0x0			0x0			0	0
Access Type	Write, Read			Write, Read			Write, Read	Write, Read

ECG_CAL_HIGH

ECG_CAL_HIGH[10:8] are the most significant 3 bits of ECG_CAL_HIGH[10:0]. ECG_CAL_HIGH[10:0] determines the time high (or duty cycle) for the calibration source when ECG_CAL_DUTY is set to 0. Time high is calculated by the equation

$t_{HIGH} = \text{ECG_CAL_HIGH}[10:0] \times 1 / \text{ECG_ADC_CLK}$, where ECG_ADC_CLK is between 19kHz and 32.768kHz (see the Timing Subsystem section).

t_{HIGH} should be lower than the calibration frequency period set by ECG_CAL_FREQ.

ECG_CAL_FREQ

ECG_CAL_FREQ selects the frequency of the calibration source (f_{CAL}), relative to the ECG ADC clock.

CAL_FREQ	CALIBRATION SIGNAL FREQUENCY	CALIBRATION SIGNAL FREQUENCY WITH ECG_ADC_CLK = 32.768kHz (Hz)
0x0	ECG_ADC_CLK / 128	256
0x1	ECG_ADC_CLK / 512	64
0x2	ECG_ADC_CLK / 2048	16
0x3	ECG_ADC_CLK / 8192	4
0x4	ECG_ADC_CLK / 2 ¹⁵	1
0x5	ECG_ADC_CLK / 2 ¹⁷	1/4
0x6	ECG_ADC_CLK / 2 ¹⁹	1/16
0x7	ECG_ADC_CLK / 2 ²¹	1/64

ECG_CAL_DUTY

ECG_CAL_DUTY selects between time-high and 50% duty modes of the calibration source.

CAL_DUTY	DECODE
0	Use CAL_HIGH to select time high.
1	Duty cycle is 50%

ECG_CAL_EN

When ECG_EN is set to 1, ECG_CAL_EN enables ECG calibration sources VCALP and VCALN. Before enabling the calibration voltage sources, ensure that the input switches are disconnected (OPEN_P and OPEN_N are set to 1 in register 0xA2).

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		DECODE
0	ECG calibration sources and modes disabled	
1	ECG calibration sources and modes enabled	

ECG CAL Configuration 2 (0x85)

BIT	7	6	5	4	3	2	1	0
Field	ECG_CAL_HIGH[7:0]							
Reset	0x00							
Access Type	Write, Read							

ECG_CAL_HIGH

ECG_CAL_HIGH[7:0] are the least significant 8 bits of ECG_CAL_HIGH[10:0]. See ECG_CAL_HIGH[10:8] for details.

ECG CAL Configuration 3 (0x86)

BIT	7	6	5	4	3	2	1	0
Field	ECG_OPE_N_P	ECG_OPE_N_N	ECG_CAL_MODE	ECG_CAL_MAG	ECG_CAL_P_SEL[1:0]		ECG_CAL_N_SEL[1:0]	
Reset	1	1	0	0	0x0		0x0	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	

ECG_OPEN_P

ECG_OPEN_P controls the ECGP input switch. This switch must be connected (ECG_OPEN_P = 0) to measure a patient ECG signal, and must be disconnected (ECG_OPEN_P = 1) before enabling the calibration voltage sources.

ECG_OPEN_P	DECODE
0	The ECGP pin is internally connected to the ECG channel
1	The ECGP pin is internally isolated from the ECG channel

ECG_OPEN_N

ECG_OPEN_N controls the ECGN input switch. This switch must be connected (ECG_OPEN_N = 0) to measure a patient ECG signal, and must be disconnected (ECG_OPEN_N = 1) before enabling the calibration voltage sources.

ECG_OPEN_N	DECODE
0	The ECGN pin is internally connected to the ECG channel
1	The ECGN pin is internally isolated from the ECG channel

ECG_CAL_MODE

ECG_CAL_MODE is used to select the mode of calibration source.

ECG_CAL_MODE	DECODE
0	Unipolar, sources swing between ($V_{MID_ECG} \pm V_{CAL_MAG}$) and (V_{MID_ECG})
1	Bipolar, sources swing between ($V_{MID_ECG} + V_{CAL_MAG}$) and ($V_{MID_ECG} - V_{CAL_MAG}$)

ECG_CAL_MAG

ECG_CAL_MAG selects the magnitude of the calibration sources.

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ECG_CAL_MAG	DECODE
0	$V_{CAL_MAG} = 0.5\text{mV}$
1	$V_{CAL_MAG} = 1.0\text{mV}$

ECG_CAL_P_SEL

ECG_ECG_CAL_P_SEL selects which calibration voltage source is connected to the ECGP input.

ECG_CAL_P_SEL	DECODE
0x0	No calibration signal applied
0x1	ECGP is connected to V_{MID_ECG}
0x2	ECGP is connected to VCALP (only available if ECG_CAL_EN = 1)
0x3	ECGP is connected to VCALN (only available if ECG_CAL_EN = 1)

ECG_CAL_N_SEL

ECG_CAL_N_SEL selects which calibration voltage source is connected to the ECGN input.

ECG_CAL_N_SEL	DECODE
0x0	No calibration signal applied
0x1	ECGN is connected to V_{MID_ECG}
0x2	ECGN is connected to VCALP (only available if ECG_CAL_EN = 1)
0x3	ECGN is connected to VCALN (only available if ECG_CAL_EN = 1)

ECG Lead Detect Configuration 1 (0x88)

BIT	7	6	5	4	3	2	1	0
Field	EN_ECG_L_ON	EN_ECG_L_OFF	-	-	ECG_LOFF_MODE	ECG_LOFF_FREQ[2:0]		
Reset	0	0	-	-	0	0x0		
Access Type	Write, Read	Write, Read	-	-	Write, Read	Write, Read		

EN_ECG_LON

EN_ECG_LON enables ultra-low-power (ULP) DC lead-on detection. ECG lead-on detection only functions when ECG is disabled (ECG_EN[0](0x80) = 0).

EN_ECG_LON	DECODE
0	ECG lead-on detection is disabled
1	ECG lead-on detection is enabled

EN_ECG_LOFF

EN_ECG_LOFF enables lead-off detection, which is either DC lead-off detection or AC lead-off detection depending on ECG_LOFF_MODE.

If ECG is not enabled, EN_ECG_LOFF is ignored and lead-off detection is disabled.

ECG_LOFF_MODE

ECG_LOFF_MODE selects between DC and AC lead-off detection.

ECG_LOFF_MODE	DECODE
0	DC lead-off detection mode

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ECG_LOFF_MODE	DECODE
1	AC lead-off detection mode

ECG_LOFF_FREQ

ECG_LOFF_FREQ selects the frequency divider of the square-wave stimulus frequency for AC lead-off, by dividing the ECG_ADC_CLK by N.

For information on how to set ECG_LOFF_FREQ see the Timing Subsystem section.

ECG_LOFF_FREQ		N DIVIDER
0x0		Stimulus disabled (DC)
0x1		4
0x2		8
0x3		16
0x4		32
0x5		64
0x6		128
0x7		256

ECG Lead Detect Configuration 2 (0x89)

BIT	7	6	5	4	3	2	1	0
Field	ECG_LOFF_IPOL	ECG_LOFF_IMAG[2:0]					ECG_LOFF_THRESH[3:0]	
Reset	0	0x0					0x0	
Access Type	Write, Read	Write, Read					Write, Read	

ECG_LOFF_IPOL

ECG_LOFF_IPOL selects the current polarity for ECG DC lead-off detection.

ECG_LOFF_IPOL	POLARITY
0	Non-inverted. ECGP sources current, ECGN sinks current.
1	Inverted. ECGP sinks current, ECGN sources current.

ECG_LOFF_IMAG

ECG_LOFF_IMAG selects the DC/AC lead-off current amplitude.

ECG_LOFF_IMAG	ECG DC/AC LEAD-OFF CURRENT (nA/nAPk)
0x0	0 (sources are disabled and disconnected)
0x1	5
0x2	10
0x3	20
0x4	50
0x5	100
0x6	200
0x7	400

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ECG_LOFF_THRESH

ECG_LOFF_THRESH selects the voltage threshold for the DC or AC lead-off window comparators, which are centered at V_{MID_ECG} . If the voltage of either ECGP or ECGN goes above the high threshold or below the low threshold, the corresponding ECG_DC_LOFF status bit is set to 1 in register 0x03.

ECG_DC_LOFF_THRESH		ECG DC/AC LEAD-OFF THRESHOLD
	0x0	$V_{MID_ECG} \pm 25\text{mV}$
	0x1	$V_{MID_ECG} \pm 50\text{mV}$
	0x2	$V_{MID_ECG} \pm 75\text{mV}$
	...	
	0xE	$V_{MID_ECG} \pm 375\text{mV}$
	0xF	$V_{MID_ECG} \pm 400\text{mV}$

ECG Lead Bias Configuration 1 (0x90)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	ECG_RBIAS_VALUE[1:0]		EN_ECG_R_BIASP	EN_ECG_R_BIASN
Reset	-	-	-	-	0x0		0	0
Access Type	-	-	-	-	Write, Read	Write, Read	Write, Read	Write, Read

ECG_RBIAS_VALUE

ECG_RBIAS_VALUE selects the ECG lead bias resistance, which is between ECGP and V_{MID_ECG} ($EN_ECG_RBIASP = 1$), and ECGN and V_{MID_ECG} ($EN_ECG_RBIASN = 1$).

ECG_RBIAS_VALUE	BIAS RESISTANCE (MΩ)
0x0	50
0x1	100
0x2	200
0x3	Do not use

EN_ECG_RBIASP

EN_ECG_RBIASP enables the ECG lead bias between ECGP and V_{MID_ECG} with the value selected by ECG_RIAS_VALUE.

EN_ECG_RBIASP	DECODE
0	ECGP is not resistively connected to V_{MID_ECG} .
1	ECGP is connected to V_{MID_ECG} using a resistor selected by ECG_RBIAS_VALUE.

EN_ECG_RBIASN

EN_ECG_RBIASN enables ECG lead bias between ECGN and V_{MID_ECG} with the value selected by ECG_RIAS_VALUE.

EN_ECG_RBIAS_N	DECODE
0	ECGN is not resistively connected to V_{MID_ECG} .
1	ECGN is connected to V_{MID_ECG} using a resistor selected by ECG_RBIAS_VALUE.

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RLD Configuration 1 (0x92)

BIT	7	6	5	4	3	2	1	0
Field	RLD_EN	RLD_MOD_E	RLD_RBIA_S	EN_RLD_O_OR	ACTV_CM_P	ACTV_CM_N	RLD_GAIN[1:0]	
Reset	0	0	0	0	0	0	0	0x0
Access Type	Write, Read	Write, Read						

RLD_EN

RLD_EN enables the right leg drive circuit.

RLD_EN	DECODE
0	RLD is disabled and the RLD pin is high-impedance.
1	RLD is enabled.

RLD_MODE

RLD_MODE controls the RLD amplifier feedback switch used to control the right leg drive AC feedback loop.

RLD_MODE	DECODE
0	Open-loop body-bias mode. The feedback network is shorted and the RLD amplifier acts as a DC buffer to bias the body to a voltage selected by BODY_BIAS_DAC.
1	Closed-loop right leg drive mode. The RLD amplifier applies inverting gain to the AC common-mode input signal, forming a feedback loop through the body to bring the ECGP and ECIN inputs to the voltage selected by BODY_BIAS_DAC.

RLD_RBIA_S

RLD_RBIA_S selects the lead-bias voltage for the ECG or BioZ inputs, which is either the V_{MID_ECG} reference or the output of the right leg drive common mode averager (V_{RLD}).

RLD_RBIA_S	DECODE
0	V _{MID_ECG} is used as the lead-bias voltage
1	V _{RLD} is used as the lead-bias voltage

EN_RLD_OOR

EN_RLD_OOR enables the RLD out of range comparator, which sets the RLD_OOR[3](0x04) status bit if the RLD amplifier output voltage is below 0.127 x V_{AVDD} or above 0.870 x V_{AVDD}.

EN_RLD_OOR	DECODE
0	OOR comparator is disabled
1	OOR comparator is enabled

ACTV_CM_P

ACTV_CM_P enables the positive input to the common-mode averager. The positive input is taken from either ECGP or CAPP, selected by RLD_SEL_ECG[6](0x93). Enable both inputs for closed-loop right leg applications.

ACTV_CM_P	DECODE
0	Positive input is disabled. The input buffer is disabled and its output is high-impedance.
1	Positive input is enabled

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ACTV_CM_N

ACTV_CM_N enables the negative input to the common-mode averager. The positive input is taken from either ECGN or CAPN, selected by RLD_SEL_ECG[6](0x93). Enable both inputs for closed-loop right leg drive applications.

ACTV_CM_N	DECODE
0	Negative input is disabled. The input buffer is disabled and its output is high-impedance.
1	Negative input is enabled

RLD_GAIN

RLD_GAIN selects the internal RLD gain when RLD_EXT_RES is set to 0 and RLD_MODE is set to 1.

RLD_GAIN	GAIN WITH BOTH INPUTS ENABLES (V/V)
0x0	12
0x1	24
0x2	48
0x3	97

RLD Configuration 2 (0x93)

BIT	7	6	5	4	3	2	1	0
Field	RLD_EXT_RES	RLD_SEL_ECG	RLD_BW[1:0]		BODY_BIAS_DAC[3:0]			
Reset	0	0	0x0		0x0			
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			

RLD_EXT_RES

RLD_EXT_RES disconnects the internal feedback resistor to use an external gain-setting resistor. RLD_EXT_RES is effective only when RLD_MODE[6](0x92) is set to 1. The gain setting resistor R_{RLDFB} must be connected between the RLD and RLD_INV pins, which each have an internal $50\text{k}\Omega$ series resistor. The resulting gain is $(100\text{k}\Omega + R_{RLDFB}) / 150\text{k}\Omega$ when both common-mode averager inputs are enabled, and $(100\text{k}\Omega + R_{RLDFB}) / 250\text{k}\Omega$ when only one is enabled.

RLD_EXT_RES	DECODE
0	Internal RLD feedback resistor is connected. If an external feedback resistor is connected, the two resistances are in parallel.
1	Internal RLD feedback resistor is disconnected. Gain is set by the external feedback resistor.

RLD_SEL_ECG

RLD_SEL_ECG selects ECGP/ECGN or CAPP/CAPN as the inputs to the RLD common-mode averager. The common-mode averager input can be switched to the BioZ inputs by setting RLD_SEL_BIOZ[7](0xA7) to 1.

The voltages at CAPP/CAPN are buffered by the ECG INA, so their common-mode voltage lags slightly behind the ECGP/ECGN common-mode voltage. This introduces phase lag into the RLD feedback loop resulting in less common-mode signal attenuation.

RLD_SEL_BIOZ	RLD_SEL_ECG	RLD INPUT SELECTION
0	0	CAPP/CAPN
0	1	ECGP/ECGN
1	x	BIP/BIN

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RLD_BW

RLD_BW selects the bandwidth for the right leg drive amplifier.

RLD_BW	RLD BANDWIDTH (Hz)			
	RLD_GAIN = 12	RLD_GAIN = 24	RLD_GAIN = 48	RLD_GAIN = 97
0	917	697	647	555
1	937	724	698	648
2	944	733	716	681
3	948	736	724	696

BODY_BIAS_DAC

BODY_BIAS_DAC sets the voltage at the noninverting terminal of the RLD amplifier. The voltage is $V_{MID_ECG} - (BODY_BIAS_DAC \times 0.04V)$, where V_{MID_ECG} is 0.76V (typ), and BODY_BIAS_DAC is a 2's complement representation.

BODY_BIAS_DAC	DECODE
0x0	$V_{MID_ECG} = 0.76V$ (mid)
0x1	$V_{MID_ECG} - 1 \times 0.04V = 0.72V$
0x2	$V_{MID_ECG} - 2 \times 0.04V = 0.68V$
...	...
0x7	$V_{MID_ECG} - 7 \times 0.04V = 0.48V$ (min)
0x8	$V_{MID_ECG} + 8 \times 0.04V = 1.08V$ (max)
...	...
0xE	$V_{MID_ECG} + 2 \times 0.04V = 0.84V$
0xF	$V_{MID_ECG} + 1 \times 0.04V = 0.80V$

[BIOZ Configuration 1 \(0xA0\)](#)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_DAC_OSR[1:0]		BIOZ_ADC_OSR[2:0]				ECG_BIOZ_BG_EN	BIOZ_EN[1:0]
Reset	0x0				0x0		0	0x0
Access Type	Write, Read				Write, Read		Write, Read	

BIOZ_DAC_OSR

BIOZ_DAC_OSR[1:0] sets the oversample ratio of the BioZ DDS DAC. For information on how to set BIOZ_DAC_OSR[1:0], see the Timing Subsystem system.

BIOZ_DAC_OSR	DAC OVER SAMPLING RATIO
0x0	32
0x1	64
0x2	128
0x3	256

BIOZ_ADC_OSR

BIOZ_ADC_OSR[2:0] sets the oversample ratio of the BioZ ADC. For information on how to set BIOZ_ADC_OSR[2:0], see the Timing Subsystem section.

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BIOZ_ADC_OSR	ADC OVER SAMPLING RATIO
0x0	8
0x1	16
0x2	32
0x3	64
0x4	128
0x5	256
0x6	512
0x7	1024

ECG_BIOZ_BG_EN

ECG_BIOZ_BG_EN enables the shared ECG and BioZ bandgap bias, which is required for all functions except the ULP LON. The bias power-up time is approximately 512ms and should be kept on between subsequent measurements. The bandgap bias also automatically enables if the ECG or BioZ channels are enabled, but it is recommended to set ECG_BIOZ_BG_EN = 1 before starting measurements.

ECG_BIOZ_BG_EN	DECODE
0	ECG and BioZ bandgap bias disabled
1	ECG and BioZ bandgap bias enabled

BIOZ_EN

BIOZ_EN[1:0] enables the bioimpedance drive and receive channels for the in-phase (I channel) or quadrature-phase (Q channel) components when enabled when EN_UTIL_MODE is set to 0. This channel is disabled and is in a low-power state when BIOZ_EN[1:0] is set to 0x0 or 0x3.

See the FIFO Description for the Tags used for the I channel and Q channel data.

EN_UTIL_MODE	BIOZ_EN[1:0]	DECODE
0	0x0	Disable all BioZ measurements
0	0x1	Enable BioZ I measurement
0	0x2	Enable BioZ Q measurement
0	0x3	Disable all BioZ measurements
1	0xX	BioZ ADC used for Utility (see the description for EN_UTIL_MODE)

BIOZ Configuration 2 (0xA1)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_DHPF[1:0]		BIOZ_DLDPF[2:0]			-	-	EN_BIOZ_T_HRESH
Reset	0x0		0x0			-	-	0
Access Type	Write, Read		Write, Read			-	-	Write, Read

BIOZ_DHPF

BIOZ_DHPF sets the BioZ channel digital high-pass filter cutoff frequency.

BIOZ_DHPF[1:0]	CUTOFF FREQUENCY (Hz)
0x0	Bypass
0x1	0.00025 x SR_BIOZ
0x2	0.002 x SR_BIOZ

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BIOZ_DHPF[1:0]	CUTOFF FREQUENCY (Hz)
0x3	0.002 x SR_BIOZ

BIOZ_DLDPF

BIOZ_DLDPF sets the BioZ channel digital low-pass filter cutoff frequency.

BIOZ_DLDPF[2:0]	CUTOFF FREQUENCY (Hz)
0x0	Bypass
0x1	0.005 x SR_BIOZ
0x2	0.02 x SR_BIOZ
0x3	0.08 x SR_BIOZ
0x4 to 0x7	0.25 x SR_BIOZ

EN_BIOZ_THRESH

When EN_BIOZ_THRESH is set to 1, the BioZ I or Q data is compared with the BIOZ_LO_THRESH[7:0](0xA8) and BIOZ_HI_THRESH[7:0](0xA9) to detect a lead-off condition. The I or Q data is compared to the thresholds and is determined by BIOZ_EN[1:0](0xA0). The status is reflected in BIOZ_OVER[6](0x04) and BIOZ_UNDR[5](0x04).

When EN_BIOZ_THRESH is set to 0, the threshold compare function is disabled.

BIOZ Configuration 3 (0xA2)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_EXT_RES	–	BIOZ_VDRV_MAG[1:0]		BIOZ_IDRV_RGE[1:0]		BIOZ_DRV_MODE[1:0]	
Reset	0	–	0x0		0x0		0x0	
Access Type	Write, Read	–	Write, Read, Dual		Write, Read, Dual		Write, Read	

BIOZ_EXT_RES

BIOZ_EXT_RES selects the external R_{EXT} resistor or the internal range settings resistors.

When BIOZ_EXT_RES is set to 0, the internal range resistors are used and the current magnitude is set by both BIOZ_VDRV_MAG[5:4](0xA2) and BIOZ_IDRV_RGE[3:2](0xA2). BIOZ_VDRV_MAG and BIOZ_IDRV_RGE can be automatically overwritten depending on the stimulus frequency according to patient safety requirements. Note that R_{EXT} is not disconnected, so the DRVXR pin should be unconnected. If DRVXR is connected, R_{EXT} is connected in parallel with the internal range resistor, which results in a larger current magnitude.

When BIOZ_EXT_RES is set to 1, BIOZ_VDRV_MAG and the value of R_{EXT} set the current magnitude. BIOZ_VDRV_MAG is not automatically overwritten.

BIOZ_VDRV_MAG

In voltage drive mode, BIOZ_VDRV_MAG sets the voltage amplitude at DRVR, which is connected to BIOZ_EL1. BIOZ_IDRV_RGE is ignored.

In current drive mode, BIOZ_VDRV_MAG and BIOZ_IDRV_RGE set the current magnitude. See BIOZ_IDRV_RGE for details.

BIOZ_VDRV_MAG[1:0]	VOLTAGE MAGNITUDE (mV_{PK})	VOLTAGE MAGNITUDE (mV_{RMS})
0x0	50	35.4
0x1	100	70.7
0x2	250	177
0x3	500	354

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BIOZ_IDRV_RGE[1:0] sets the value of the internal current range resistor, which determines the current magnitude when BIOZ_EXT_RES = 0.

BIOZ_IDRV_RGE[1:0]	INTERNAL RANGE RESISTOR VALUE
0x0	552.5kΩ (VDRV magnitude reduced by 4x)
0x1	110.5kΩ
0x2	5.525kΩ
0x3	276.25Ω

When BIOZ_EXT_RES = 1, the external resistor connected between DRVXR and DRVXC, and determines the drive-current amplitude: $I_{MAG} = V_{DRV} / R_{EXT}$.

When BIOZ_EXT_RES = 0, BIOZ_VDRV_MAG and BIOZ_IDRV_RGE together select the magnitude of the stimulus current. When BIOZ_IDRV_RGE = 0x0 in current mode, the drive voltage at DRVR is reduced by a factor of four to support smaller current magnitudes.

BIOZ_IDRV_RGE[1:0]	BIOZ_VDRV_MAG[1:0]	AMPLITUDE OF V_{DRV} (mV _{PK})	AMPLITUDE OF V_{DRV} (mV _{RMS})	AMPLITUDE OF CURRENT (PEAK)	AMPLITUDE OF CURRENT (RMS)
0x0	0x0	12.5	8.8	23nA	16nA
0x0	0x1	25	17.7	45nA	32nA
0x0	0x2	62.5	44.2	113nA	80nA
0x0	0x3	125	88.4	226nA	160nA
0x1	0x0	50	35.4	452nA	320nA
0x1	0x1	100	70.7	905nA	640nA
0x1	0x2	250	177	2.262μA	1.6μA
0x1	0x3	500	354	4.525μA	3.2μA
0x2	0x0	50	35.4	9.05μA	6.4μA
0x2	0x1	100	70.7	18.10μA	12.8μA
0x2	0x2	250	177	45.25μA	32μA
0x2	0x3	500	354	90.50μA	64μA
0x3	0x0	50	35.4	181μA	128μA
0x3	0x1	100	70.7	362μA	256μA
0x3	0x2	250	177	905μA	640μA
0x3	0x3	500	354	1.81mA	1.28mA

BIOZ_DRV_MODE

BIOZ_DRV_MODE selects the stimulus type of the BioZ transmit channel.

When RESP_EN[0](0xB6) = 1, BIOZ_DRV_MODE is ignored.

BIOZ_DRV_MODE[1:0]	DRIVE TYPE
0x0	Current Drive. A sine-wave current is driven into the body through selectable electrode pins.
0x1	Voltage Drive. A sine-wave voltage is applied to BIOZ_EL1 while BIOZ_EL4 is driven to V _{MID_TX} .
0x2	H-Bridge Drive. BIOZ_EL1 and BIOZ_EL4 are alternately switched between AVDD and AGND.
0x3	Standby. The transmit channel is reset and held in a low-power state, driving the electrodes to V _{MID_TX} .

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BIOZ Configuration 4 (0xA3)

BIT	7	6	5	4	3	2	1	0
Field	EN_UTIL_MODE	–	–	–	–	–	–	–
Reset	0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

EN_UTIL_MODE

When EN_UTIL_MODE is set to 0, BIOZ_EN[1:0] selects the I or Q channel.

When EN_UTIL_MODE is set to 1, the BioZ ADC is used as a utility ADC to sense a differential ECG-related voltage selected by BIOZ_EN[1:0].

See the FIFO Description section for the Tags used in this mode.

EN_UTIL_MODE	BIOZ_EN	UTILITY FUNCTION
0	0x0 to 0x3	Utility mode is disabled.
1	0x0	$V_{ECGP} - V_{ECGN}$ differential input is connected to the BioZ channel.
1	0x1	$V_{ECGP} - V_{MID_ECG}$ differential input is connected to the BioZ channel.
1	0x2	$V_{ECGN} - V_{MID_ECG}$ differential input is connected to the BioZ channel.
1	0x3	$V_{CAPP} - V_{CAPN}$ differential input is connected to the BioZ channel.

BIOZ Configuration 5 (0xA4)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_DC_CODE_SEL				BIOZ_DC_DAC_CODE[6:0]			
Reset	0				0x00			
Access Type	Write, Read				Write, Read			

BIOZ_DC_CODE_SEL

When BIOZ_DC_CODE_SEL is set to 0, the DDS DAC code (sine-wave sample) is selected for the 10-bit BioZ DAC. When BIOZ_DC_CODE_SEL is set to 1, BIOZ_DC_DAC_CODE[6:0] is selected for the upper 7 bits of the BioZ DAC, and the lower 3 bits are set to 0.

BIOZ_DC_DAC_CODE

BIOZ_DC_DAC_CODE[6:0] are the upper 7 bits of the 10-bit DC code for the BioZ DAC when BIOZ_DC_CODE_SEL is set to 1. The lower 3 bits for the DAC code are set to 0.

BIOZ Configuration 6 (0xA5)

BIT	7	6	5	4	3	2	1	0
Field		BIOZ_AHPF[3:0]			BIOZ_INA_MODE	BIOZ_DM_DIS		BIOZ_GAIN[1:0]
Reset		0x0			0	0		0x0
Access Type		Write, Read			Write, Read	Write, Read		Write, Read

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BIOZ_AHPF sets the corner frequency of the internal analog high-pass filter, or sets the filter resistance when using external capacitors on BIP and BIN. The resistance is center tapped with the midpoint connected to V_{MID_RX} through a 100MΩ resistor. The 100MΩ midpoint resistor can be bypassed by settings BIOZ_CMRES_DIS[5](0xA7) to 1. When using external capacitors, the analog HPF corner frequency is set by the series capacitance and the selected common-mode resistance according to the following equation:

- $f_{-3dB} = 1/(2 \times \pi \times R_{AHPF} \times C_{SERIES})$

where C_{SERIES} is the series combination of the external capacitors on BIP and BIN:

- $C_{SERIES} = (C_{BIP} \times C_{BIN}) / (C_{BIP} + C_{BIN})$

BIOZ_AHPF[3:0]	DECODE
0x0	100Hz
0x1	200Hz
0x2	500Hz
0x3	1,000Hz
0x4	2,000Hz
0x5	5,000Hz
0x6	10,000Hz
0x7	Resistor opened, internal capacitors shorted (AHPF bypassed)
0x8	42.4MΩ, internal capacitors shorted
0x9	21.2MΩ, internal capacitors shorted
0xA	8.4MΩ, internal capacitors shorted
0xB	4.2MΩ, internal capacitors shorted
0xC	2.2MΩ, internal capacitors shorted
0xD	848kΩ, internal capacitors shorted
0xE	848kΩ, internal capacitors shorted
0xF	Resistor opened, internal capacitor shorted (AHPF bypassed)

BIOZ_INA_MODE

BIOZ_INA_MODE sets the BioZ receive channel instrumentation amplifier (INA) power mode.

BIOZ_INA_MODE	DECODE
0	BioZ INA is in high-power mode (low noise mode)
1	BioZ INA is in low-power mode

BIOZ_DM_DIS

BIOZ_DM_DIS disables the BioZ receive channel demodulator to allow a direct conversion of the differential input voltage across BIP and BIN.

BIOZ_DM_DIS	DECODE
0	BioZ demodulation clock enabled
1	BioZ demodulation clock disabled

BIOZ_GAIN

BIOZ_GAIN sets the combined gain of the BioZ receive channel INA and PGA.

BIOZ_GAIN[1:0]	TOTAL GAIN (V/V)	INA GAIN (V/V)	PGA GAIN (V/V)
0x0	1	1	1

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BIOZ_GAIN[1:0]	TOTAL GAIN (V/V)	INA GAIN (V/V)	PGA GAIN (V/V)
0x1	2	2	1
0x2	5	2	2.5
0x3	10	2	5

BIOZ Configuration 7 (0xA6)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_EXT_CAP	BIOZ_DC_RESET	BIOZ_DRV_RESET	BIOZ_DAC_RESET	BIOZ_AMP_RGE[1:0]	BIOZ_AMP_BW[1:0]		
Reset	1	0	0	0	0x0	0x0		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

BIOZ_EXT_CAP

BIOZ_EXT_CAP selects the external capacitor C_{EXT} connected between DRVXC and DRVSJ, which AC-couples the stimulus current in current mode; thus, preventing DC current from passing into the patient stimulus electrodes. When not using an AC-coupling external capacitor, it is recommended to short DRVXC and DRVSJ since the internal switch on-resistance is approximately 35Ω .

BIOZ_EXT_CAP	DECODE
0	No external capacitor used. The internal switch shorts the DRVXC and DRVSJ pins together with an on-resistance of approximately 35Ω .
1	External capacitor used. The internal switch is open, and AC current is coupled through the external capacitor.

BIOZ_DC_RESET

BIOZ_DC_RESET closes the DC_RESET switch in the current-generator amplifier circuit, which applies a feedback resistance of approximately $10M\Omega$ to the current-drive amplifier. This maintains the DC bias of the drive electrodes during a lead-off event, which reduces the amplifier setting time when the lead is reconnected.

When using external AC coupling capacitors on the pins assigned to DRVP or DRVN, it is recommended to set DC_RESET to 1 to absorb any DC offset currents and prevent amplifier saturation.

BIOZ_DC_RESET	DECODE
0	DC_RESET switch is open. No feedback resistance is applied to the current drive amplifier.
1	DC_RESET switch is closed. A $10M\Omega$ feedback resistance is applied to the current-drive amplifier.

BIOZ_DRV_RESET

BIOZ_DRV_RESET places the BioZ transmit channel in a reset state by disabling the DDS DAC and closing the RESET switch of the current-drive amplifier. This shorts the feedback network of the amplifier, configuring it as a unity gain buffer and driving both drive electrodes to V_{MID_TX} .

BIOZ_DRV_RESET	DECODE
0	Normal Operation. The RESET switch is open.
1	Reset Condition. The DDS DAC is disabled and the RESET switch is closed, shorting the current drive amplifier feedback.

BIOZ_DAC_RESET

BIOZ_DAC_RESET forces the DDS DAC output to zero. The human body load is driven by the reference voltage V_{MID_TX} , and the AC current going through the human body load is zero.

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BIOZ_AMP_RGE

BIOZ_AMP_RGE selects the output stage option for the voltage-drive amplifier and current-drive amplifier within the BioZ transmit channel. Higher strength is recommended for higher output current loading. Higher settings increase supply-current consumption.

It is recommended to match this settings with the BIOZ_IDRV_RGE setting.

BIOZ_AMP_RGE[1:0]		BIOZ AMPLIFIER RANGE
0x0	Low	
0x1	Medium-Low	
0x2	Medium-High	
0x3	High	

BIOZ_AMP_BW

BIOZ_AMP_BW sets the gain bandwidth of the voltage-drive amplifier and current-drive amplifier in the BioZ transmit channel. Higher bandwidth is recommended for high-frequency applications including bioimpedance analysis and impedance cardiography. Low bandwidth is recommended for low-frequency applications including galvanic skin response to reduce power consumption.

BIOZ_AMP_BW[1:0]		BIOZ AMPLIFIER BANDWIDTH
0x0	Low	
0x1	Medium-Low	
0x2	Medium-High	
0x3	High	

BIOZ Configuration 8 (0xA7)

BIT	7	6	5	4	3	2	1	0
Field	RLD_SEL_BIOZ	RLD_DRV	BIOZ_CMRES_DIS	BIOZ_STBY_ON	BIOZ_IPOL	BIOZ_FAST	BIOZ_INA_CHOP_EN	BIOZ_CH_F_SEL
Reset	0	0	0	0	0		0	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

RLD_SEL_BIOZ

RLD_SEL_BIOZ selects the BIP and BIN voltages as the inputs for the RLD common mode averager, and overrides RLD_SEL_ECG.

RLD_SEL_BIOZ		RLD_SEL_ECG	RLD INPUT SELECTION
0	0		CAPP and CAPN
0	1		ECGP and ECGN
1	x		BIP and BIN

RLD_DRV

RLD_DRV selects between V_{MID_TX} and V_{RLD} for the BioZ transmit channel common-mode voltage, applied to the VDRV and IDR_V amplifiers' noninverting terminals. This enables the DRVN pin to function as right leg drive during BioZ measurements.

RLD_DRV	DECODE
0	V _{MID_TX} selected as the BioZ common-mode voltage.
1	V _{RLD} selected as the BioZ common-mode voltage.

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BIOZ_CMRES_DIS

BIOZ_CMRES_DIS controls the resistance between the analog HPF midpoint and V_{MID_RX} , which affects the common-mode input impedance of the BioZ receive channel when the analog HPF is enabled.

BIOZ_CMRES_DIS	DECODE
0	100MΩ
1	0Ω

BIOZ_STBYON

BIOZ_STBYON selects the BioZ receive channel behavior when the transmit channel is in standby mode (BIOZ_DRV_MODE = 0x3). When in standby mode, the transmit channel does not generate a stimulus, so the receive channel can be powered down in most cases.

BIOZ_STBYON	RECEIVE CHANNEL BEHAVIOR IN STANDBY MODE
0	Disabled. The receive channel amplifiers, demodulator, and ADC are disabled.
1	Enabled. The BioZ receive channel amplifiers, demodulator, and ADC remain enabled.

BIOZ_IPOL

BIOZ_IPOL selects the polarity of the BioZ receive channel by inverting the demodulator clock phase. This is useful if either the drive electrodes or the receive electrodes are connected with inverted polarity.

BIOZ_IPOL	DECODE
0	Non-inverted
1	Inverted

BIOZ_FAST

When BIOZ_FAST_START is set to 1, the FAST_START function is enabled until the register bit is set to 0.

The FAST START function is to connect the BioZ inputs to V_{MID_RX} through 10kΩ resistors. This helps to quickly establish the DC bias of the BioZ inputs, especially when the inputs have high capacitance.

This function can be applied any time after ECG_BIOZ_BG_EN is asserted, and is recommended to be used before BioZ measurements begin.

BIOZ_FAST	DECODE
0	Normal operation
1	BIP and BIN are resistively connected to V_{MID_RX} through 10kΩ resistors.

BIOZ_INA_CHOP_EN

BIOZ_INA_CHOP_EN enables 16kHz chopping in the BioZ receive channel instrumentation amplifier.

BIOZ_INA_CHOP_EN	DECODE
0	16kHz chopping disabled
1	16kHz chopping enabled

BIOZ_CH_FSEL

BIOZ_CH_FSEL selects the chopping frequency of the BioZ receive channel PGA and AAF.

Set to 0 if the F_BIOZ is not equal to BIOZ_ADC_CLK

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Set to 1 if the F_BIOZ is equal to BIOZ_ADC_CLK

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Note: The synthesis frequency CANNOT equal the PGA chopping frequency or the correlator will not work. Use BIOZ_CH_FSEL to ensure they are not equal.

BIOZ_CH_FSEL	DECODE
0	BioZ PGA chopping frequency is $f_{BIOZ_ADC_CLK} / 16$
1	BioZ PGA chopping frequency is $f_{BIOZ_ADC_CLK} / 8$

BIOZ Low Threshold (0xA8)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_LO_THRESH[7:0]							
Reset	0x00							
Access Type	Write, Read							

BIOZ_LO_THRESH

BIOZ_LO_THRESH sets the BioZ underrange threshold.

If the BioZ measurement is within the symmetric thresholds defined by $\pm 32 \times$ BIOZ_LO_THRESH for longer than approximately 128ms, the BIOZ_UNDR status bit is asserted.

BIOZ High Threshold (0xA9)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_HI_THRESH[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BIOZ_HI_THRESH

BIOZ_HI_THRESH sets the BioZ overrange threshold.

If the BioZ measurement is outside of the symmetric thresholds defined by $\pm 2048 \times$ BIOZ_HI_THRESH for longer than approximately 128ms, the BIOZ_OVER status bit is asserted.

The default value (BIOZ_HI_THRESH = 0xFF) corresponds to a BioZ output upper threshold of 0x7F800, or about 99.6% of the full-scale range.

BIOZ Mux Configuration 1 (0xAA)

BIT	7	6	5	4	3	2	1	0
Field	BMUX_RSEL[1:0]		BMUX_BIS_T_EN	–	–	CONNECT_CAL_ONLY	BIOZ_MUX_EN	BIOZ_CAL_EN
Reset	0x0		0	–	–	0	0	0
Access Type	Write, Read		Write, Read	–	–	Write, Read	Write, Read	Write, Read

BMUX_RSEL

BMUX_RSEL selects the value of the resistive calibration load applied across DRVP and BIP, and DRVN and BIN for non-GSR applications. This load is only applied when BMUX_BIST_EN = 1. The resistor error is measured during factory test, and the error value is saved in BIST_R_ERR[7:0](0xAD).

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BMUX_RSEL[1:0]	CALIBRATION RESISTANCE (Ω)
0x0	5000
0x1	800
0x2	500
0x3	200

BMUX_BIST_EN

BMUX_BIST_EN enables the built-in self-test resistor between DRVP and BIP, andDRVN and BIN for non-GSR applications. To avoid external interference, BIOZ_MUX_EN and BIOZ_CAL_EN should both be disabled when using BMUX_BIST_EN. The resistive value is selected by BMUX_RSEL.

BMUX_BIST_EN	DECODE
0	Disabled. The internal resistive load is disconnected.
1	Enabled. The internal resistive load is connected between DRVP and BIP, andDRVN and BIN.

CONNECT_CAL_ONLY

When both BIOZ_MUX_EN and BIOZ_CAL_EN are set to 1, enabling CONNECT_CAL_ONLY connects only the CAL1-CAL4 pins and disconnects the BIOZ_ELx pins. See BIOZ_MUX_EN for details.

BIOZ_MUX_EN

BIOZ_MUX_EN enables the BioZ input/output MUX connections to the BIOZ_ELx pins and/or CALx pins selected by DRVP_ASSIGN, DRVN_ASSIGN, BIP_ASSIGN, BIN_ASSIGN, BIOZ_CAL_EN, and CONNECT_CAL_ONLY.

BIOZ_MUX_EN	BIOZ_CAL_EN	CONNECT_CAL_ONLY	DECODE
0	X	X	MUX Disabled. All BIOZ_ELx and CALx pins are disconnected.
1	0	X	BIOZ_ELx pins are connected according to BIP_ASSIGN, BIN_ASSIGN, DRVP_ASSIGN, and DRVN_ASSIGN. CALx pins are disconnected.
1	1	0	BIOZ_ELx pins are connected according to BIP_ASSIGN, BIN_ASSIGN, DRVP_ASSIGN, and DRVN_ASSIGN. CALx pins are also connected.
1	1	1	BIOZ_ELx pins are disconnected. CALx pins are connected only.

BIOZ_CAL_EN

BIOZ_CAL_EN connects the calibration pins (CAL1-CAL4) of the BioZ input/output MUX to measure the external calibration resistor when BIOZ_MUX_EN = 1. See BIOZ_MUX_EN for details.

BIOZ Mux Configuration 2 (0xAB)

BIT	7	6	5	4	3	2	1	0
Field	BMUX_GSR_RSEL[1:0]		GSR_LOAD_EN	–	–	–	EN_EXT_IN LOAD	EN_INT_IN LOAD
Reset	0x0		0	–	–	–	0	0
Access Type	Write, Read		Write, Read	–	–	–	Write, Read	Write, Read

BMUX_GSR_RSEL

BMUX_GSR_RSEL selects the value of the resistive calibration load applied across DRVP and BIP, andDRVN and BIN for GSR applications. This load is only applied when GSR_LOAD_EN = 1.

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BMUX_GSR_RSEL[1:0]	LOAD RESISTANCE (kΩ)
0x0	25
0x1	100
0x2	500
0x3	1000

GSR_LOAD_EN

GSR_LOAD_EN enables the built-in GSR load resistor between DRVP and BIP, andDRVN and BIN. To avoid external interference, BIOZ_MUX_EN and BIOZ_CAL_EN should both be disabled when using GSR_LOAD_EN. The resistive value is selected by BMUX_GSR_RSEL.

GSR_LOAD_EN	DECODE
0	Disabled. The internal resistive load is disconnected.
1	Enabled. The internal resistive load is connected between DRVP and BIP, andDRVN and BIN.

EN_EXT_INLOAD

EN_EXT_INLOAD enables the external guard-trace-drive circuit, which outputs the buffered voltage from BIP and BIN onto the BIOZ_EL2 and BIOZ_EL3 pins.

EN_EXT_INLOAD	DECODE
0	External guard-drive circuit disabled.
1	External guard-drive circuit enabled.

EN_INT_INLOAD

EN_INT_INLOAD enables the circuit that compensates for input capacitive loading on BIN and BIP.

EN_INT_INLOAD	DECODE
0	Input capacitive loading compensation circuit disabled.
1	Input capacitive loading compensation circuit enabled.

BIOZ Mux Configuration 3 (0xAC)

BIT	7	6	5	4	3	2	1	0
Field	BIP_ASSIGN[1:0]		BIN_ASSIGN[1:0]		DRV_P_ASSIGN[1:0]			DRV_N_ASSIGN[1:0]
Reset	0x0		0x0		0x0			0x0
Access Type	Write, Read		Write, Read		Write, Read			Write, Read

BIP_ASSIGN

BIP_ASSIGN selects the electrode pin used for the BioZ positive input (BIP) when BIOZ_MUX_EN = 1. The MUX is also used to select the Utility ADC signal (see the Utility Mode Measurement section).

BIP_ASSIGN[1:0]	ASSIGNED ELECTRODE PIN
0x0	BIOZ_EL1
0x1	BIOZ_EL2A
0x2	BIOZ_EL2B
0x3	Utility ADC Mode

BIN_ASSIGN

BIN_ASSIGN selects the electrode pin used for the BioZ negative input (BIN) when BIOZ_MUX_EN = 1. The MUX is

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also used to select the utility ADC signal (see the Utility Mode Measurement section).

BIN_ASSIGN[1:0]	ASSIGNED ELECTRODE PIN
0x0	BIOZ_EL4
0x1	BIOZ_EL3A
0x2	BIOZ_EL3B
0x3	Utility ADC Mode

DRV_P_ASSIGN

DRV_P_ASSIGN selects the electrode pin used for the BioZ positive drive (DRV_P) in current mode when BIOZ_MUX_EN = 1.

In voltage mode or H-bridge mode, the BioZ positive drive only connects to BIOZ_EL1.

The BIOZ_EL1 MUX switch has lower on-resistance than BIOZ_EL2A and BIOZ_EL2B, so it is recommended to assign DRV_P to BIOZ_EL1 when BIOZ_IDRV_RGE = 0x3.

BIOZ_DRV_MODE[1:0]	DRV_P_ASSIGN[1:0]	ASSIGNED ELECTRODE PIN
0x0 or 0x3	0x0	BIOZ_EL1 (low resistance)
0x0 or 0x3	0x1	BIOZ_EL2A
0x0 or 0x3	0x2	BIOZ_EL2B
0x0 or 0x3	0x3	No Connection
0x1	X	BIOZ_EL1
0x2	X	BIOZ_EL1

DRV_N_ASSIGN

DRV_N_ASSIGN selects the electrode pin used for the BioZ negative drive (DRV_N) in current mode when BIOZ_MUX_EN = 1.

In voltage mode or H-bridge mode, the BioZ negative drive only connects to BIOZ_EL4.

The BIOZ_EL4 MUX switch has lower on-resistance than BIOZ_EL3A and BIOZ_EL3B, so it is recommended to assign DRV_N to BIOZ_EL4 when BIOZ_IDRV_RGE = 0x3.

BIOZ_DRV_MODE[1:0]	DRV_N_ASSIGN[1:0]	ASSIGNED ELECTRODE PIN
0x0 or 0x3	0x0	BIOZ_EL4 (low resistance)
0x0 or 0x3	0x1	BIOZ_EL3A
0x0 or 0x3	0x2	BIOZ_EL3B
0x0 or 0x3	0x3	No Connection
0x1	X	BIOZ_EL4
0x2	X	BIOZ_EL4

BIOZ Mux Configuration 4 (0xAD)

BIT	7	6	5	4	3	2	1	0
Field	BIST_R_ERR[7:0]							
Reset	0x00							
Access Type	Read Only							

BIST_R_ERR

The on-chip built-in self-test (BIST) resistors are available for calibrating the BioZ channel magnitude/phase error. 5kΩ,

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800Ω , 500Ω , or 200Ω of resistors can be chosen by BMUX_RSEL. Due to process variations, the actual resistances vary by up to $\pm 25\%$. During factory test, the actual resistance of the 800Ω resistor is measured, and the error stored in the BIST_R_ERR field. The actual resistance can be calculated with the following equation, where BIST_R_ERR is a 2's complement representation. The other values ($5k\Omega$, 500Ω , and 200Ω) are process-matched to the 800Ω resistor with approximately 2% precision.

$$R_{ACTUAL} = R_{NOMINAL} \times (1 + BIST_R_ERR / 512)$$

For example, when BIST_R_ERR = 64 and BMUX_RSEL = 0x1, $R_{ACTUAL} = 800\Omega \times (1 + 64 / 512) = 900\Omega$.

BIST_R_ERR is a read-only register.

BIOZ Lead Detect Configuration 1 (0xB0)

BIT	7	6	5	4	3	2	1	0
Field	EN_BIOZ_L_ON	EN_BIOZ_L_OFF	EN_EXT_BI_OZ_LOFF	EN_BIOZ_DRV_OOR	BIOZ_LOFF_IPOL	BIOZ_LOFF_IMAG[2:0]		
Reset	0	0	0	0	0	0x0		
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		

EN_BIOZ_LON

EN_BIOZ_LON enables ultra-low-power (ULP) DC lead-on detection on the BIP and BIN inputs. ULP mode only functions when BioZ is not enabled (BIOZ_EN = 0x0).

EN_BIOZ_LON	DECODE
0	ULP lead-on detection is disabled
1	ULP lead-on detection is enabled

EN_BIOZ_LOFF

EN_BIOZ_LOFF enables DC lead-off detection on the BIP and BIN inputs, and only functions when BioZ is enabled (BIOZ_EN = 0x1 or 0x2). When enabled, the lead-off status is reported by the BIOZ_LOFF_PH, BIOZ_LOFF_PL, BIOZ_LOFF_NH, and BIOZ_LOFF_NL status bits and interrupts.

EN_BIOZ_LOFF	DECODE
0	BioZ DC lead-off detection is disabled.
1	BioZ DC lead-off detection is enabled.

EN_EXT_BIOZ_LOFF

EN_EXT_BIOZ_LOFF enables DC lead-off detection on the BIOZ_EL2B and BIOZ_EL3B pins when the BIOZ_EL2A and BIOZ_EL3A pins are being used as AC-coupled BioZ inputs. BIOZ_EL2B and BIOZ_EL3B must be connected externally to the electrode side of the AC-coupling capacitors for this feature to function.

EN_EXT_BIOZ_LOFF	DECODE
0	DC lead-off detection is applied to the internal BIP and BIN nodes.
1	DC lead-off detection is applied externally through BIOZ_EL2B and BIOZ_EL3B for AC-coupled applications.

EN_BIOZ_DRV_OOR

EN_BIOZ_DRV_OOR enables the voltage monitor on DRVN to detect the drive electrode lead-off conditions. If the total impedance between DRVP and DRVN is high, due to either the DRVP or DRVN electrode being disconnected, the AC voltage at DRVN is large and trigger a BIOZ_DRV_OOR status and interrupt.

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EN_BIOZ_DRV_OOR	DECODE
0	Drive voltage out-of-range detection is disabled.
1	Drive voltage out-of-range detection is enabled.

BIOZ_LOFF_IPOL

BIOZ_LOFF_IPOL sets the polarity of the matched DC current sources used for DC lead-off detection.

BIOZ_LOFF_IPOL	LEAD-OFF CURRENT POLARITY
0	Non-inverted. BIP sources current; BIN sinks current.
1	Inverted. BIP sinks current; BIN sources current.

BIOZ_LOFF_IMAG

BIOZ_LOFF_IMAG selects the DC lead-off current magnitude.

BIOZ_LOFF_IMAG[2:0]	DC CURRENT MAGNITUDE (nA)
0x0	0 (current sources disabled)
0x1	5
0x2	10
0x3	20
0x4	50
0x5	100
0x6	100
0x7	100

BIOZ Lead-Off Threshold (0xB1)

BIT	7	6	5	4	3	2	1	0
Field	RESP(CG) MAG_4X		RESP(CG) MAG[2:0]		BIOZ_LOFF_THRESH[3:0]			
Reset	0		0x0		0x0			
Access Type	Write, Read		Write, Read		Write, Read			

RESP(CG) MAG_4X

RESP(CG)
MAG_4X selects the amplitude of the respiration current along with RESP(CG)
MAG.

RESP(CG) MAG_4X	DECODE
0	RESP(CG) MAG current multiplied by 1x
1	RESP(CG) MAG current multiplied by 4x

RESP(CG) MAG

RESP(CG)
MAG together with RESP(CG)
MAG_4X selects the amplitude of the respiration drive current.

CG_MAG[2:0]	OUTPUT CURRENT WITH RESP(CG) MAG_4X = 0 (μ A _{PK})	OUTPUT CURRENT WITH RESP(CG) MAG_4X = 1 (μ A _{PK})
0x0	0	0
0x1	8	32
0x2	16	64
0x3	32	128

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CG_MAG[2:0]	OUTPUT CURRENT WITH RESP(CG_MAG_4X = 0) (μ A _{PK})	OUTPUT CURRENT WITH RESP(CG_MAG_4X = 1) (μ A _{PK})
0x4	48	192
0x5	64	256
0x6	80	320
0x7	96	384

BIOZ_LOFF_THRESH

BIOZ_LOFF_THRESH selects the voltage threshold for the DC lead-off window comparators, which are centered at V_{MID_RX}. If the voltage of either BIP or BIN goes above the high threshold or below the low threshold for approximately 128ms, the corresponding BIOZ_LOFF status bit is set to 1 in register 0x04.

BIOZ_LOFF_THRESH[3:0]	BIOZ DC LEAD-OFF THRESHOLD
0x0	V _{MID_RX} ±200mV
0x1	V _{MID_RX} ±225mV
0x2	V _{MID_RX} ±250mV
...	...
0xE	V _{MID_RX} ±550mV
0xF	V _{MID_RX} ±575mV

BIOZ Lead Bias Configuration 1 (0xB4)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	-	BIOZ_RBIAS_VALUE[1:0]		EN_BIOZ_RBIASP	EN_BIOZ_RBIASN
Reset	-	-	-	-		0x0	0	0
Access Type	-	-	-	-		Write, Read	Write, Read	Write, Read

BIOZ_RBIAS_VALUE

BIOZ_RBIAS_VALUE selects the BioZ input lead bias resistance, which is between BIP and V_{MID_RX} (EN_BIOZ_RBIASP = 1), and BIN and V_{MID_RX} (EN_BIOZ_RBIASN = 1).

BIOZ_RBIAS_VALUE[1:0]	BIAS RESISTANCE (MΩ)
0x0	50
0x1	100
0x2	200
0x3	Do not use

EN_BIOZ_RBIASP

EN_BIOZ_RBIASP enables the BioZ lead bias on BIP. The resistor connecting BIP to V_{MID_RX} is selected in BIOZ_RBIAS_VALUE.

EN_BIOZ_RBIASP	DECODE
0	BIP is not resistively connected to V _{MID_RX} .
1	BIP is connected to V _{MID_RX} using a resistor (selected by BIOZ_RBIAS_VALUE).

EN_BIOZ_RBIASN

EN_BIOZ_RBIASN enables BioZ lead bias on BIN. The resistor connecting BIN to V_{MID_RX} is selected in

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BIOZ_RBIAS_VALUE.

EN_BIOZ_RBIASN		DECODE
0		BIN is not resistively connected to V _{MID_RX} .
1		BIN is connected to V _{MID_RX} using a resistor (selected by BIOZ_RBIAS_VALUE).

Respiration Configuration 1 (0xB6)

BIT	7	6	5	4	3	2	1	0
Field	CG_LPF_DUTY[2:0]			CG_CHOP_CLK[1:0]			CG_MODE[1:0]	
Reset	0x0			0x0			0x0	
Access Type	Write, Read			Write, Read			Write, Read	

CG_LPF_DUTY

CG_LPF_DUTY sets the duty cycle of the respiration current generator common-mode feedback low-pass filter. Doubling the duty cycle doubles the common-mode-feedback bandwidth. Higher bandwidths result in faster current source settling, while lower bandwidths maintain higher current source output impedance.

CG_LPF_DUTY[2:0]	TIME HIGH (BIOZ_SYNTH_CLK CYCLES)	APPROXIMATE BANDWIDTH (Hz)
0x0	1	0.98
0x1	2	1.95
0x2	4	3.90
0x3	8	7.79
0x4	16	15.54
0x5	32	30.89
0x6	64	61.08
0x7	Always On	N/A

CG_CHOP_CLK

CG_CHOP_CLK selects the respiration current source chopping clock divider ratio from BIOZ_SYNTH_CLK. The respiration current generators are chopped at a frequency of BIOZ_SYNTH_CLK / CG_CHOP_CLK.

CG_CHOP_CLK[1:0]	DIVIDER RATIO
0x0	256
0x1	512
0x2	1024
0x3	2048

CG_MODE

CG_MODE selects a current source dynamic matching and common-mode feedback scheme for the respiration-current generators. These schemes can help mitigate flicker noise in the respiration current generators.

CG_MODE[1:0]	CURRENT SOURCE ROTATION SCHEME
0x0	Dynamic matching disabled with analog low-pass filter
0x1	Dynamic matching enabled without analog low-pass filter
0x2	Dynamic matching enabled with analog low-pass filter
0x3	Dynamic matching enabled with internal resistive-common mode load

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RESP_EN

When the BioZ channel is enabled, RESP_EN switches the stimulus source from the transmit channel to the balanced respiration current generators. BIOZ_BG_EN must be set to 1 and BIOZ_EN must be set to 0x1 or 0x2.

RESP_EN	DECODE
0	Respiration mode is disabled, and the BioZ transmit channel is used.
1	Respiration mode is enabled, and the balanced respiration current generators are used in place of the BioZ transmit channel.

Interrupt1 Enable 1 (0xC0)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL_E_N1	PPG_FRAM_E_RDY_EN1	FIFO_DATA_RDY_EN1	ALC_OVF_EN1	EXP_OVF_EN1	PPG_THRE_SH2_HILO_EN1	PPG_THRE_SH1_HILO_EN1	-
Reset	0	0	0	0	0	0	0	-
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	-

A_FULL_EN1

Enables the A_FULL[7](0x00) status bit to trigger the INT1 output pin.

A_FULL_EN1	Decode
0	The A_FULL status bit does not impact the INT1 output pin.
1	INT1 is triggered when A_FULL is set to 1

PPG_FRAME_RDY_EN1

Enables the FRAME_RDY[6](0x00) status bit to trigger the INT1 output pin.

PPG_FRAME_RDY_EN1	Decode
0	The FRAME_RDY status bit does not impact the INT1 output pin.
1	INT1 is triggered when FRAME_RDY is set to 1.

FIFO_DATA_RDY_EN1

Enables the FIFO_DATA_RDY[5](0x00) status bit to trigger the INT1 output pin.

FIFO_DATA_RDY_EN1	Decode
0	The FIFO_DATA_RDY status bit does not impact the INT1 output pin.
1	INT1 is triggered when FIFO_DATA_RDY is set to 1.

ALC_OVF_EN1

Enables the ALC_OVF[4](0x00) status bit to trigger the INT1 output pin.

ALC_OVF_EN1	Decode
0	The ALC_OVF status bit does not impact the INT1 output pin.
1	INT1 is triggered when ALC_OVF is set to 1.

EXP_OVF_EN1

Enables the EXP_OVF[3](0x00) status bit to trigger the INT1 output pin.

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EXP_OVF_EN1		Decode
0	The EXP_OVF status bit does not impact the INT1 output pin.	
1	INT1 is triggered when EXP_OVF is set to 1.	

PPG_THRESH2_HILO_EN1

Enables the PPG_THRESH2_HILO[2](0x00) status bit to trigger the INT1 output pin.

PPG_THRESH2_HILO_EN1		Decode
0	The PPG_THRESH2_HILO status bit does not impact the INT1 output pin.	
1	INT1 is triggered when PPG_THRESH2_HILO is set to 1.	

PPG_THRESH1_HILO_EN1

Enables the PPG_THRESH1_HILO[1](0x00) status bit to trigger the INT1 output pin.

PPG_THRESH1_HILO_EN1		Decode
0	The PPG_THRESH1_HILO status bit does not impact the INT1 output pin.	
1	INT1 is triggered when PPG_THRESH1_HILO is set to 1.	

Interrupt1 Enable 2 (0xC1)

BIT	7	6	5	4	3	2	1	0
Field	INVALID_P PG_CFG_E N1	-	LED6_COM PB_EN1	LED5_COM PB_EN1	LED4_COM PB_EN1	LED3_COM PB_EN1	LED2_COM PB_EN1	LED1_COM PB_EN1
Reset	0	-	0	0	0	0	0	0
Access Type	Write, Read	-	Write, Read					

INVALID_PPG_CFG_EN1

Enables the INVALID_PPG_CFG[7](0x01) status bit to trigger the INT1 output pin.

INVALID_PPG_CFG_EN1		Decode
0	The INVALID_PPG_CFG status bit does not impact the INT1 output pin.	
1	INT1 is triggered when INVALID_PPG_CFG is set to 1.	

LED6_COMPB_EN1

Enables the LED6_COMPB[5](0x01) status bit to trigger the INT1 output pin.

LED6_COMPB_EN1		Decode
0	The LED6_COMPB status bit does not impact the INT1 output pin.	
1	INT1 is triggered when LED6_COMPB is set to 1.	

LED5_COMPB_EN1

Enables the LED5_COMPB[4](0x01) status bit to trigger the INT1 output pin.

LED5_COMPB_EN1		Decode
0	The LED5_COMPB status bit does not impact the INT1 output pin.	
1	INT1 is triggered when LED5_COMPB is set to 1.	

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LED4_COMPB_EN1

Enables the LED4_COMPB[3](0x01) status bit to trigger the INT1 output pin.

Decode	
0	The LED4_COMPB status bit does not impact the INT1 output pin.
1	INT1 is triggered when LED4_COMPB is set to 1.

LED3_COMPB_EN1

Enables the LED3_COMPB[2](0x01) status bit to trigger the INT1 output pin.

Decode	
0	The LED3_COMPB status bit does not impact the INT1 output pin.
1	INT1 is triggered when LED3_COMPB is set to 1.

LED2_COMPB_EN1

Enables the LED2_COMPB[1](0x01) status bit to trigger the INT1 output pin.

Decode	
0	The LED2_COMPB status bit does not impact the INT1 output pin.
1	INT1 is triggered when LED2_COMPB is set to 1.

LED1_COMPB_EN1

Enables the LED1_COMPB[0](0x01) status bit to trigger the INT1 output pin.

Decode	
0	The LED1_COMPB status bit does not impact the INT1 output pin.
1	INT1 is triggered when LED1_COMPB is set to 1.

Interrupt1 Enable 3 (0xC2)

BIT	7	6	5	4	3	2	1	0
Field	-	-	-	FREQ_UNL_OCK_EN1	FREQ_LOC_K_EN1	PHASE_UN_LOCK_EN1	PHASE_LO_CK_EN1	-
Reset	-	-	-			0	0	-
Access Type	-	-	-	Write, Read	Write, Read	Write, Read	Write, Read	-

FREQ_UNLOCK_EN1

Enables the FREQ_UNLOCK[4](0x02) status bit to trigger the INT1 output pin.

Decode	
0	The FREQ_UNLOCK status bit does not impact the INT1 output pin.
1	INT1 is triggered when FREQ_UNLOCK is set to 1.

FREQ_LOCK_EN1

Enables the FREQ_LOCK[3](0x02) status bit to trigger the INT1 output pin.

Decode	
0	The FREQ_LOCK status bit does not impact the INT1 output pin.
1	INT1 is triggered when FREQ_LOCK is set to 1.

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Enables PHASE_UNLOCK[2](0x02) to trigger the INT1 output pin. This interrupt is only asserted if PLL_EN[0](0x18) is set to 1.

PHASE_UNLOCK_EN1	Decode
0	The PHASE_UNLOCK status bit does not impact the INT1 output pin.
1	INT1 is triggered when PHASE_UNLOCK is set to 1.

PHASE_LOCK_EN1

Enables the PHASE_LOCK[1](0x02) status bit to trigger the INT1 output pin.

PHASE_LOCK_EN1	Decode
0	The PHASE_LOCK status bit does not impact the INT1 output pin.
1	INT1 is triggered when PHASE_LOCK is set to 1.

Interrupt1 Enable 4 (0xC3)

BIT	7	6	5	4	3	2	1	0
Field	ECG_LON_EN1	–	ECG_FAST_REC_EN1	RLD_OOR_EN1	ECG_LOFF_PH_EN1	ECG_LOFF_PL_EN1	ECG_LOFF_NH_EN1	ECG_LOFF_NL_EN1
Reset	0	–	0	0	0	0	0	0
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

ECG_LON_EN1

Enables ECG_LON[7](0x03) to trigger the INT1 output pin.

ECG_LON_EN1	Decode
0	The ECG_LON status bit does not impact the INT1 output pin.
1	INT1 is triggered when ECG_LON is set to 1.

ECG_FAST_REC_EN1

Enables the ECG_FAST_REC[5](0x03) status bit to trigger the INT1 output pin.

ECG_FAST_REC_EN1	Decode
0	The ECG_FAST_REC status bit does not impact the INT1 output pin.
1	INT1 is triggered when ECG_FAST_REC is set to 1.

RLD_OOR_EN1

Enables the RLD_OOR[4](0x03) status bit to trigger the INT1 output pin.

RLD_OOR_EN1	Decode
0	The RLD_OOR status bit does not impact the INT1 output pin.
1	INT1 is triggered when RLD_OOR is set to 1.

ECG_LOFF_PH_EN1

Enables the ECG_LOFF_PH[3](0x03) status bit to trigger the INT1 output pin.

ECG_LOFF_PH_EN1	Decode
0	The ECG_LOFF_PH status bit does not impact the INT1 output pin.
1	INT1 is triggered when ECG_LOFF_PH is set to 1.

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Enables the ECG_LOFF_PL[2](0x03) status bit to trigger the INT1 output pin.

ECG_LOFF_PL_EN1		Decode
0	The ECG_LOFF_PL status bit does not impact the INT1 output pin.	
1	INT1 is triggered when ECG_LOFF_PL is set to 1.	

ECG_LOFF_NH_EN1

Enables the ECG_LOFF_NH[1](0x03) status bit to trigger the INT1 output pin.

ECG_LOFF_NH_EN1		Decode
0	The ECG_LOFF_NH status bit does not impact the INT1 output pin.	
1	INT1 is triggered when ECG_LOFF_NH is set to 1.	

ECG_LOFF_NL_EN1

Enables the ECG_LOFF_NL[0](0x03) status bit to trigger the INT1 output pin.

ECG_LOFF_NL_EN1		Decode
0	The ECG_LOFF_NL status bit does not impact the INT1 output pin.	
1	INT1 is triggered when ECG_LOFF_NL is set to 1.	

Interrupt1 Enable 5 (0xC4)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_LON_EN1	BIOZ_OVE_R_EN1	BIOZ_UND_R_EN1	BIOZ_DRV_P_OFF_EN1	BIOZ_LOFF_PH_EN1	BIOZ_LOFF_PL_EN1	BIOZ_LOFF_NH_EN1	BIOZ_LOFF_NL_EN1
Reset	0	0	0	0b0	0	0	0	0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BIOZ_LON_EN1

Enables the BIOZ_LON[7](0x04) status bit to trigger the INT1 output pin.

BIOZ_LON_EN1		Decode
0	The BIOZ_LON status bit does not impact the INT1 output pin.	
1	INT1 is triggered when BIOZ_LON is set to 1.	

BIOZ_OVER_EN1

Enables the BIOZ_OVER[6](0x04) status bit to trigger the INT1 output pin.

BIOZ_OVER_EN1		Decode
0	The BIOZ_OVER status bit does not impact the INT1 output pin.	
1	INT1 is triggered when BIOZ_OVER is set to 1.	

BIOZ_UNDR_EN1

Enables the BIOZ_UNDR[5](0x04) status bit to trigger the INT1 output pin.

BIOZ_UNDR_EN1		Decode
0	The BIOZ_UNDR status bit does not impact the INT1 output pin.	
1	INT1 is triggered when BIOZ_UNDR is set to 1.	

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BIOZ_DRVP_OFF_EN1

Enables RLD_OOR[3](0x04) to trigger the INT1 output pin.

Value	Decode
0	RLD_OOR does not impact the INT1 output pin.
1	INT1 is triggered when RLD_OOR is set to 1.

BIOZ_LOFF_PH_EN1

Enables the BIOZ_LOFF_PH[3](0x04) status bit to trigger the INT1 output pin.

BIOZ_LOFF_PH_EN1	Decode
0	The BIOZ_LOFF_PH status bit does not impact the INT1 output pin.
1	INT1 is triggered when BIOZ_LOFF_PH is set to 1.

BIOZ_LOFF_PL_EN1

Enables BIOZ_LOFF_PL[3](0x04) to trigger the INT1 output pin.

BIOZ_LOFF_PL_EN1	Decode
0	The BIOZ_LOFF_PL status bit does not impact the INT1 output pin.
1	INT1 is triggered when BIOZ_LOFF_PL is set to 1.

BIOZ_LOFF_NH_EN1

Enables the BIOZ_LOFF_NH[1](0x04) status bit to trigger the INT1 output pin.

BIOZ_LOFF_NH_EN1	Decode
0	The BIOZ_LOFF_NH status bit does not impact the INT1 output pin.
1	INT1 is triggered when BIOZ_LOFF_NH is set to 1.

BIOZ_LOFF_NL_EN1

Enables the BIOZ_LOFF_NL[0](0x04) status bit to trigger the INT1 output pin.

BIOZ_LOFF_NL_EN1	Decode
0	The BIOZ_LOFF_NL status bit does not impact the INT1 output pin.
1	INT1 is triggered when BIOZ_LOFF_NL is set to 1.

Interrupt2 Enable 1 (0xC5)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL_E_N2	PPG_FRAM_E_RDY_EN2	FIFO_DATA_RDY_EN2	ALC_OVF_EN2	EXP_OVF_EN2	PPG_THRE_SH2_HILO_EN2	PPG_THRE_SH1_HILO_EN2	-
Reset	0	0	0	0	0	0	0	-
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	-

A_FULL_EN2

Enables the A_FULL[7](0x00) status bit to trigger the INT2 output pin.

A_FULL_EN2	Decode
0	The A_FULL status bit does not impact the INT2 output pin.
1	INT2 is triggered when A_FULL is set to 1

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PPG_FRAME_RDY_EN2

Enables the FRAME_RDY[6](0x00) status bit to trigger the INT2 output pin.

Decode	
0	The FRAME_RDY status bit does not impact the INT2 output pin.
1	INT2 is triggered when FRAME_RDY is set to 1.

FIFO_DATA_RDY_EN2

Enables the FIFO_DATA_RDY[5](0x00) status bit to trigger the INT2 output pin.

Decode	
0	The FIFO_DATA_RDY status bit does not impact the INT2 output pin.
1	INT2 is triggered when FIFO_DATA_RDY is set to 1.

ALC_OVF_EN2

Enables the ALC_OVF[4](0x00) status bit to trigger the INT2 output pin.

Decode	
0	The ALC_OVF status bit does not impact the INT2 output pin.
1	INT2 is triggered when ALC_OVF is set to 1.

EXP_OVF_EN2

Enables the EXP_OVF[3](0x00) status bit to trigger the INT2 output pin.

Decode	
0	EXP_OVF does not impact the INT2 output pin.
1	INT2 is triggered when EXP_OVF is set to 1.

PPG_THRESH2_HILO_EN2

Enables the PPG_THRESH2_HILO[2](0x00) status bit to trigger the INT2 output pin.

Decode	
0	The PPG_THRESH2_HILO status bit does not impact the INT2 output pin.
1	INT2 is triggered when PPG_THRESH2_HILO is set to 1.

PPG_THRESH1_HILO_EN2

Enables the PPG_THRESH1_HILO[1](0x00) status bit to trigger the INT2 output pin.

Decode	
0	The PPG_THRESH1_HILO status bit does not impact the INT2 output pin.
1	INT2 is triggered when PPG_THRESH1_HILO is set to 1.

Interrupt2 Enable 2 (0xC6)

BIT	7	6	5	4	3	2	1	0
Field	INVALID_P PG_CFG_E N2	–	LED6_COM PB_EN2	LED5_COM PB_EN2	LED4_COM PB_EN2	LED3_COM PB_EN2	LED2_COM PB_EN2	LED1_COM PB_EN2
Reset	0	–	0	0	0	0	0	0
Access Type	Write, Read	–	Write, Read					

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Enables the INVALID_PPG_CFG[7](0x01) status bit to trigger the INT2 output pin.

INVALID_PPG_CFG_EN2	Decode
0	The INVALID_PPG_CFG status bit does not impact the INT2 output pin.
1	INT2 is triggered when INVALID_PPG_CFG is set to 1.

LED6_COMPB_EN2

Enables the LED6_COMPB[5](0x01) status bit to trigger the INT2 output pin.

LED6_COMPB_EN2	Decode
0	The LED6_COMPB status bit does not impact the INT2 output pin.
1	INT2 is triggered when LED6_COMPB is set to 1.

LED5_COMPB_EN2

Enables the LED5_COMPB[4](0x01) status bit to trigger the INT2 output pin.

LED5_COMPB_EN2	Decode
0	The LED5_COMPB status bit does not impact the INT2 output pin.
1	INT2 is triggered when LED5_COMPB is set to 1.

LED4_COMPB_EN2

Enables the LED4_COMPB[3](0x01) status bit to trigger the INT2 output pin.

LED4_COMPB_EN2	Decode
0	The LED4_COMPB status bit does not impact the INT2 output pin.
1	INT2 is triggered when LED4_COMPB is set to 1.

LED3_COMPB_EN2

Enables the LED3_COMPB[2](0x01) status bit to trigger the INT2 output pin.

LED3_COMPB_EN2	Decode
0	The LED3_COMPB status bit does not impact the INT2 output pin.
1	INT2 is triggered when LED3_COMPB is set to 1.

LED2_COMPB_EN2

Enables the LED2_COMPB[1](0x01) status bit to trigger the INT2 output pin.

LED2_COMPB_EN2	Decode
0	The LED2_COMPB status bit does not impact the INT2 output pin.
1	INT2 is triggered when LED2_COMPB is set to 1.

LED1_COMPB_EN2

Enables the LED1_COMPB[0](0x01) status bit to trigger the INT2 output pin.

LED1_COMPB_EN2	Decode
0	The LED1_COMPB status bit does not impact the INT2 output pin.
1	INT2 is triggered when LED1_COMPB is set to 1.

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Interrupt2 Enable 3 (0xC7)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FREQ_UNL OCK_EN2	FREQ_LOC K_EN2	PHASE_UN LOCK_EN2	PHASE_LO CK_EN2	–
Reset	–	–	–			0	0	–
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	–

FREQ_UNLOCK_EN2

Enables the FREQ_UNLOCK[4](0x02) status bit to trigger the INT2 output pin.

FREQ_UNLOCK_EN2	Decode
0	The FREQ_UNLOCK status bit does not impact the INT2 output pin.
1	INT2 is triggered when FREQ_UNLOCK is set to 1.

FREQ_LOCK_EN2

Enables the FREQ_LOCK[3](0x02) status bit to trigger the INT2 output pin.

FREQ_LOCK_EN2	Decode
0	The FREQ_LOCK status bit does not impact the INT2 output pin.
1	INT2 is triggered when FREQ_LOCK is set to 1.

PHASE_UNLOCK_EN2

Enables the PHASE_UNLOCK[2](0x02) status bit to trigger the INT2 output pin. This interrupt is only asserted if PLL_EN[0](0x18) is set to 1.

PHASE_UNLOCK_EN2	Decode
0	The PHASE_UNLOCK status bit does not impact the INT2 output pin.
1	INT2 is triggered when PHASE_UNLOCK is set to 1.

PHASE_LOCK_EN2

Enables the PHASE_LOCK[1](0x02) status bit to trigger the INT2 output pin.

PHASE_LOCK_EN2	Decode
0	The PHASE_LOCK status bit does not impact the INT2 output pin.
1	INT2 is triggered when PHASE_LOCK is set to 1.

Interrupt2 Enable 4 (0xC8)

BIT	7	6	5	4	3	2	1	0
Field	ECG_LON_EN2	–	ECG_FAST_REC_EN2	RLD_OOR_EN2	ECG_LOFF_PH_EN2	ECG_LOFF_PL_EN2	ECG_LOFF_NH_EN2	ECG_LOFF_NL_EN2
Reset	0	–	0	0	0	0	0	0
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

ECG_LON_EN2

Enables ECG_LON[7](0x05) to trigger the INT2 output pin.

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ECG_LON_EN2	Decode
0	The ECG_LON status bit does not impact the INT2 output pin.
1	INT2 is triggered when ECG_LON is set to 1.

ECG_FAST_REC_EN2

Enables the ECG_FAST_REC[5](0x03) status bit to trigger the INT2 output pin.

ECG_FAST_REC_EN2	Decode
0	The ECG_FAST_REC status bit does not impact the INT2 output pin.
1	INT2 is triggered when ECG_FAST_REC is set to 1.

RLD_OOR_EN2

Enables the RLD_OOR[4](0x03) status bit to trigger the INT2 output pin.

RLD_OOR_EN2	Decode
0	The RLD_OOR status bit does not impact the INT2 output pin.
1	INT2 is triggered when RLD_OOR is set to 1.

ECG_LOFF_PH_EN2

Enables ECG_LOFF_PH[3](0x03) to trigger the INT2 output pin.

ECG_LOFF_PH_EN2	Decode
0	The ECG_LOFF_PH status bit does not impact the INT2 output pin.
1	INT2 is triggered when ECG_LOFF_PH is set to 1.

ECG_LOFF_PL_EN2

Enables ECG_LOFF_PL[2](0x03) to trigger the INT2 output pin.

ECG_LOFF_PL_EN2	Decode
0	The ECG_LOFF_PL status bit does not impact the INT2 output pin.
1	INT2 is triggered when ECG_LOFF_PL is set to 1.

ECG_LOFF_NH_EN2

Enables the ECG_LOFF_NH[1](0x03) status bit to trigger the INT2 output pin.

ECG_LOFF_NH_EN2	Decode
0	The ECG_LOFF_NH status bit does not impact the INT2 output pin.
1	INT2 is triggered when ECG_LOFF_NH is set to 1.

ECG_LOFF_NL_EN2

Enables the ECG_LOFF_NL[0](0x03) status bit to trigger the INT2 output pin.

ECG_LOFF_NL_EN2	Decode
0	The ECG_LOFF_NL status bit does not impact the INT2 output pin.
1	INT2 is triggered when ECG_LOFF_NL is set to 1.

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Interrupt2 Enable 5 (0xC9)

BIT	7	6	5	4	3	2	1	0
Field	BIOZ_LON_EN2	BIOZ_OVE_R_EN2	BIOZ_UND_R_EN2	BIOZ_DRV_P_OFF_EN2	BIOZ_LOFF_PH_EN2	BIOZ_LOFF_PL_EN2	BIOZ_LOFF_NH_EN2	BIOZ_LOFF_NL_EN2
Reset	0	0	0	0b0	0	0	0	0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BIOZ_LON_EN2

Enables the BIOZ_LON[7](0x04) status bit to trigger the INT2 output pin.

BIOZ_LON_EN2	Decode
0	The BIOZ_LON status bit does not impact the INT2 output pin.
1	INT2 is triggered when BIOZ_LON is set to 1.

BIOZ_OVER_EN2

Enables the BIOZ_OVER[6](0x04) status bit to trigger the INT2 output pin.

BIOZ_OVER_EN2	Decode
0	The BIOZ_OVER status bit does not impact the INT2 output pin.
1	INT2 is triggered when BIOZ_OVER is set to 1.

BIOZ_UNDR_EN2

Enables the BIOZ_UNDR[5](0x04) status bit to trigger the INT2 output pin.

BIOZ_UNDR_EN2	Decode
0	The BIOZ_UNDR status bit does not impact the INT2 output pin.
1	INT2 is triggered when BIOZ_UNDR is set to 1.

BIOZ_DRVP_OFF_EN2

Enables DRVN_OOR [4](0x04) to trigger the INT2 output pin.

Value	Decode
0	The DRVP_OOR does not impact the INT2 output pin.
1	INT2 is triggered when DRVN_OOR is set to 1.

BIOZ_LOFF_PH_EN2

Enables the BIOZ_LOFF_PH[3](0x05) status bit to trigger the INT2 output pin.

BIOZ_LOFF_PH_EN2	Decode
0	The BIOZ_LOFF_PH status bit does not impact the INT2 output pin.
1	INT2 is triggered when BIOZ_LOFF_PH is set to 1.

BIOZ_LOFF_PL_EN2

Enables the BIOZ_LOFF_PL[2](0x04) status bit to trigger the INT2 output pin.

BIOZ_LOFF_PL_EN2	Decode
0	The BIOZ_LOFF_PL status bit does not impact the INT2 output pin.
1	INT2 is triggered when BIOZ_LOFF_PL is set to 1.

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BIOZ_LOFF_NH_EN2

Enables the BIOZ_LOFF_NH[1](0x04) status bit to trigger the INT2 output pin.

BIOZ_LOFF_NH_EN2		Decode
0		The BIOZ_LOFF_NH status bit does not impact the INT2 output pin.
1		INT2 is triggered when BIOZ_LOFF_NH is set to 1.

BIOZ_LOFF_NL_EN2

Enables the BIOZ_LOFF_NL[0](0x04) status bit to trigger the INT2 output pin.

BIOZ_LOFF_NL_EN2		Decode
0		The BIOZ_LOFF_NL status bit does not impact the INT2 output pin.
1		INT2 is triggered when BIOZ_LOFF_NL is set to 1.

Part ID (0xFF)

BIT	7	6	5	4	3	2	1	0
Field	PART_ID[7:0]							
Reset	0x43							
Access Type	Read Only							

PART_ID

This register stores the Part identifier for the chip.

PART_ID[7:0]	Part Number	Description
0x43	MAX86178	ECG + BioZ + Quad PD, Dual-Channel PPG with six LED Drivers

PRELIMINARY

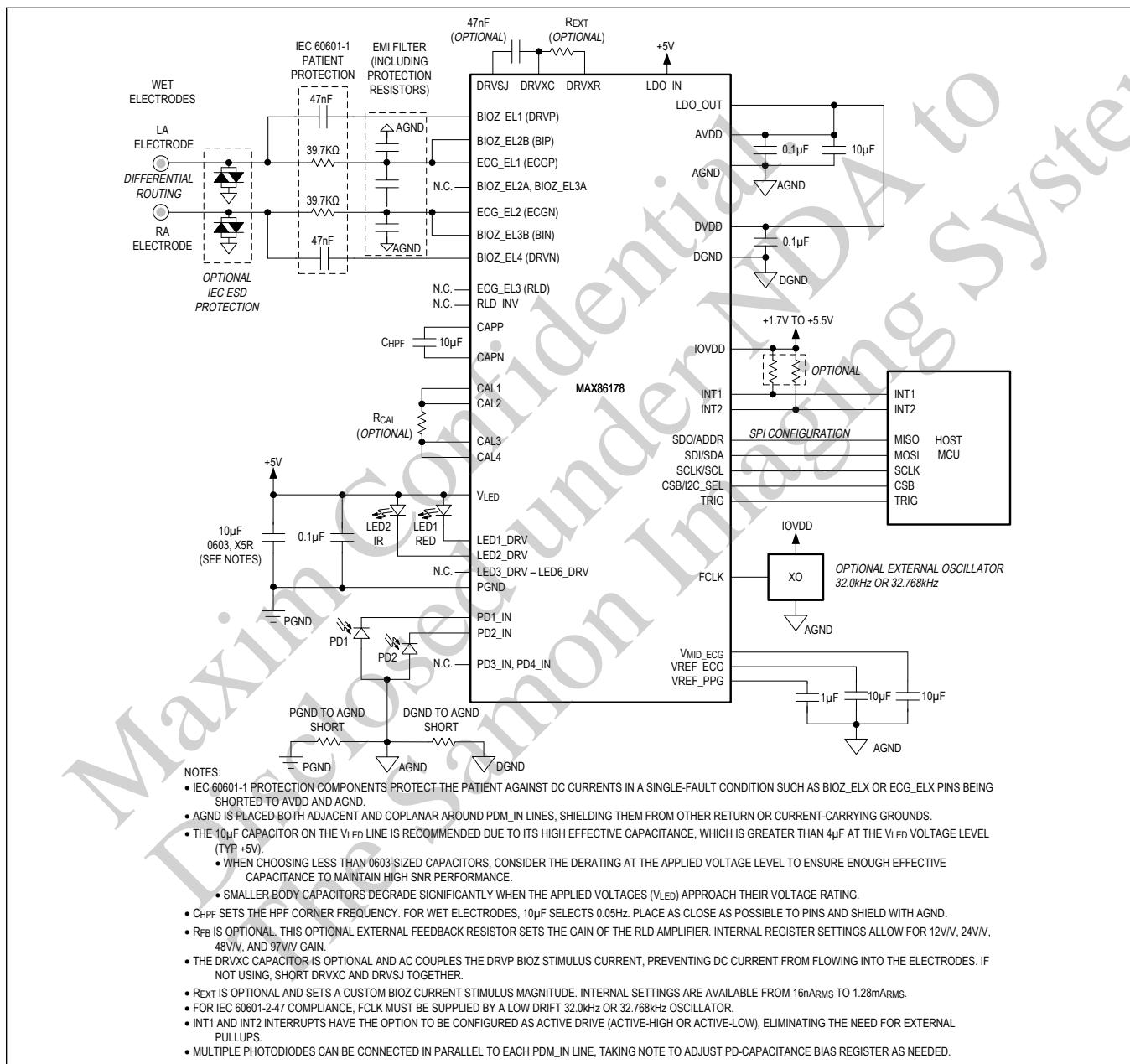
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Typical Application Circuits

Typical Application Circuit 1

Chest Patch with 2 Wet Electrodes Supporting Continuous Respiration or ICG, Intermittent BIA, Continuous ECG, and Continuous SpO₂



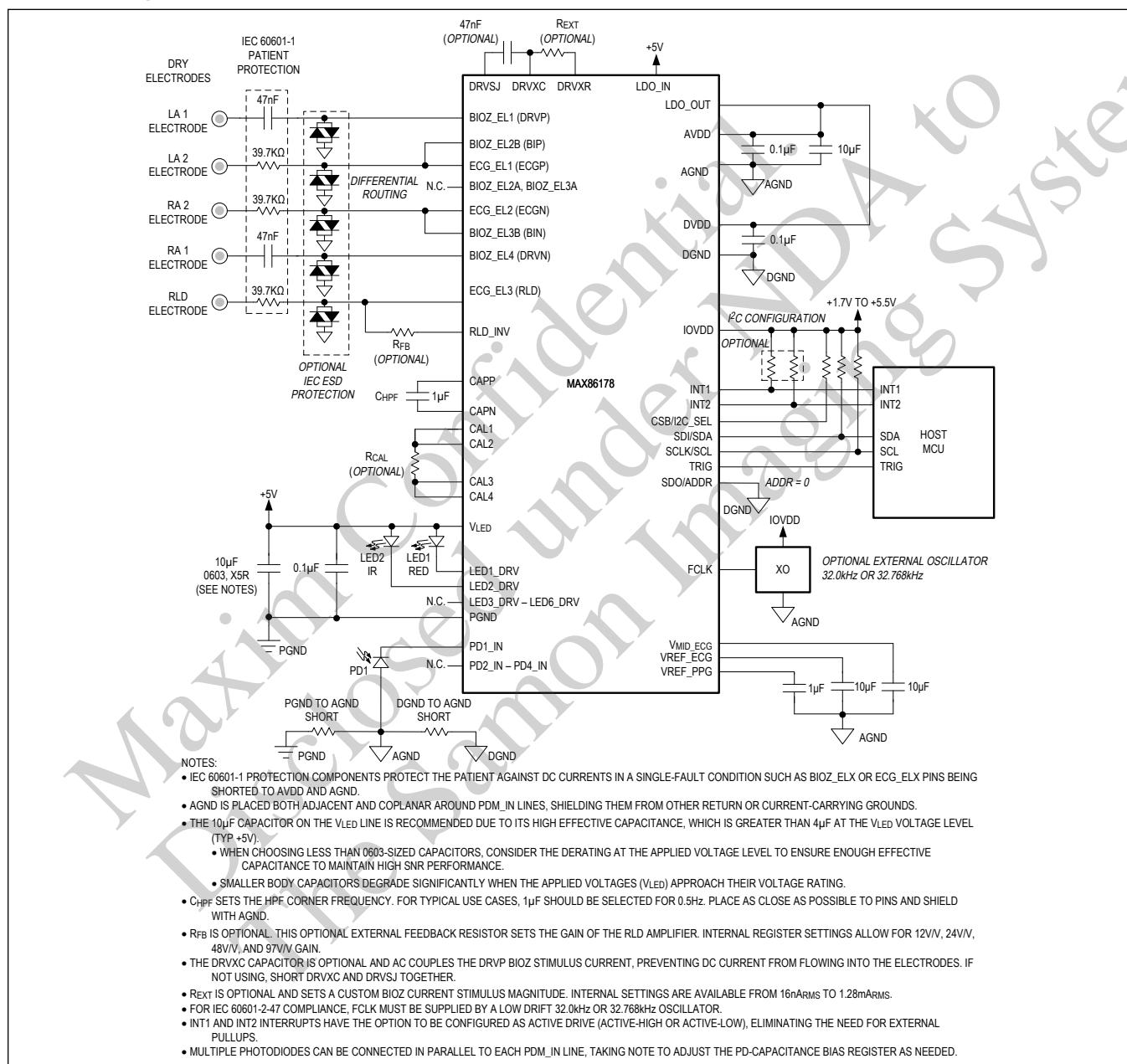
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Typical Application Circuits (continued)

Typical Application Circuit 2

Chest Strap with 5 Dry Electrodes Supporting Continuous Respiration, Intermittent BIA, Continuous ECG, and Continuous SpO₂



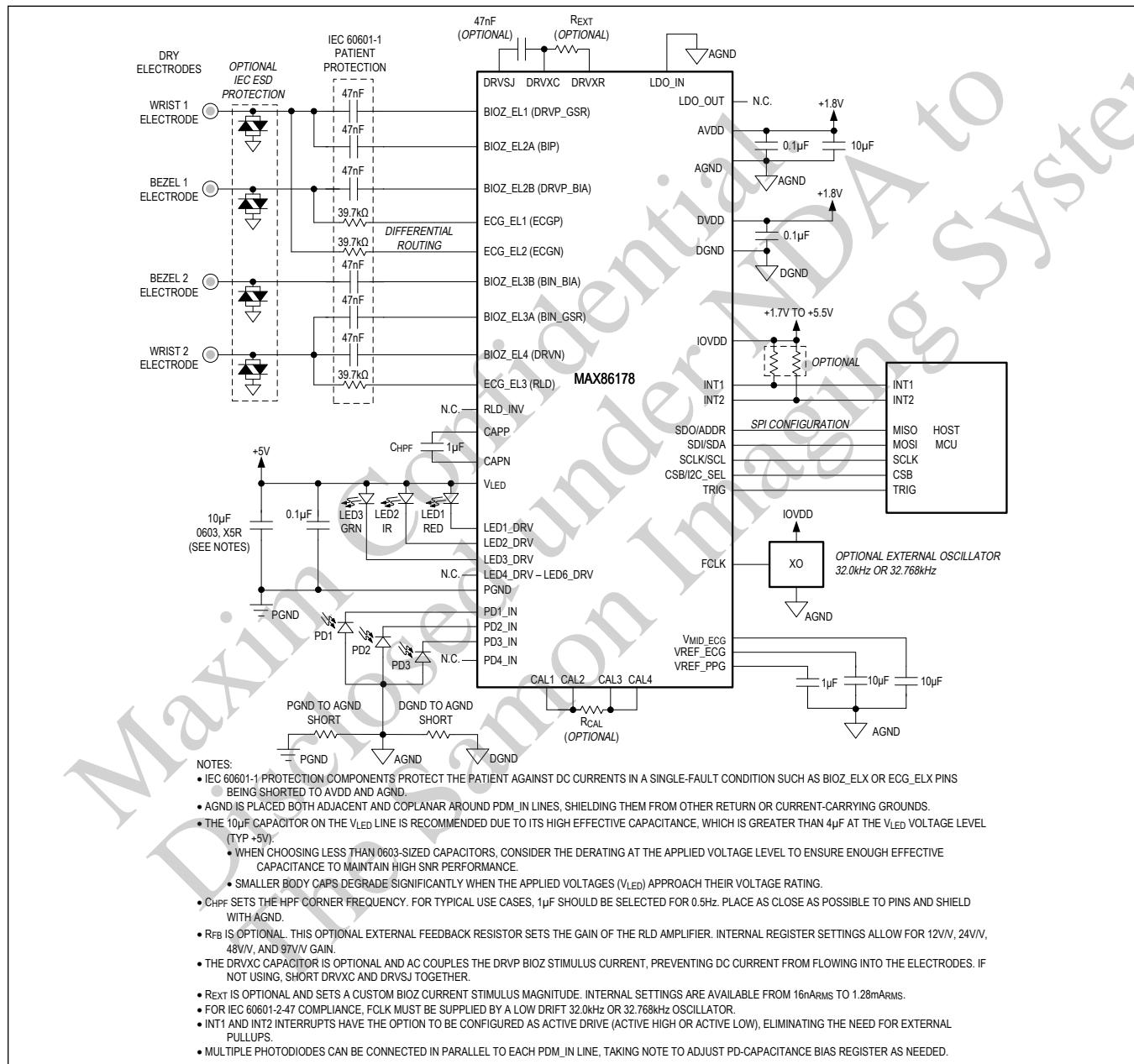
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Typical Application Circuits (continued)

Typical Application Circuit 3

Wrist Device with 4 Dry Electrodes Supporting On-Demand BIA, On-Demand ECG, Continuous HRM and SpO₂, and Continuous EDA/GSR



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Ordering Information

PART NUMBER	TEMP. RANGE	PIN-PACKAGE
MAX86178ENJ+	-40°C to +85°C	49 WLP
MAX86178ENJ+T	-40°C to +85°C	49 WLP

+Denotes lead(Pb)-free/RoHS compliance.

T = Tape-and-reel.

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/21	Release for market intro	—
1	8/21	Updated IOVDD to DGND Absolute Maximum Rating, IOVDD Supply Voltage Max in Electrical Characteristics, Timing Subsystem, ECG EMI Filtering, BioZ EMI Filtering, BIOZ_KDIV, ECG_LOFF_FREQ, BIOZ Mux Configuration 1, Typical Application Circuits	9, 41, 73, 97, 125, 143, 182, 195-196, 215-217

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For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

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