CMPEN 270 Spring 2022

Design Project #3 – 10% of Final Grade

Instructions

1. **All submitted work must be independent. All college and university guidelines regarding academic integrity will be strictly enforced.**

2. **VERIFY the contents of any submissions is included in the Gradescope course drop box. No credit will be given for blank or corrupt submissions.**

Due Friday, 4/22/2022 @11:59pm

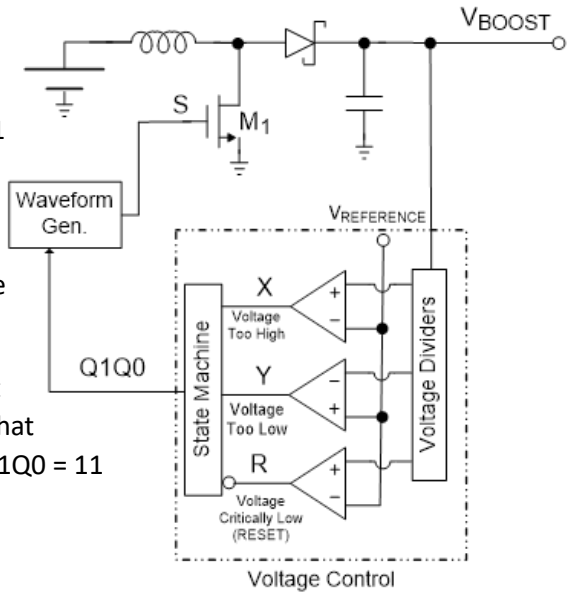
1) **Design of a switching power converter PART I.** As we've learned, digital design serves as the fundamental backbone to CPUs, software, memory, and many other modern components in digital systems. However, there are MANY other applications. For example, power electronic circuits depend on digital design for their control. A boost converter is one example, which converts lower to higher voltage. You can use these for many interesting projects converting small voltages, i.e. from wearable and implantable medical devices, or a battery or solar cell powering heavy loads like motors, etc. They are also vital in electric and hybrid cars, where its motor is running at multiple times the voltage the battery provides. But caution! Do a quick ideal power analysis $V_{out}I_{out} = V_{in}I_{in}$, and observe what happens to I_{in} as V_{in} gets very small (i.e. be careful not to burn things!!!).

What could happen to a power electronic circuit if you're not careful!!! 🔥🔥🔥
source: https://metlabs.com/wp-content/uploads/2020/05/Circuit-Board-Fire.jpg

In a boost converter, its switching control input (S) to its NMOS transistor is a square wave of variable duty cycle (d), and ideal voltage gain of 1/(1-d). This charges up an inductor d % of the time, and then dumps the charge into an output capacitor during each off cycle – the result is a boosted voltage. Note the description is a surface level analysis of this circuit which would take a long time to study! However, the explanation suffices for our application in digital design.

The following is a schematic of a DC/DC boost converter deployed in an implantable device application. It works by converting its small input voltage of 0.8 V max to ~2 V (V_{boost}) to power a wireless transmitter. Current load, losses through the NMOS, inductor, diode, as well as an unreliable input voltage all play a role in determining the duty cycle necessary to provide 2 V output. Part I of this activity is to design the voltage control which computes this value (d) based on feedback from measurement of V_{boost}. Note: d is

not to be confused with capital D, the input of a D flip flop.



a) We designate Q1Q0 to be the state variables representing the duty cycle of the square wave activating NMOS switch M1. Note that operating at 100% duty cycle would mean S = 1 constantly and short the inductor to ground, which wouldn't allow any charge transfer to V_{boost}, and will probably cook the inductor! However, zero percent is desirable because when S = 0 the system can turn off and save power when not in use.

Find all values (in *equally spaced intervals* from 0% - 75%) that can be realized with the 2-bit scheme. Record this in a table that lists the states to the corresponding duty cycle. Q1Q0 = 00, Q1Q0 = 11 have been filled out for you.

Q1Q0	Duty Cycle (d)
00	0%
01	25 %
10	50 %
11	75%

b) The voltage control block modifies the duty cycle depending on the measured V_{boost}. Let this measurement be reflected in logic signals X and Y (i.e. X = 1 means the voltage is too high, Y = 1 means the voltage is too low). An asynchronous reset signal (R) is activated when the voltage is critically low, then the system immediately selects the maximum duty cycle to increase the voltage as much as possible. Complete the blanks in the table for the correct X and Y inputs under each condition.

Input Condition	Voltage Control Inputs	Action Taken
Vboost < 1.8 V	R = 0	Increase to maximum duty cycle (asynchronous reset)
1.8 V <= Vboost < 1.9	R = 1, X = 0, Y = 1	Increase duty cycle to its next highest value
1.9 V <= Vboost < 2.1	R = 1, X = 0, Y = 0	None
Vboost > 2.1 V	R = 1, X = 1, Y = 0	Reduce duty cycle to next lowest value

c) Assume that a command to decrease d when at 0% produces a 0% next state, and increasing d past 75% results in 75% for the next state. Implement the sequential circuit that produces the correct state

variables Q1Q0. It is best to start with a state transition table. Fill out this table based on the information in part (b).

d) Draw the state machine diagram corresponding to the table from part (c)

e) Design and draw the circuit based on the information from parts (c) and (d)

f) Why was it necessary to incorporate the restrictions from part (c)? In other words, what are the practical reasons we chose to guarantee the duty cycle stays at 0% (when it's requested to reduce d) and stays at 75% (when requested to increase d)?

2) **Design of a switching power converter PART II.** Now we have the design that computes the correct duty cycle in the format Q1Q0 which represents 0% to 75%. We can set these state variables equal to d1d0 and consider them inputs to our next circuit, which generates (S) controlling the NMOS. For example, if d = 75%, then S is logic '1' 75% of the time and '0' 25% of the time. The idea behind this design is to generate a 2-bit up counter (C1C0) with output S = 1 if d1d0 > C1C0 and S = 0 if d1d2 <= C1C0.

a) Design the 2-bit counter circuit that cycles C1C0 = 00, 01, 10, 11 and loops back to 00, with inputs d1d0 and output S. Show the state transition table

b) Show the state machine diagram

c) Derive the logical functional expressions, and logic circuit

d) Draw the timing diagrams for S for both 25% and 75% duty cycles. At minimum, these should have the CLK for the 2-bit counter, C1, C0 and S.

e) Analog engineers designing the clock for the 2-bit counter determined due to constraints in their power budget, the maximum frequency of their clock will be 1 MHz because as clock frequency increases, the clock consumes more power. What would be the maximum switching frequency of the converter (signal S)? Propose a general rule for obtaining the converter's switching frequency based on: the counter's clock frequency and # of bits of the counter.

f) Designing high frequency clocks is a challenge and requires increased power consumption. Explain the design tradeoff between duty cycle precision (# of bits), and maximum clock frequency. Why would in some applications it be preferable to have less precise duty cycles?

3) Prototype your waveform generator circuit from part (2). To show a working waveform you may use any of the OUT bits on the DEB or LED to demonstrate the duty cycle (2 bits i.e. IN1 and IN0) by timing how long it is ON vs. OFF, and comparing this with your CLOCK signal. NOTE the DEB has a built-in clock which is activated by setting CLOCK_ENABLE to '1.'

Submit your answers to questions (1) and (2) and a written explanation of how you approached the design – about one page NEATLY handwritten or typed. Describe any methods used and include a schematic of the circuit design.

3) Build the waveform generator circuit from part (2) and take a video demo of your working prototype. A working demo shall be submitted via Gradescope along with your write-up. This is most easily done using a Digital Evaluation Board (DEB).

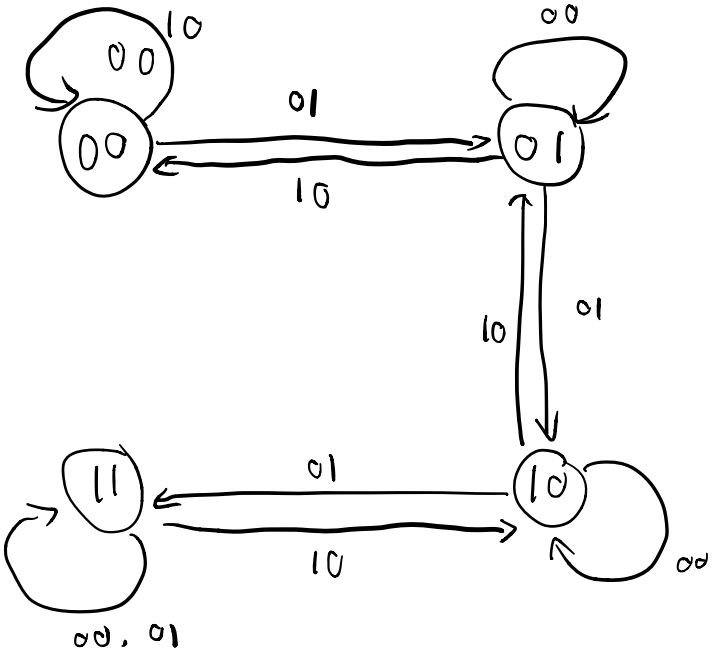
You may check your progress at any time, during office hours or lab. Experimentation is encouraged!

Although you may find and use IC's supplied by the lab, we do not guarantee that parts will always be available. You are responsible for obtaining your own hardware if needed, which is best with a DEB-1002. Please see more info in Lecture Set 1 or syllabus for acquiring necessary course materials.

1.(c)

Present $(Q_1\ Q_0)$	Next, R = 1 (XY) 00	Next, R = 1 (XY) 01	Next, R = 1 (XY) 10	Next, R = 0 (XY) dd
0 0	0 0	0 1	0 0	1 1
0 1	0 1	1 0	0 0	1 1
1 0	1 0	1 1	0 1	1 1
1 1	1 1	1 1	1 0	1 1

(d)
control input: X Y



(e)

Q_1^*

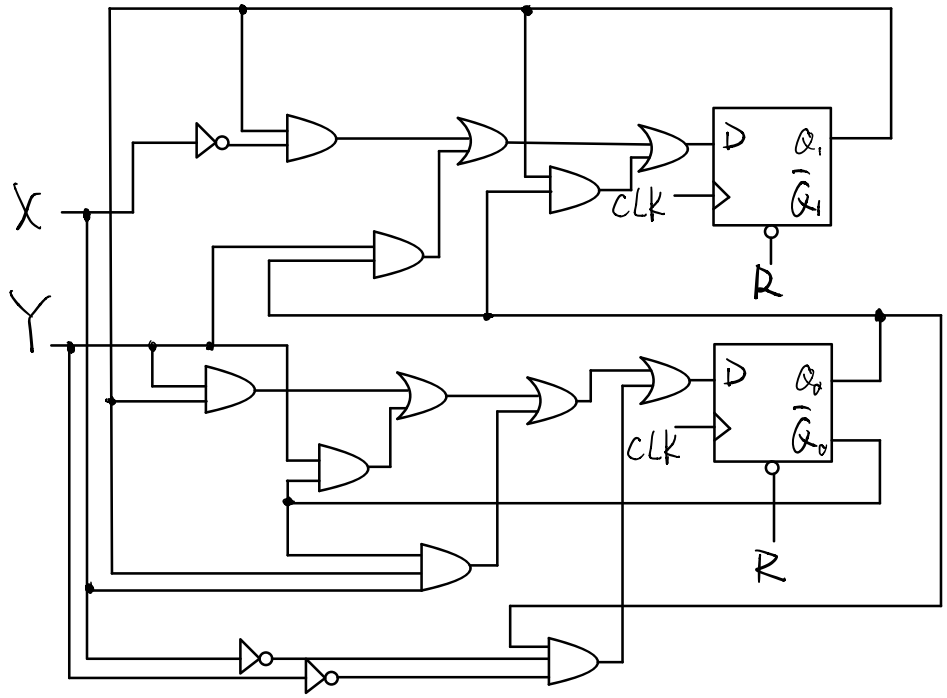
X Y \ Q_1Q_0	00	01	11	10
0 0	0	0	1	1
0 1	0	1	1	1
1 1	d	d	d	d
1 0	0	0	1	0

$$Q_1^* = Q_1\bar{X} + Q_0Y + Q_1Q_0$$

Q_0^*

X Y \ Q_1Q_0	00	01	11	10
0 0	0	1	1	0
0 1	1	0	1	1
1 1	d	d	d	d
1 0	0	0	0	1

$$Q_0^* = Q_1Y + \bar{Q}_0Y + Q_1\bar{Q}_0X + Q_0\bar{X}\bar{Y}$$

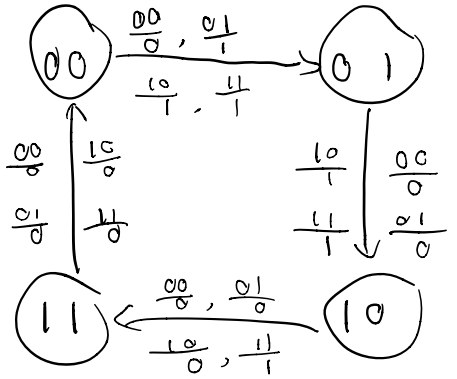


(f) When input Condition is too high or too low, that is, when Vboost always higher than 2.1 V or lower than 1.8 V, we hope to keep decreasing / increasing the voltage for a while, until the Vboost back to the expected range.

2. (a)

Current (C1 C0)	next	output S				(input d1 d0)
		00	01	10	11	
0 0	0 1	0	1	1	1	
0 1	1 0	0	0	1	1	
1 0	1 1	0	0	0	1	
1 1	0 0	0	0	0	0	

(b)



(c)

C_1^*:

C_1 \ C_0	0	1
0	0	1
1	1	0

$C_1^* = \bar{C}_1 C_0 + C_1 \bar{C}_0$

$= C_1 \oplus C_0$

C_0^*:

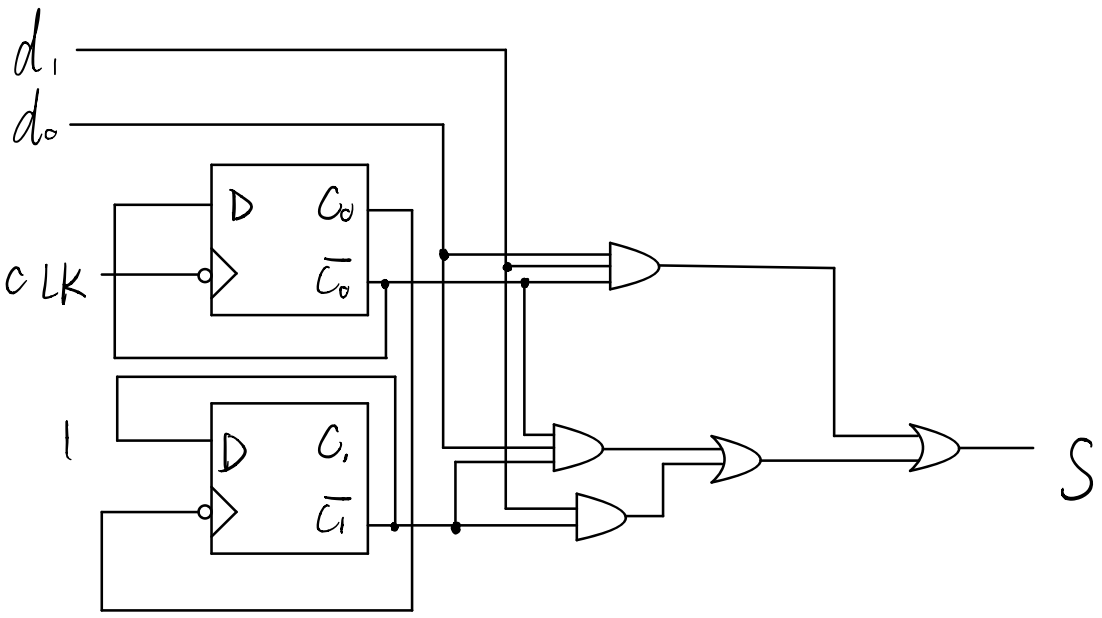
C_1 \ C_0	0	1
0	1	1
1	0	0

$C_0^* = \bar{C}_0$

S:

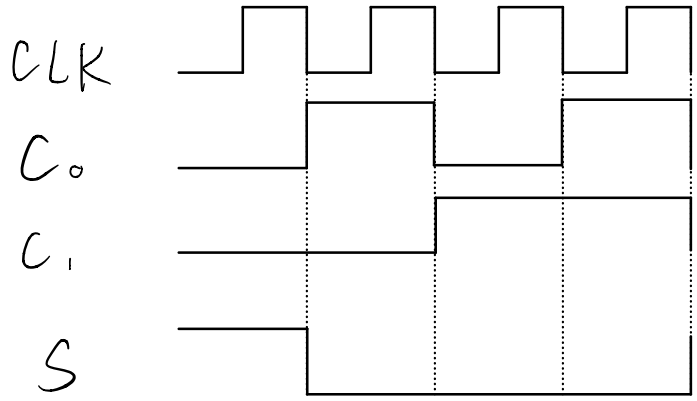
$d_1 d_0$ \ $C_1 C_0$	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	1	0	0

$S = \bar{C}_1 d_1 + \bar{C}_1 \bar{C}_0 d_0 + \bar{C}_0 d_1 d_0$

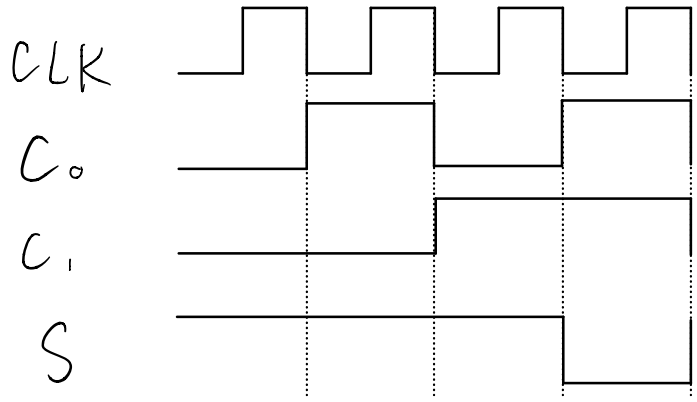


(d)

25%:



75%:



(e) we know that for a cycle, CLK's frequency is 4, while S is 1

So when CLK's frequency is 1MHz,

S's frequency is 250kHz

(f) Duty cycle precision means the number of bits. Higher precision, more bites. more flip flops in the circuit. That means more complecated the circuit will be and more mechanical error will appear. So less precise duty will make circuit easier and make less error.

3. one drive URL:
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The circuit is the same as 2(c), use 2 DFF to build a 2-bits counter and use And, Or gates to access S.