RPS-Z7020-TK User Guide
Rev1.3

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Version :

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0.2-00.00	2012-12-24	RPS-Z7020-TK Rev1.2 User Guide	HUINS

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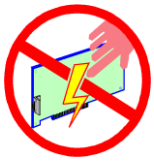

Caution

Be careful to use.this product. It is very sensitive to static discharge and make sure that you're properly grounded whenever handling the board directly.

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1. 개 요

RPS-Z7020-TK는 RPS-Z7020M을 탑재한 보드이고, Multi-Media 기능을 포함한다.

RPS-Z7020M은 Xilinx Zynq-7000을 내장하고 있는 모듈이다. Xilinx Zynq-7000은 프로그래밍 가능한 SoC이고, PS(Processor System)과 PL(Programmable Logic)로 나뉜다. 그러므로 Xilinx Zynq-7000 SoC는 PS Pin과 PL Pin을 보유하고 있다. PS Pin과 연결된 Device들 대부분은 RPS-Z7020M에 탑재되어 있고, PL Pin과 연결된 Device들은 RPS-Z7020-TK 보드에 탑재되어 있다. RPS-Z7020M은 RPS-Z7020-TK 보드와 다른 Base 보드에 연결될 수도 있다.

RPS-Z7020-TK 보드에 탑재된 Device들의 사항은 다음 1.1절에 나열되어 있다. 특히 RPS-Z7020-TK는 200만화소 카메라 인터페이스와 4.2인치 TFT-LCD를 탑재하여, 영상 처리에 적합하도록 되어 있다.

RPS-Z7020-TK에 탑재된 device들을 구동하기 위한 예제들과 교재를 제공한다.

1.1. RPS-Z7020-TK 보드 사양

- Samtec QTH-060(120pin) connector 2ea
- 5V input power connector and Power Switch
- 4.3 Inch TFT-LCD
- Text-LCD (16X2 Character)
- 7-Segment (4X2 Display)
- USB port (for UART)
- 8-DIP switches, LED 8ea, Push button 4ea
- HDMI output port
- Audio input/output port
- Camera Interface 2ea
- OSC connector (for clock input) 1ea and PLL system
- ARM JTAG port
- 14 pin GPIO connector

1.2. RPS-Z7020M 사양

- All programmable SoC XC7Z020-1CLF484
- 1GB DDR3 SDRAM
- T-Flash memory socket
- USB2.0 ULPI transceiver
- 1000/100/10 Ethernet phy
- Push button 2ea and LED 2ea
- QT/SH-060(120pin) Connectors 2ea (200 Zynq PL I/Os)
- 14pin JTAG Port

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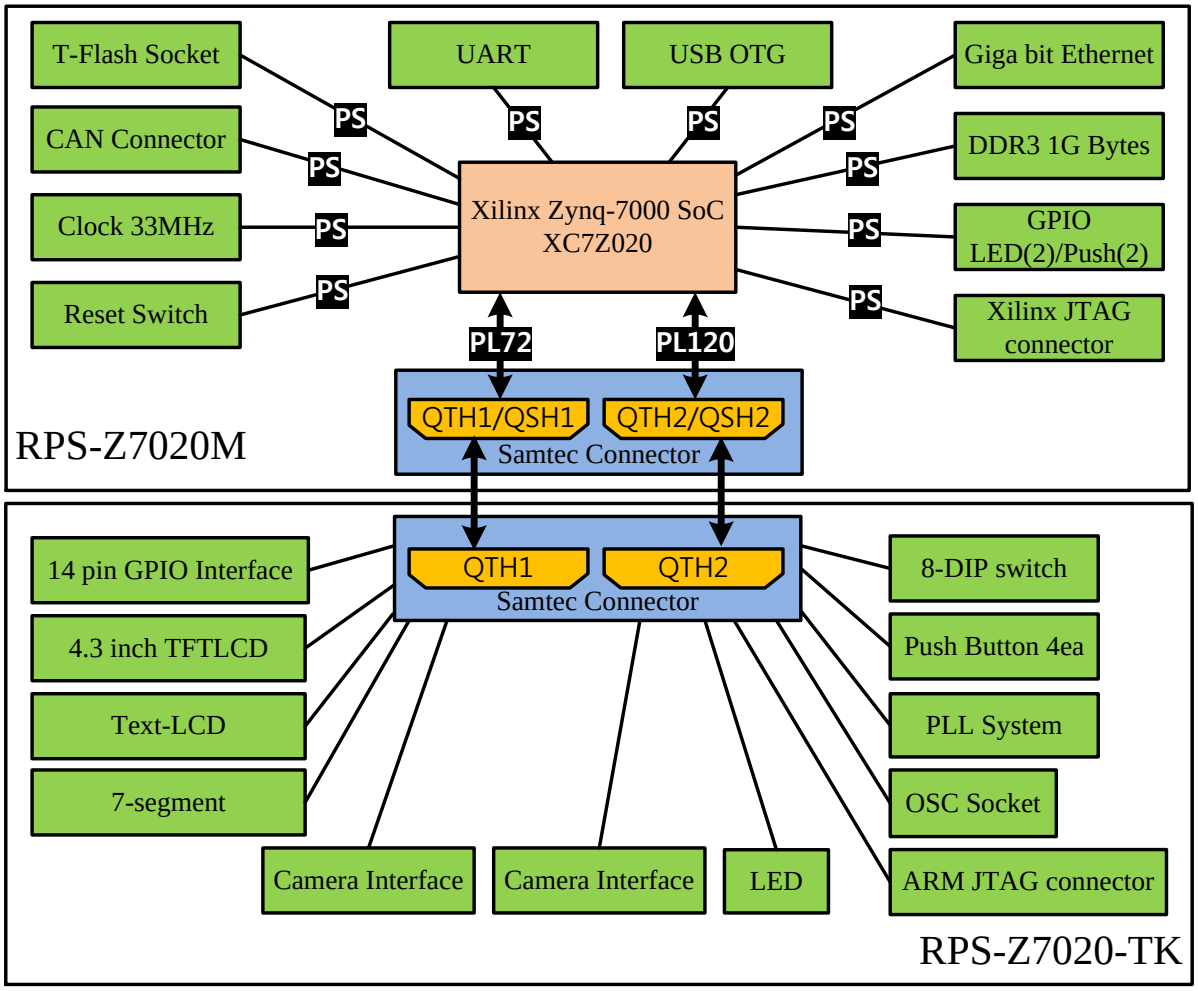
1.3. RPS-Z7020-TK Block Diagram



Samtec connector 는 QTH 와 QSH 가 된다. QTH 는 보드의 윗면에 탑재된 것을 가리키고, QSH 는 보드의 밑면에 탑재된 것을 가리킨다. RPS-Z7020-TK 의 윗면에 있는 Samtec connector 와 RPS-Z7020M 의 밑면에 있는 Samtec connector 가 서로 연결된다.

RPS-Z7020M 은 QTH 와 QSH 모두 가지고 있다. QTH 와 QSH 는 상호 연결되어 있어서, RPS-Z7020M 의 QTH 와 연결되어 사용되는 base 보드가 탑재될 수 있다.

OSC Socket 은 Half Size 의 Oscillator 를 장착할 수 있는 Socket 이고, 제품 납품될 때 25MHz 가 장착된다.

ARM JTAG Connector 는 Xilinx Zynq-7000 PS 에 있는 PJAG 와 연결하고, Bootloader 가 동작되고 있는 상태에서 Cortex-A9 을 디버깅하는 목적으로 사용 가능하다.

위의 Block Diagram 에서 대부분의 Device 가 한꺼번에 동작시키려면, 제품 CD 에 있는 예제를 참고하면 된다.

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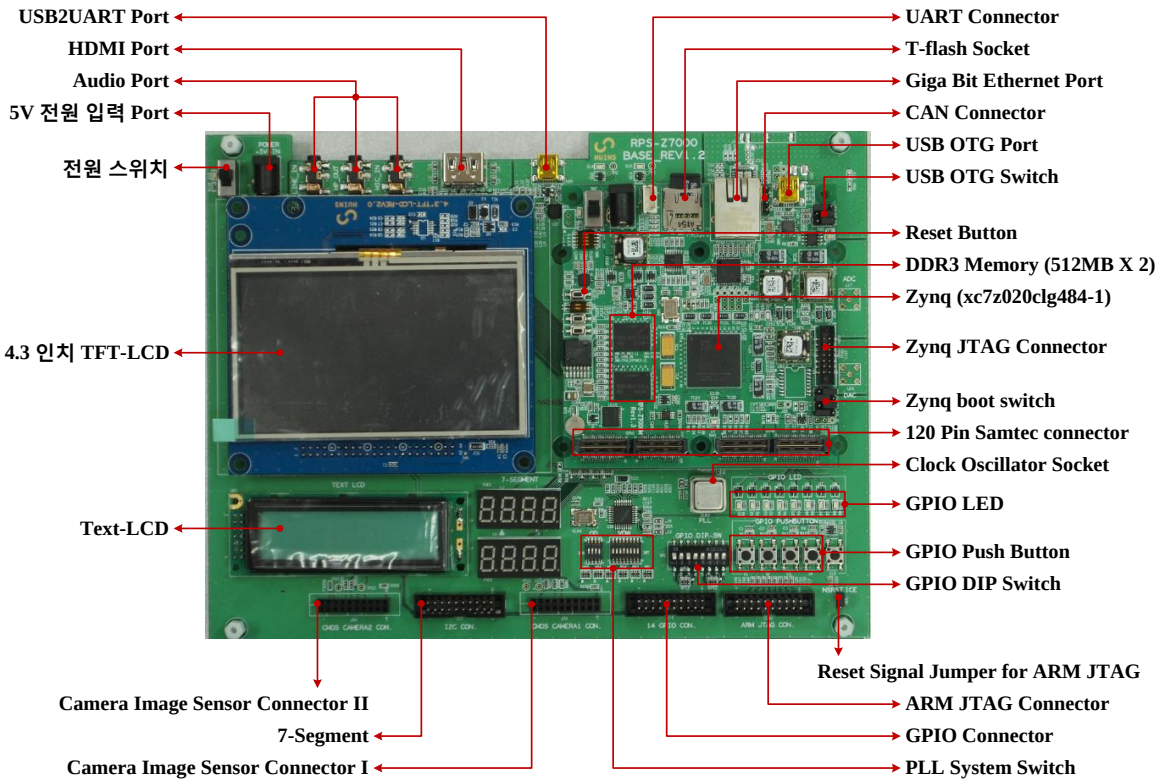
1.4. 보드 외관

각 장치의 세부적인 회로도와 연결된 Zynq PL 핀 목록은 2장에 나열되어 있다.
다음 그림은 각 장치들의 이름과 위치를 나열하고 있다.
그림에서 보이는 Samtec connector는 RPS-Z7020M의 QTH connector가 된다. RPS-Z7020M의 QSH connector와 RPS-Z7020-TK의 QTH connector는 RPS-Z7020M 밑에 있어서 보이지 않는다.
그림에 명시된 5V 전원 입력 포트와 전원 스위치는 RPS-Z7020-TK 보드에 있는 것으로 RPS-Z7020M에 전원을 공급한다. RPS-Z7020-TK 보드는 RPS-Z7020M에 있는 전원 스위치와 5V 전원 입력 포트는 사용하지 않는다.



RPS-Z7020-TK 보드 외관

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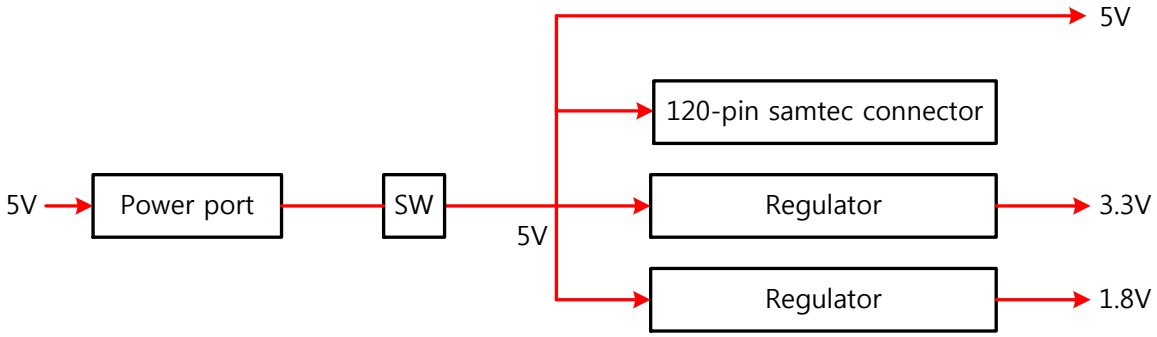
2. 기능 설명

2.1. power

RPS-Z7020-TK 보드는 5V, 3.3V, 1.8V 전원을 사용한다. 5V는 전원 커넥터로부터 받아 사용하고, 5V를 3.3V와 1.8V로 변환하여 사용한다.



Block diagram에서 120-pin Samtec connector에 5V 전원이 들어가고, RPS-Zynq7000M은 120-pin samtec connector를 통해서 5V 전원을 공급받을 수 있다.
대부분의 장치들은 3.3V를 사용하고, HDMI 출력 장치가 1.8V를 사용한다.

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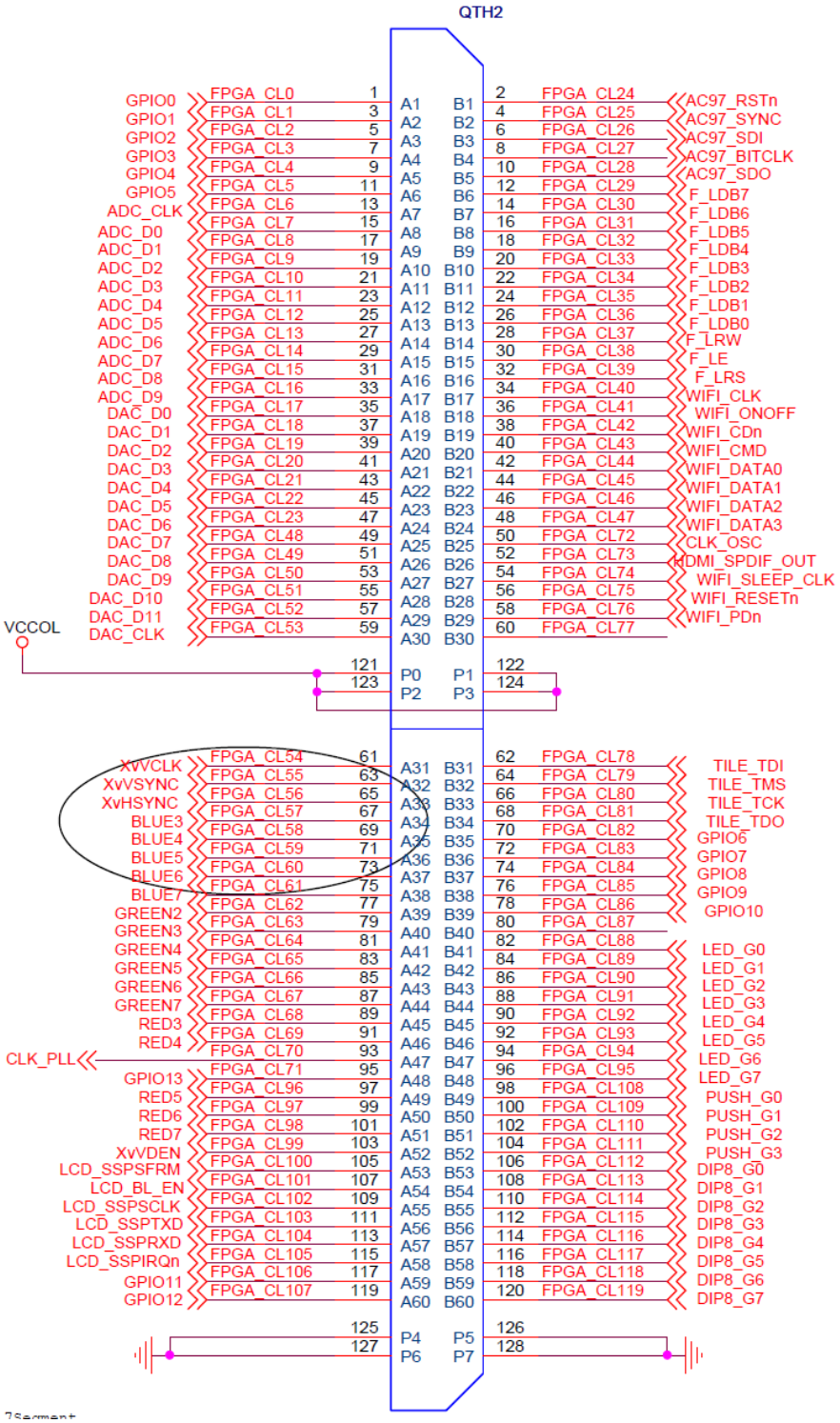
2.2. 120핀 samtec connector

RPS-Z7020-TK에 있는 모든 장치들은 120핀 samtec connector와 연결되어 있다.

RPS-Zynq7000M에 있는 Xilinx Zynq 칩(xc7z020clg484)의 모든 PL(Programmable Logic) 핀은 120핀 samtec connector와 연결되어 있다. 다음은 samtec connector인 QTH2 회로이고, 다음 페이지에 QTH1 회로가 있다.



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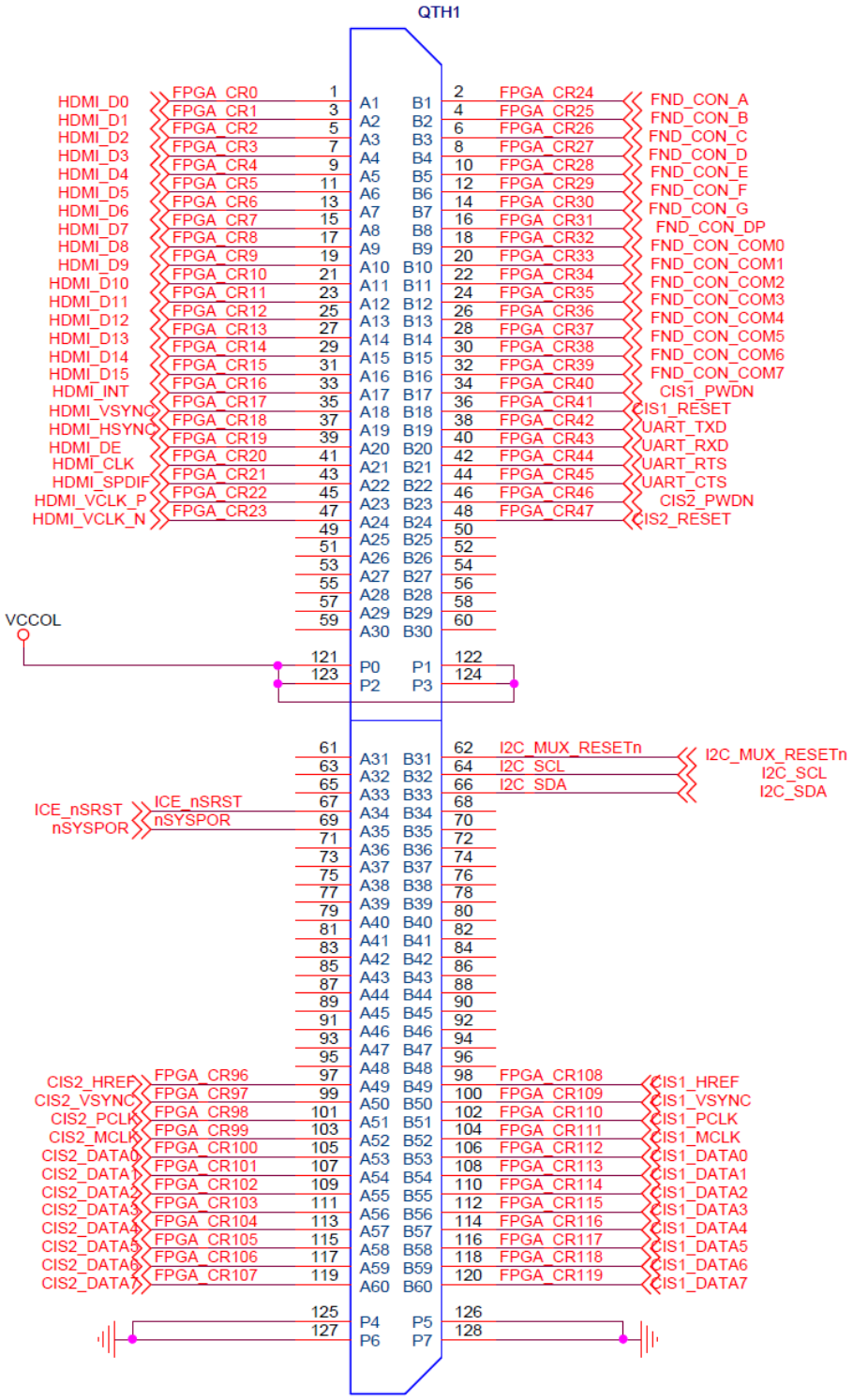

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다음 표에서 RPS-Zynq7000M을 장착하였을 때, PL 핀 번호와 장치들 목록을 나열하고 있다.

NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CL0	F16	QTH2-1	J14-2	GPIO0	35
FPGA_CL1	E16	QTH2-3	J14-4	GPIO1	35
FPGA_CL2	D16	QTH2-5	J14-6	GPIO2	35
FPGA_CL3	D17	QTH2-7	J14-8	GPIO3	35
FPGA_CL4	E15	QTH2-9	J14-10	GPIO4	35
FPGA_CL5	D15	QTH2-11	J14-12	GPIO5	35
FPGA_CL6	G15	QTH2-13	Reserved	Reserved	35
FPGA_CL7	G16	QTH2-15	Reserved	Reserved	35
FPGA_CL8	F18	QTH2-17	Reserved	Reserved	35
FPGA_CL9	E18	QTH2-19	Reserved	Reserved	35
FPGA_CL10	G17	QTH2-21	Reserved	Reserved	35
FPGA_CL11	F17	QTH2-23	Reserved	Reserved	35
FPGA_CL12	C15	QTH2-25	Reserved	Reserved	35
FPGA_CL13	B15	QTH2-27	Reserved	Reserved	35
FPGA_CL14	B16	QTH2-29	Reserved	Reserved	35
FPGA_CL15	B17	QTH2-31	Reserved	Reserved	35
FPGA_CL16	A16	QTH2-33	Reserved	Reserved	35
FPGA_CL17	A17	QTH2-35	Reserved	Reserved	35
FPGA_CL18	A18	QTH2-37	Reserved	Reserved	35
FPGA_CL19	A19	QTH2-39	Reserved	Reserved	35
FPGA_CL20	C17	QTH2-41	Reserved	Reserved	35
FPGA_CL21	C18	QTH2-43	Reserved	Reserved	35
FPGA_CL22	D18	QTH2-45	Reserved	Reserved	35
FPGA_CL23	C19	QTH2-47	Reserved	Reserved	35
FPGA_CL24	B19	QTH2-2	U40-11	AC97_RSTn	35
FPGA_CL25	B20	QTH2-4	U40-10	AC97_SYNC	35
FPGA_CL26	D20	QTH2-6	U40-8	AC97_SDI	35
FPGA_CL27	C20	QTH2-8	U40-6	AC97_BITCLK	35
FPGA_CL28	A21	QTH2-10	U40-5	AC97_SDO	35
FPGA_CL29	A22	QTH2-12	U21-14	F_LDB7	35
FPGA_CL30	D22	QTH2-14	U21-13	F_LDB6	35
FPGA_CL31	C22	QTH2-16	U21-12	F_LDB5	35
FPGA_CL32	E21	QTH2-18	U21-11	F_LDB4	35
FPGA_CL33	D21	QTH2-20	U21-10	F_LDB3	35
FPGA_CL34	B21	QTH2-22	U21-9	F_LDB2	35
FPGA_CL35	B22	QTH2-24	U21-8	F_LDB1	35

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NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CL36	H19	QTH2-26	U21-7	F_LDB0	35
FPGA_CL37	H20	QTH2-28	U21-5	F_LRW	35
FPGA_CL38	G19	QTH2-30	U21-6	F_LE	35
FPGA_CL39	F19	QTH2-32	U21-4	F_LRS	35
FPGA_CL40	E19	QTH2-34	Reserved	Reserved	35
FPGA_CL41	E20	QTH2-36	Reserved	Reserved	35
FPGA_CL42	G20	QTH2-38	Reserved	Reserved	35
FPGA_CL43	G21	QTH2-40	Reserved	Reserved	35
FPGA_CL44	F21	QTH2-42	Reserved	Reserved	35
FPGA_CL45	F22	QTH2-44	Reserved	Reserved	35
FPGA_CL46	H22	QTH2-46	Reserved	Reserved	35
FPGA_CL47	G22	QTH2-48	Reserved	Reserved	35
FPGA_CL48	J15	QTH2-49	Reserved	Reserved	34
FPGA_CL49	K15	QTH2-51	Reserved	Reserved	34
FPGA_CL50	J16	QTH2-53	Reserved	Reserved	34
FPGA_CL51	J17	QTH2-55	Reserved	Reserved	34
FPGA_CL52	K16	QTH2-57	Reserved	Reserved	34
FPGA_CL53	L16	QTH2-59	Reserved	Reserved	34
FPGA_CL54	L17	QTH2-61	J25-1	XvVCLK	34
FPGA_CL55	M17	QTH2-63	J25-3	XvVSYNC	34
FPGA_CL56	N17	QTH2-65	J25-2	XvHSYNC	34
FPGA_CL57	N18	QTH2-67	J25-6	BLUE3	34
FPGA_CL58	M15	QTH2-69	J25-7	BLUE4	34
FPGA_CL59	M16	QTH2-71	J25-8	BLUE5	34
FPGA_CL60	J18	QTH2-73	J25-9	BLUE6	34
FPGA_CL61	K18	QTH2-75	J25-10	BLUE7	34
FPGA_CL62	J21	QTH2-77	J25-12	GREEN2	34
FPGA_CL63	J22	QTH2-79	J25-13	GREEN3	34
FPGA_CL64	J20	QTH2-81	J25-14	GREEN4	34
FPGA_CL65	K21	QTH2-83	J25-15	GREEN5	34
FPGA_CL66	L21	QTH2-85	J25-16	GREEN6	34
FPGA_CL67	L22	QTH2-87	J25-17	GREEN7	34
FPGA_CL68	K19	QTH2-89	J25-20	RED3	34
FPGA_CL69	K20	QTH2-91	J25-21	RED4	34
FPGA_CL70	L18	QTH2-93	U36-15	CLK_PLL	34
FPGA_CL71	L19	QTH2-95	J14-9	GPIO13	34
FPGA_CL72	M19	QTH2-50	CLK3-3	CLK_OSC	34

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NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CL73	M20	QTH2-52	U6-46	HDMI_SPDIF_OUT	34
FPGA_CL74	N19	QTH2-54	Reserved	Reserved	34
FPGA_CL75	N20	QTH2-56	Reserved	Reserved	34
FPGA_CL76	M21	QTH2-58	Reserved	Reserved	34
FPGA_CL77	M22	QTH2-60	Reserved	Reserved	34
FPGA_CL78	N22	QTH2-62	CON3-5	TILE_TDI	34
FPGA_CL79	P22	QTH2-64	CON3-7	TILE_TMS	34
FPGA_CL80	R20	QTH2-66	CON3-9	TILE_TCK	34
FPGA_CL81	R21	QTH2-68	CON3-13	TILE_TDO	34
FPGA_CL82	P20	QTH2-70	J14-14	GPIO6	34
FPGA_CL83	P21	QTH2-72	J14-16	GPIO7	34
FPGA_CL84	N15	QTH2-74	J14-18	GPIO8	34
FPGA_CL85	P15	QTH2-76	J14-20	GPIO9	34
FPGA_CL86	P17	QTH2-78	J14-3	GPIO10	34
FPGA_CL87	P18	QTH2-80	Reserved	Reserved	34
FPGA_CL88	T16	QTH2-82	Q1-G	LED_G0	34
FPGA_CL89	T17	QTH2-84	Q2-G	LED_G1	34
FPGA_CL90	R19	QTH2-86	Q3-G	LED_G2	34
FPGA_CL91	T19	QTH2-88	Q4-G	LED_G3	34
FPGA_CL92	R18	QTH2-90	Q5-G	LED_G4	34
FPGA_CL93	T18	QTH2-92	Q6-G	LED_G5	34
FPGA_CL94	P16	QTH2-94	Q7-G	LED_G6	34
FPGA_CL95	R16	QTH2-96	Q8-G	LED_G7	34
FPGA_CL96	T21	QTH2-97	J25-22	RED5	33
FPGA_CL97	U21	QTH2-99	J25-23	RED6	33
FPGA_CL98	T22	QTH2-101	J25-24	RED7	33
FPGA_CL99	U22	QTH2-103	J25-26	XvVDEN	33
FPGA_CL100	V22	QTH2-105	J25-31	LCD_SSPSFRM	33
FPGA_CL101	W22	QTH2-107	J25-32	LCD_BL_EN	33
FPGA_CL102	W20	QTH2-109	J25-37	LCD_SSPSCLK	33
FPGA_CL103	W21	QTH2-111	J25-39	LCD_SSPTXD	33
FPGA_CL104	U20	QTH2-113	J25-38	LCD_SSPRXD	33
FPGA_CL105	V20	QTH2-115	J25-40	LCD_SSPIRQn	33
FPGA_CL106	V18	QTH2-117	J14-5	GPIO11	33
FPGA_CL107	V19	QTH2-119	J14-7	GPIO12	33
FPGA_CL108	Y18	QTH2-98	S1-1/2	PUSH_G0	33
FPGA_CL109	AA18	QTH2-100	S2_1/2	PUSH_G1	33

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FPGA_CL110	Y19	QTH2-102	S3_1/2	PUSH_G2	33
FPGA_CL111	AA19	QTH2-104	S4_1/2	PUSH_G3	33
FPGA_CL112	Y20	QTH2-106	SW1-1	DIP8_G0	33
FPGA_CL113	Y21	QTH2-108	SW1-2	DIP8_G1	33
FPGA_CL114	AB19	QTH2-110	SW1-3	DIP8_G2	33
FPGA_CL115	AB20	QTH2-112	SW1-4	DIP8_G3	33
FPGA_CL116	AA22	QTH2-114	SW1-5	DIP8_G4	33
FPGA_CL117	AB22	QTH2-116	SW1-6	DIP8_G5	33
FPGA_CL118	AA21	QTH2-118	SW1-7	DIP8_G6	33
FPGA_CL119	AB21	QTH2-120	SW1-8	DIP8_G7	33
FPGA_CR0	V10	QTH1-1	U6-88	HDMI_D0	13
FPGA_CR1	V9	QTH1-3	U6-87	HDMI_D1	13
FPGA_CR2	V8	QTH1-5	U6-86	HDMI_D2	13
FPGA_CR3	W8	QTH1-7	U6-85	HDMI_D3	13
FPGA_CR4	W11	QTH1-9	U6-84	HDMI_D4	13
FPGA_CR5	W10	QTH1-11	U6-83	HDMI_D5	13
FPGA_CR6	V12	QTH1-13	U6-82	HDMI_D6	13
FPGA_CR7	W12	QTH1-15	U6-81	HDMI_D7	13
FPGA_CR8	U12	QTH1-17	U6-80	HDMI_D8	13
FPGA_CR9	U11	QTH1-19	U6-78	HDMI_D9	13
FPGA_CR10	U10	QTH1-21	U6-74	HDMI_D10	13
FPGA_CR11	U9	QTH1-23	U6-73	HDMI_D11	13
FPGA_CR12	AA12	QTH1-25	U6-72	HDMI_D12	13
FPGA_CR13	AB12	QTH1-27	U6-71	HDMI_D13	13
FPGA_CR14	AA11	QTH1-29	U6-70	HDMI_D14	13
FPGA_CR15	AB11	QTH1-31	U6-69	HDMI_D15	13
FPGA_CR16	AB10	QTH1-33	U6-45	HDMI_INT	13
FPGA_CR17	AB9	QTH1-35	U6-2	HDMI_VSYNC	13
FPGA_CR18	Y11	QTH1-37	U6-98	HDMI_HSYNC	13
FPGA_CR19	Y10	QTH1-39	U6-97	HDMI_DE	13
FPGA_CR20	AA9	QTH1-41	U6-79	HDMI_CLK	13
FPGA_CR21	AA8	QTH1-43	U6-10	HDMI_SPDIF	13
FPGA_CR22	Y9	QTH1-45	U37-4	HDMI_VCLK_P	13
FPGA_CR23	Y8	QTH1-47	U37-5	HDMI_VCLK_N	13
FPGA_CR24	Y6	QTH1-2	FND1-11, FND2-11	FND_CON_A	13
FPGA_CR25	Y5	QTH1-4	FND1-7, FND2-7	FND_CON_B	13
FPGA_CR26	AA7	QTH1-6	FND1-4, FND2-4	FND_CON_C	13

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NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CR27	AA6	QTH1-8	FND1-2, FND2-2	FND_CON_D	13
FPGA_CR28	AB2	QTH1-10	FND1-1, FND2-1	FND_CON_E	13
FPGA_CR29	AB1	QTH1-12	FND1-10, FND2-10	FND_CON_F	13
FPGA_CR30	AB5	QTH1-14	FND1-5, FND2-5	FND_CON_G	13
FPGA_CR31	AB4	QTH1-16	FND1-3, FND2-3	FND_CON_DP	13
FPGA_CR32	AB7	QTH1-18	FND1-12	FND_CON_COM0	13
FPGA_CR33	AB6	QTH1-20	FND1-9	FND_CON_COM1	13
FPGA_CR34	Y4	QTH1-22	FND1-8	FND_CON_COM2	13
FPGA_CR35	AA4	QTH1-24	FND1-6	FND_CON_COM3	13
FPGA_CR36	R6	QTH1-26	FND2-12	FND_CON_COM4	13
FPGA_CR37	T6	QTH1-28	FND2-9	FND_CON_COM5	13
FPGA_CR38	T4	QTH1-30	FND2-8	FND_CON_COM6	13
FPGA_CR39	U4	QTH1-32	FND2-6	FND_CON_COM7	13
FPGA_CR40	V5	QTH1-34	J23-4	CIS1_PWDN	13
FPGA_CR41	V4	QTH1-36	J23-20	CIS1_RESET	13
FPGA_CR42	U6	QTH1-38	U27-25	UART_TXD	13
FPGA_CR43	U5	QTH1-40	U27-24	UART_RXD	13
FPGA_CR44	V7	QTH1-42	U27-23	UART_RTS	13
FPGA_CR45	W7	QTH1-44	U27-22	UART_CTS	13
FPGA_CR46	W6	QTH1-46	J24-4	CIS2_PWDN	13
FPGA_CR47	W5	QTH1-48	J24-20	CIS2_RESET	13
FPGA_CR96	Y13	QTH1-97	J24-2	CIS2_HREF	33
FPGA_CR97	AA13	QTH1-99	J24-3	CIS2_VSYNC	33
FPGA_CR98	AB14	QTH1-101	J24-5	CIS2_PCLK	33
FPGA_CR99	AB15	QTH1-103	J24-9	CIS2_MCLK	33
FPGA_CR100	W15	QTH1-105	J24-11	CIS2_DATA0	33
FPGA_CR101	Y15	QTH1-107	J24-12	CIS2_DATA1	33
FPGA_CR102	Y14	QTH1-109	J24-13	CIS2_DATA2	33
FPGA_CR103	AA14	QTH1-111	J24-14	CIS2_DATA3	33
FPGA_CR104	V13	QTH1-113	J24-16	CIS2_DATA4	33
FPGA_CR105	W13	QTH1-115	J24-17	CIS2_DATA5	33
FPGA_CR106	V14	QTH1-117	J24-18	CIS2_DATA6	33
FPGA_CR107	V15	QTH1-119	J24-19	CIS2_DATA7	33
FPGA_CR108	W17	QTH1-98	J23-2	CIS1_HREF	33
FPGA_CR109	W18	QTH1-100	J23-3	CIS1_VSYNC	33
FPGA_CR110	W16	QTH1-102	J23-5	CIS1_PCLK	33
FPGA_CR111	Y16	QTH1-104	J23-9	CIS1_MCLK	33

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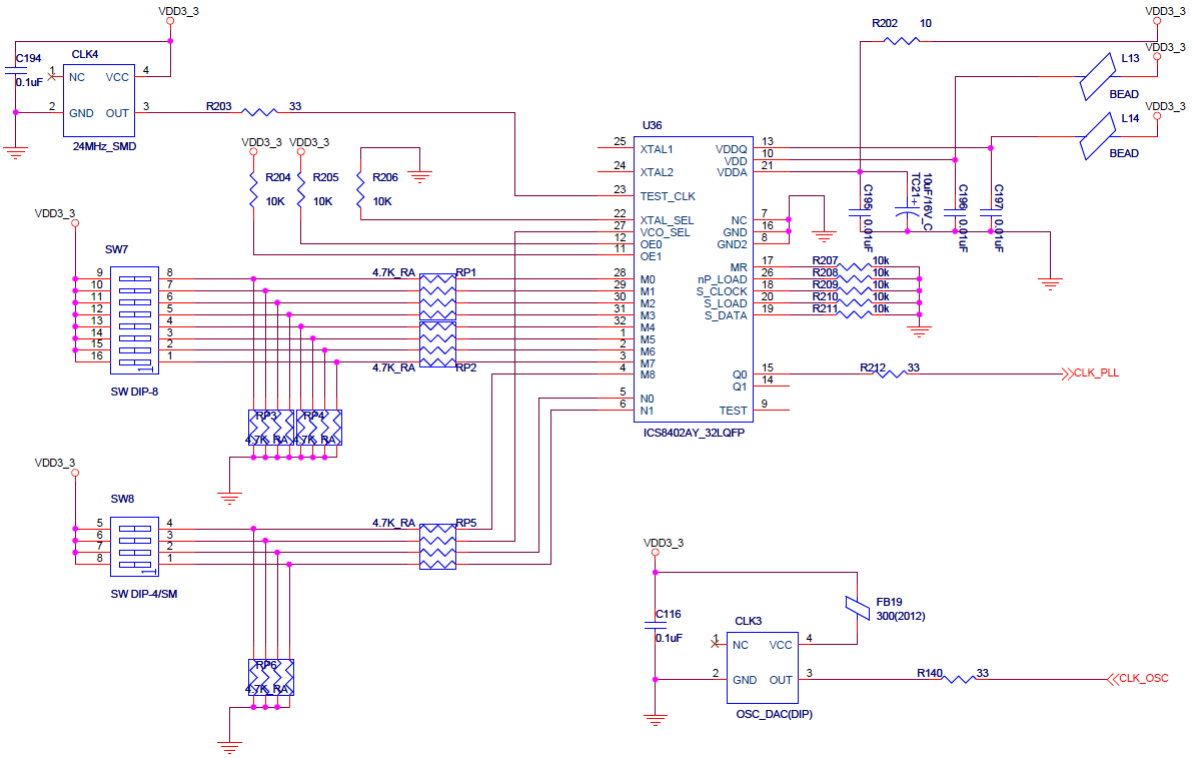
NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CR112	U15	QTH1-106	J23-11	CIS1_DATA0	33
FPGA_CR113	U16	QTH1-108	J23-12	CIS1_DATA1	33
FPGA_CR114	U17	QTH1-110	J23-13	CIS1_DATA2	33
FPGA_CR115	V17	QTH1-112	J23-14	CIS1_DATA3	33
FPGA_CR116	AA17	QTH1-114	J23-16	CIS1_DATA4	33
FPGA_CR117	AB17	QTH1-116	J23-17	CIS1_DATA5	33
FPGA_CR118	AA16	QTH1-118	J23-18	CIS1_DATA6	33
FPGA_CR119	AB16	QTH1-120	J23-19	CIS1_DATA7	33

2.3. clock

RPS-Z7020-TK는 Clock 2개를 RPS-Z7020M에 공급한다. Clock 1개는 Oscillator Socket에서 출력되고, 나머지 1개는 PLL System에서 출력된다. 다음 clock source 회로에서 CLK_OSC 신호가 Oscillator Socket에서 출력되고, CLK_PLL 신호가 PLL System에서 출력된다. CLK_PLL 신호의 주파수는 8-DIP, 4-DIP 스위치에 의해 변경된다.



NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CL70	L18	QTH2-93	U36-15	CLK_PLL	34
FPGA_CL72	M19	QTH2-50	CLK3-3	CLK_OSC	34

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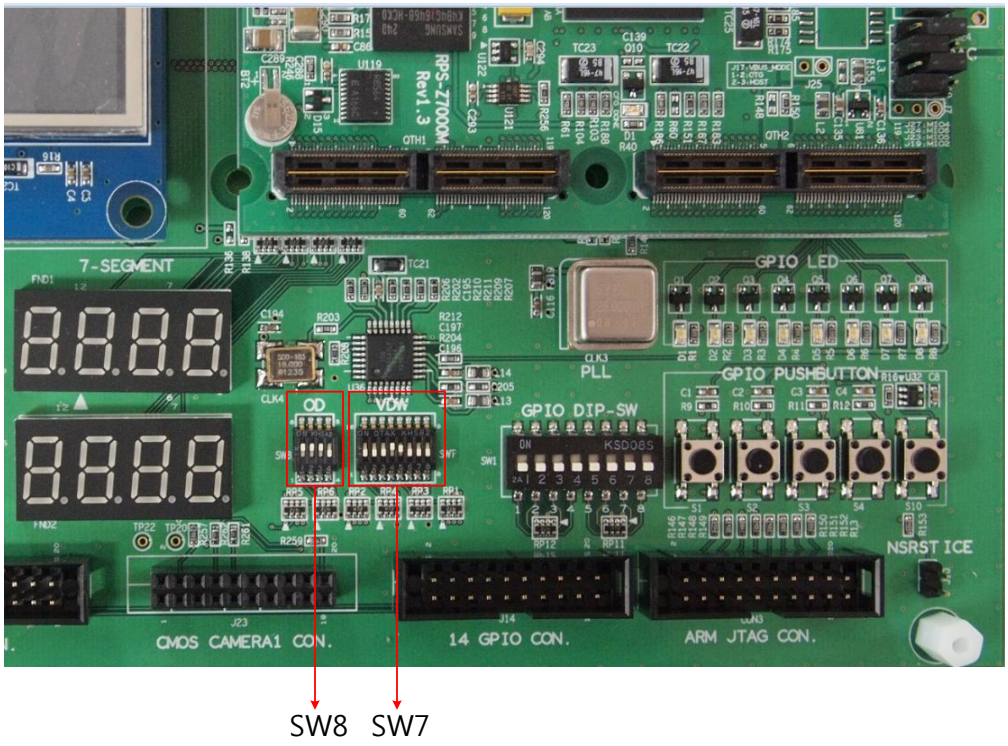

다음 표는 PLL 스위치 설정에 따른 주파수이다.
VCO 주파수는 250MHz ~ 700MHz 범위 안에 있어야 하기 때문에, M[8:6]는 항상 0이어야 된다.
PLL System의 DIP-SW(M8=SW8[4], M[7:6] = SW7[1:2])은 항상 0으로 고정되어 있어야 한다.

VCO 주파수 = [16MHz (Crystal Frequency)] X [M Divide] 가 되고,
[CLK_PLL 주파수] = [VCO 주파수] / N이 된다.

VCO_SEL8[3]이 0이 되면, VCO는 사용하지 않는다.

				32	16	8	4	2	1			
CLK_PLL	VCO_SEL SW8[3]	VCO 주파수	M	M5 SW7[3]	M4 SW7[4]	M3 SW7[5]	M2 SW7[6]	M1 SW7[7]	M0 SW7[8]	N	N1 SW8[1]	N0 SW8[2]
128MHz	1	256MHz	16		1	0	0	0	0	2	0	0
64MHz	1		16		1	0	0	0	0	4	0	1
32MHz	1		16		1	0	0	0	0	8	1	0
16MHz	1		16		1	0	0	0	0	16	1	1
136MHz	1	272MHz	17		1	0	0	0	1	2	0	0
•••	1	•••	•••		•••	•••	•••	•••	•••	•••	•••	•••
•••	1	•••	•••		•••	•••	•••	•••	•••	•••	•••	•••
42MHz	1	672MHz	42		1	1	1	0	0	16	1	1
344MHz	1	688MHz	43		1	1	1	0	1	2	0	0
172MHz	1	688MHz	43		1	1	1	0	1	4	0	1
86MHz	1	688MHz	43		1	1	1	0	1	8	1	0
43MHz	1	688MHz	43		1	1	1	0	1	16	1	1
8MHz	0	X	X		X	X	X	X	X	2	0	0
4MHz	0	X	X		X	X	X	X	X	4	0	1
2MHz	0	X	X		X	X	X	X	X	8	1	0
1MHz	0	X	X		X	X	X	X	X	16	1	1

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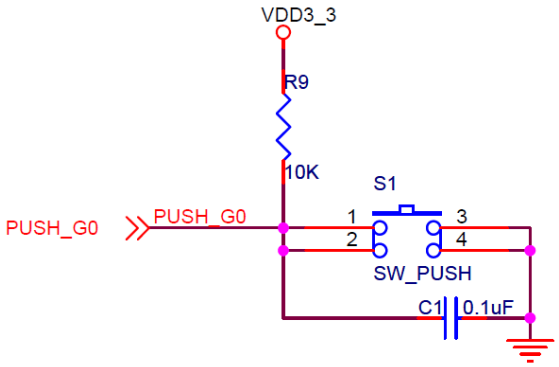
2.4. Push 버튼

회로에서 Push 버튼이 눌려졌을 때, PUSH_G0는 Low가 된다.



NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CL108	Y18	QTH2-98	S1_1/2	PUSH_G0	33
FPGA_CL109	AA18	QTH2-100	S2_1/2	PUSH_G1	33
FPGA_CL110	Y19	QTH2-102	S3_1/2	PUSH_G2	33
FPGA_CL111	AA19	QTH2-104	S4_1/2	PUSH_G3	33

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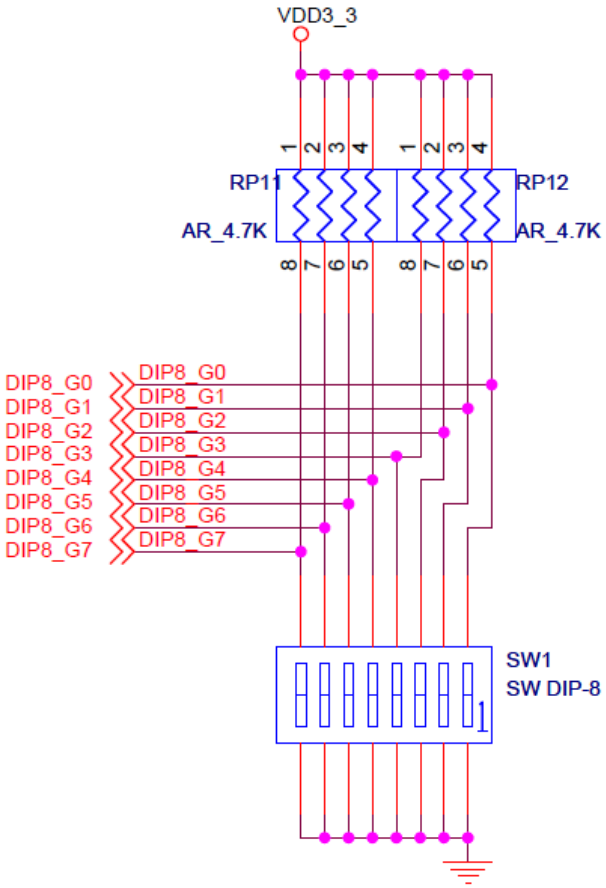
2.5. DIP-8 스위치

DIP-8의 1번 스위치가 ON이 되었을 때, DIP8_G0은 Low가 된다.



NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CL112	Y20	QTH2-106	SW1-1	DIP8_G0	33
FPGA_CL113	Y21	QTH2-108	SW1-2	DIP8_G1	33
FPGA_CL114	AB19	QTH2-110	SW1-3	DIP8_G2	33
FPGA_CL115	AB20	QTH2-112	SW1-4	DIP8_G3	33
FPGA_CL116	AA22	QTH2-114	SW1-5	DIP8_G4	33
FPGA_CL117	AB22	QTH2-116	SW1-6	DIP8_G5	33
FPGA_CL118	AA21	QTH2-118	SW1-7	DIP8_G6	33
FPGA_CL119	AB21	QTH2-120	SW1-8	DIP8_G7	33

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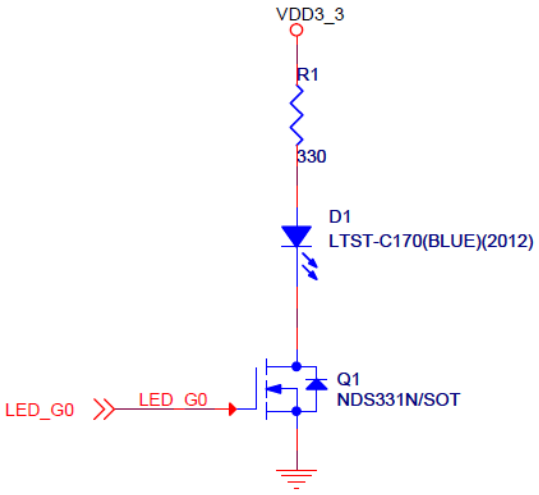
2.6. LED

LED_G0이 High가 되어야 D1은 발광한다.



NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CL88	T16	QTH2-82	Q1-G	LED_G0	34
FPGA_CL89	T17	QTH2-84	Q2-G	LED_G1	34
FPGA_CL90	R19	QTH2-86	Q3-G	LED_G2	34
FPGA_CL91	T19	QTH2-88	Q4-G	LED_G3	34
FPGA_CL92	R18	QTH2-90	Q5-G	LED_G4	34
FPGA_CL93	T18	QTH2-92	Q6-G	LED_G5	34
FPGA_CL94	P16	QTH2-94	Q7-G	LED_G6	34
FPGA_CL95	R16	QTH2-96	Q8-G	LED_G7	34

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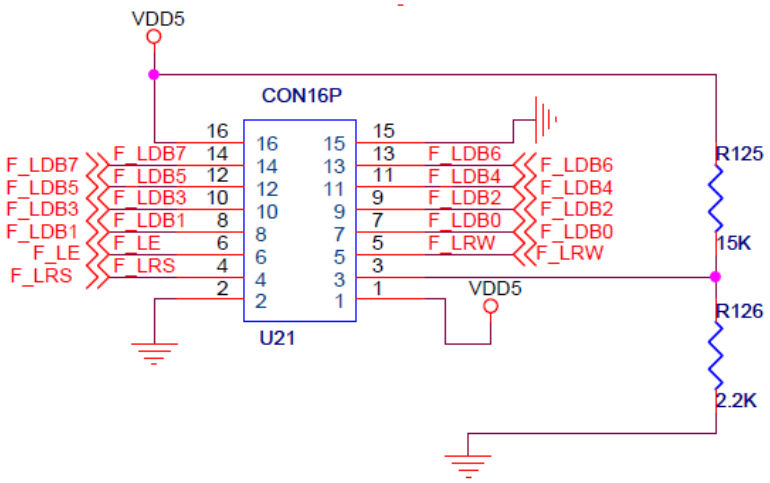
2.7. Text-LCD

다음 회로에서 Text-LCD는 8 bits 데이터(F_LDB0 ~ F_LDB7)를 입력 받는다. 그 외에 Enable 신호(F_LE), Read/Write Selection(F_LRW), Register Selection(F_LRS) 신호가 있다.



NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CL29	A22	QTH2-12	U21-14	F_LDB7	35
FPGA_CL30	D22	QTH2-14	U21-13	F_LDB6	35
FPGA_CL31	C22	QTH2-16	U21-12	F_LDB5	35
FPGA_CL32	E21	QTH2-18	U21-11	F_LDB4	35
FPGA_CL33	D21	QTH2-20	U21-10	F_LDB3	35
FPGA_CL34	B21	QTH2-22	U21-9	F_LDB2	35
FPGA_CL35	B22	QTH2-24	U21-8	F_LDB1	35
FPGA_CL36	H19	QTH2-26	U21-7	F_LDB0	35
FPGA_CL37	H20	QTH2-28	U21-5	F_LRW	35
FPGA_CL38	G19	QTH2-30	U21-6	F_LE	35
FPGA_CL39	F19	QTH2-32	U21-4	F_LRS	35

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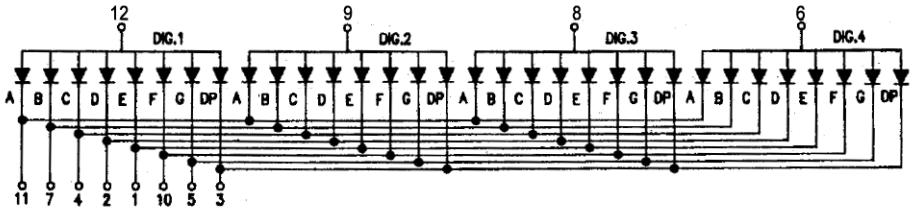
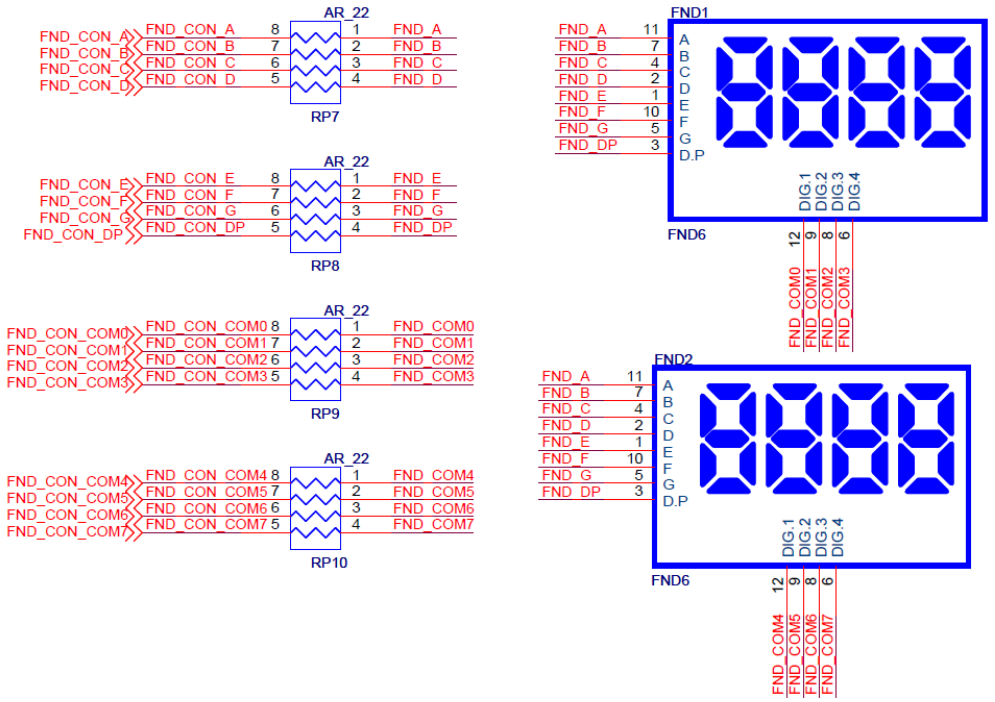
2.8. 7-Segment

RPS-Z7020-TK에는 Anode형 7-Segment가 포함되어 있다.



Anode형 7-Segment



NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CR24	Y6	QTH1-2	FND1-11, FND2-11	FND_CON_A	13
FPGA_CR25	Y5	QTH1-4	FND1-7, FND2-7	FND_CON_B	13
FPGA_CR26	AA7	QTH1-6	FND1-4, FND2-4	FND_CON_C	13
FPGA_CR27	AA6	QTH1-8	FND1-2, FND2-2	FND_CON_D	13
FPGA_CR28	AB2	QTH1-10	FND1-1, FND2-1	FND_CON_E	13
FPGA_CR29	AB1	QTH1-12	FND1-10, FND2-10	FND_CON_F	13
FPGA_CR30	AB5	QTH1-14	FND1-5, FND2-5	FND_CON_G	13
FPGA_CR31	AB4	QTH1-16	FND1-3, FND2-3	FND_CON_DP	13
FPGA_CR32	AB7	QTH1-18	FND1-12	FND_CON_COM0	13
FPGA_CR33	AB6	QTH1-20	FND1-9	FND_CON_COM1	13
FPGA_CR34	Y4	QTH1-22	FND1-8	FND_CON_COM2	13
FPGA_CR35	AA4	QTH1-24	FND1-6	FND_CON_COM3	13
FPGA_CR36	R6	QTH1-26	FND2-12	FND_CON_COM4	13
FPGA_CR37	T6	QTH1-28	FND2-9	FND_CON_COM5	13
FPGA_CR38	T4	QTH1-30	FND2-8	FND_CON_COM6	13
FPGA_CR39	U4	QTH1-32	FND2-6	FND_CON_COM7	13

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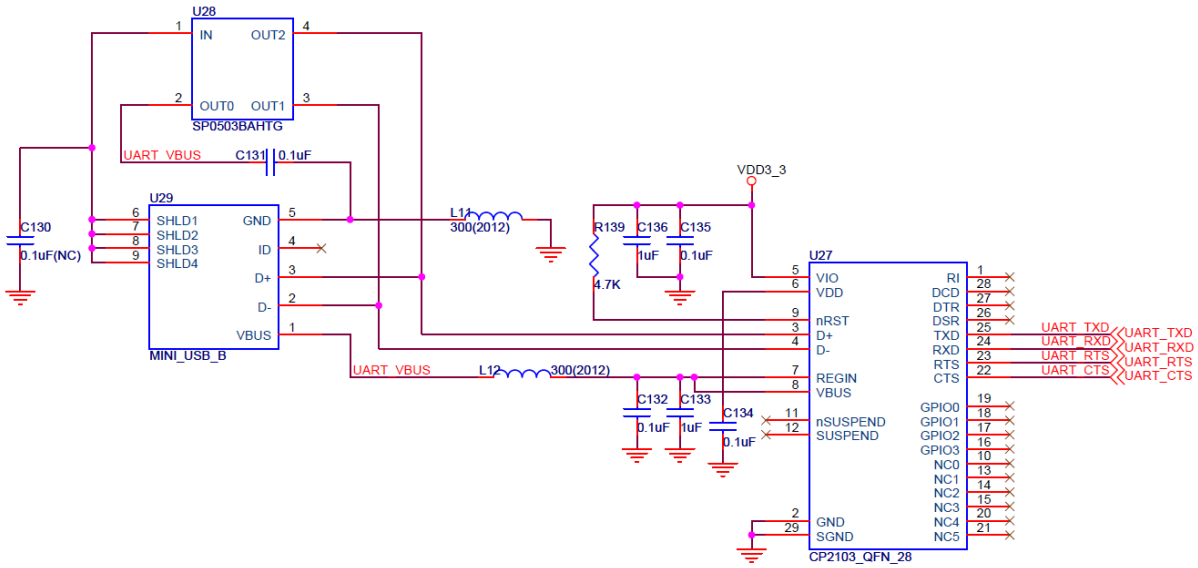
2.9. USB2UART

USB Interface를 UART로 사용 할 수 있게 해주는 장치이다. 드라이버는 다음 링크에서 다운로드 받을 수 있다.

드라이버 위치: http://www.silabs.com/products/mcu/Pages/USBtoUARTBridgeVCPDrivers.aspx



NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CR42	U6	QTH1-38	U27-25	UART_TXD	13
FPGA_CR43	U5	QTH1-40	U27-24	UART_RXD	13
FPGA_CR44	V7	QTH1-42	U27-23	UART_RTS	13
FPGA_CR45	W7	QTH1-44	U27-22	UART_CTS	13

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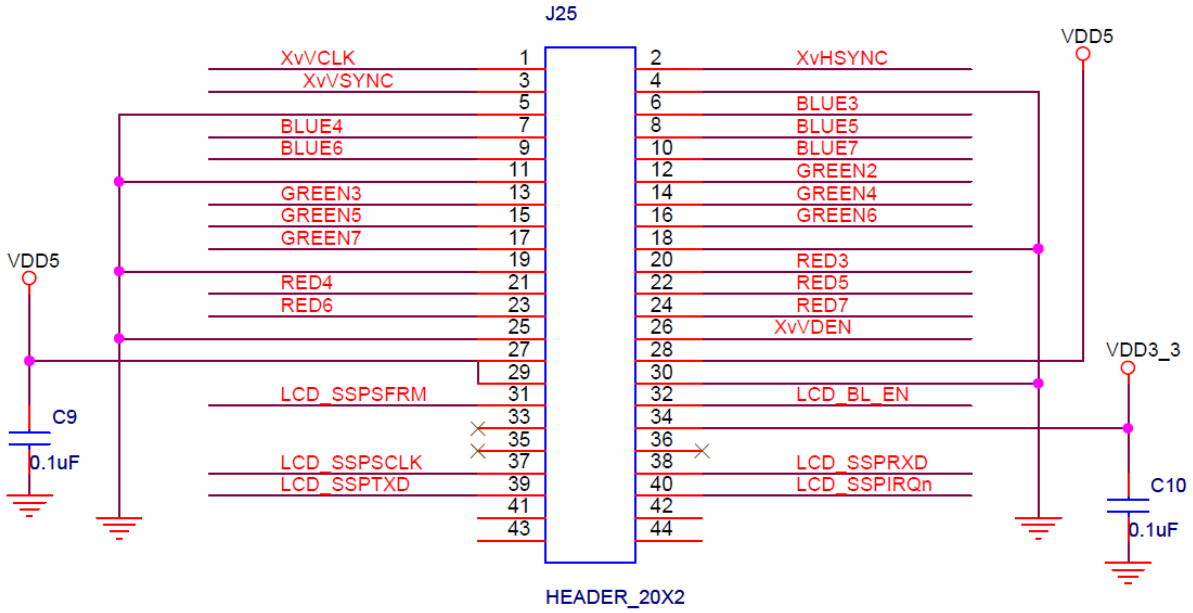
2.10. TFT-LCD

4.3인치 TFTLCD를 사용하며, Red 5 bits, Green 6 bits, Blue 5 bits의 색상이 표현 가능하다.



NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CL54	L17	QTH2-61	J25-1	XvVCLK	34
FPGA_CL55	M17	QTH2-63	J25-3	XvVSYNC	34
FPGA_CL56	N17	QTH2-65	J25-2	XvHSYNC	34
FPGA_CL57	N18	QTH2-67	J25-6	BLUE3	34
FPGA_CL58	M15	QTH2-69	J25-7	BLUE4	34
FPGA_CL59	M16	QTH2-71	J25-8	BLUE5	34
FPGA_CL60	J18	QTH2-73	J25-9	BLUE6	34
FPGA_CL61	K18	QTH2-75	J25-10	BLUE7	34
FPGA_CL62	J21	QTH2-77	J25-12	GREEN2	34
FPGA_CL63	J22	QTH2-79	J25-13	GREEN3	34
FPGA_CL64	J20	QTH2-81	J25-14	GREEN4	34
FPGA_CL65	K21	QTH2-83	J25-15	GREEN5	34
FPGA_CL66	L21	QTH2-85	J25-16	GREEN6	34
FPGA_CL67	L22	QTH2-87	J25-17	GREEN7	34
FPGA_CL68	K19	QTH2-89	J25-20	RED3	34
FPGA_CL69	K20	QTH2-91	J25-21	RED4	34
FPGA_CL96	T21	QTH2-97	J25-22	RED5	33
FPGA_CL97	U21	QTH2-99	J25-23	RED6	33
FPGA_CL98	T22	QTH2-101	J25-24	RED7	33
FPGA_CL99	U22	QTH2-103	J25-26	XvVDEN	33
FPGA_CL100	V22	QTH2-105	J25-31	LCD_SSPSFRM	33
FPGA_CL101	W22	QTH2-107	J25-32	LCD_BL_EN	33
FPGA_CL102	W20	QTH2-109	J25-37	LCD_SSPSCLK	33
FPGA_CL103	W21	QTH2-111	J25-39	LCD_SSPTXD	33
FPGA_CL104	U20	QTH2-113	J25-38	LCD_SSPRXD	33
FPGA_CL105	V20	QTH2-115	J25-40	LCD_SSPIRQn	33

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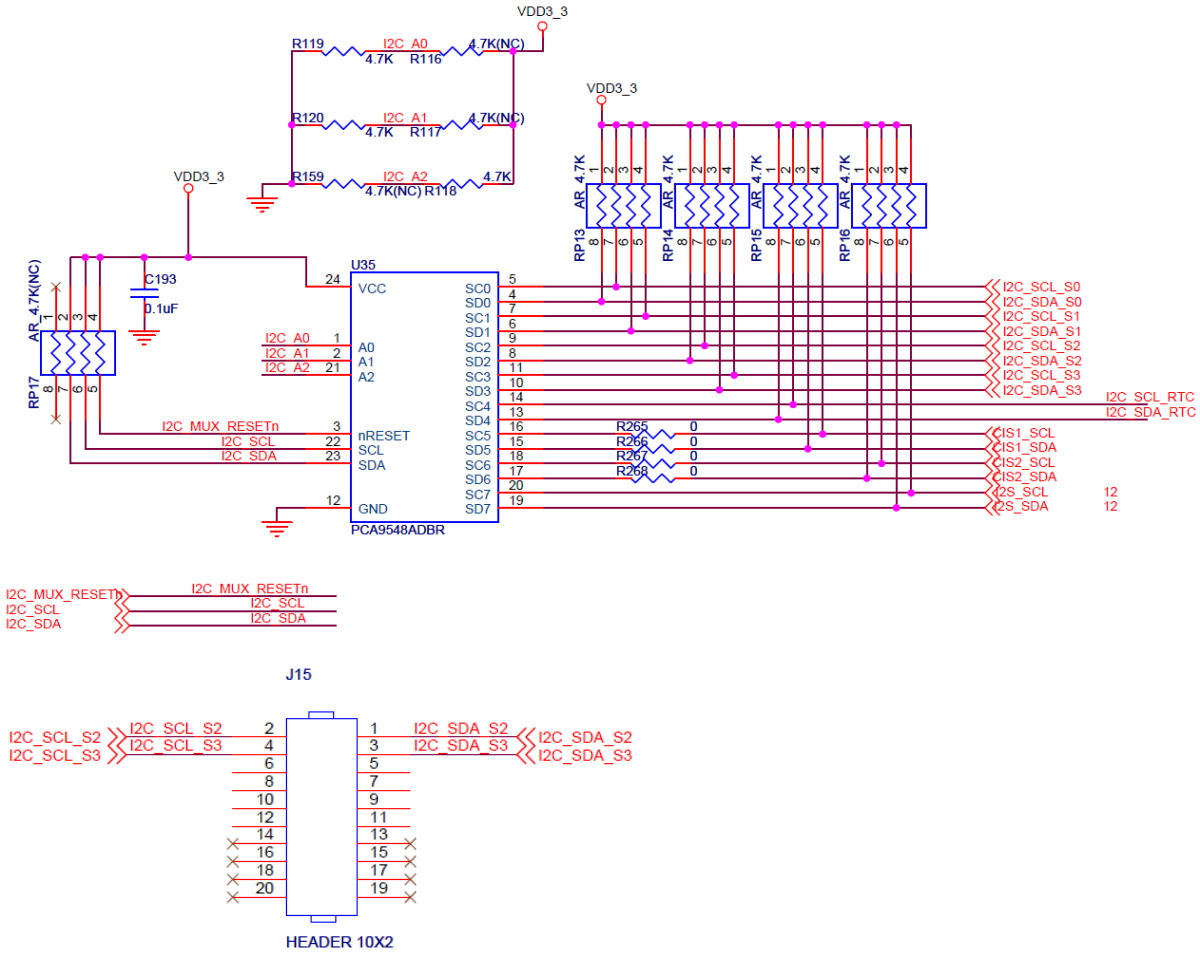
2.11. I2C Connector

I2C 신호는 Zynq PS의 I2C 신호는 I2C MUX 장치인 PCA9548ADBR과 연결되어 있다. 그 MUX는 I2C 인터페이스를 8개로 확장하는데, 그 중의 2개의 인터페이스가 I2C 커넥터와 연결되어 있다. I2C 커넥터는 I2C 인터페이스를 가진 장치를 붙여 사용 가능하다.

I2C_MUX_RESETn은 PS내의 GPIO IP에 의해 출력되고, I2C_SCL, I2C_SDA는 PS내의 I2C IP에 의해 출력된다.



NET	PS Pin	CONNECTOR	Device	IP	MIO
I2C_MUX_RESETn	A6	QTH1-62	U35-3	GPIO	MIO13
I2C_SCL	D13	QTH1-64	U35-22	I2C Ctrl.	MIO50
I2C_SDA	C10	QTH1-66	U35-23	I2C Ctrl.	MIO51

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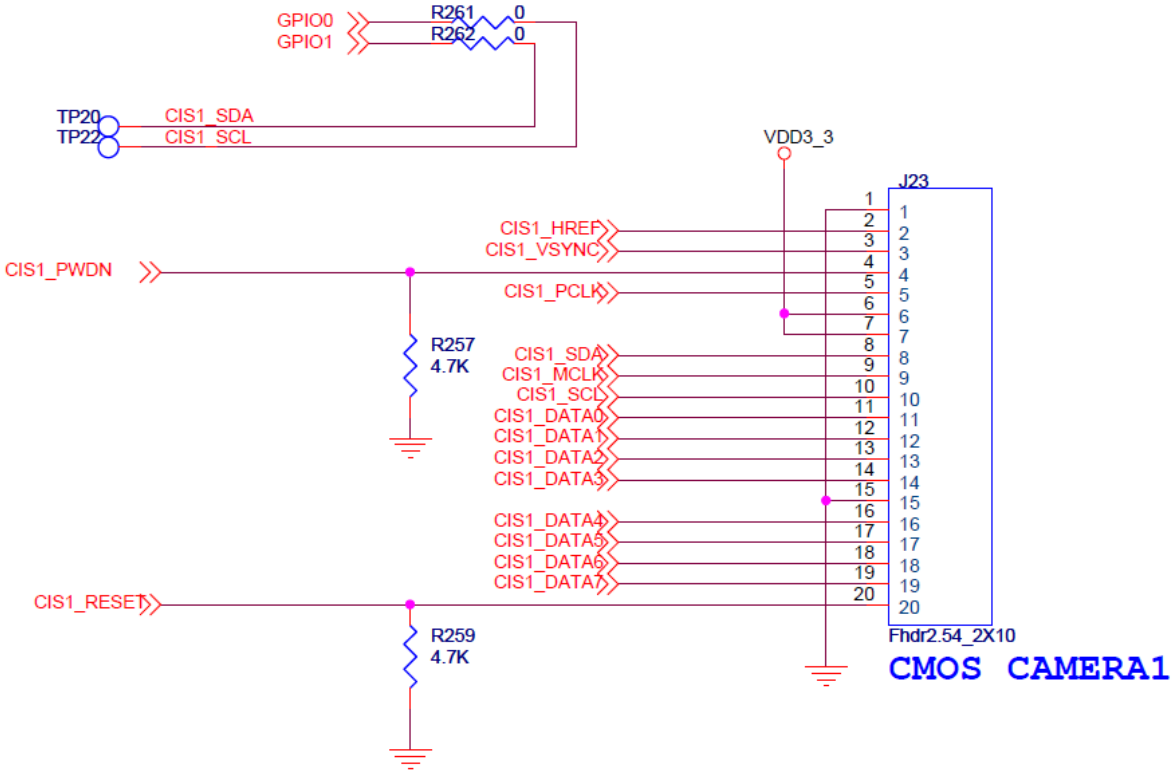
2.12. CMOS camera connector

RPS-Z7020-TK 보드는 8 bits Data Interface를 가진 카메라 Interface 2개를 제공한다. HUINS에서 200만화소 Camera를 추가 구매할 수 있다. I2C 인터페이스로 Camera 동작 설정을 하는데, 예제에서는 PL 영역에서 I2C IP를 구현해서 Camera에 I2C 신호를 넣어 주었다.



NET	PS Pin	CONNECTOR	Device	IP	MIO
FPGA_CL0	F16	QTH2-1	J14-2	GPIO0	35
FPGA_CL1	E16	QTH2-3	J14-4	GPIO1	35
FPGA_CR40	V5	QTH1-34	J23-4	CIS1_PWDN	13
FPGA_CR41	V4	QTH1-36	J23-20	CIS1_RESET	13
FPGA_CR108	W17	QTH1-98	J23-2	CIS1_HREF	33
FPGA_CR109	W18	QTH1-100	J23-3	CIS1_VSYNC	33
FPGA_CR110	W16	QTH1-102	J23-5	CIS1_PCLK	33
FPGA_CR111	Y16	QTH1-104	J23-9	CIS1_MCLK	33
FPGA_CR112	U15	QTH1-106	J23-11	CIS1_DATA0	33
FPGA_CR113	U16	QTH1-108	J23-12	CIS1_DATA1	33
FPGA_CR114	U17	QTH1-110	J23-13	CIS1_DATA2	33
FPGA_CR115	V17	QTH1-112	J23-14	CIS1_DATA3	33
FPGA_CR116	AA17	QTH1-114	J23-16	CIS1_DATA4	33
FPGA_CR117	AB17	QTH1-116	J23-17	CIS1_DATA5	33
FPGA_CR118	AA16	QTH1-118	J23-18	CIS1_DATA6	33
FPGA_CR119	AB16	QTH1-120	J23-19	CIS1_DATA7	33

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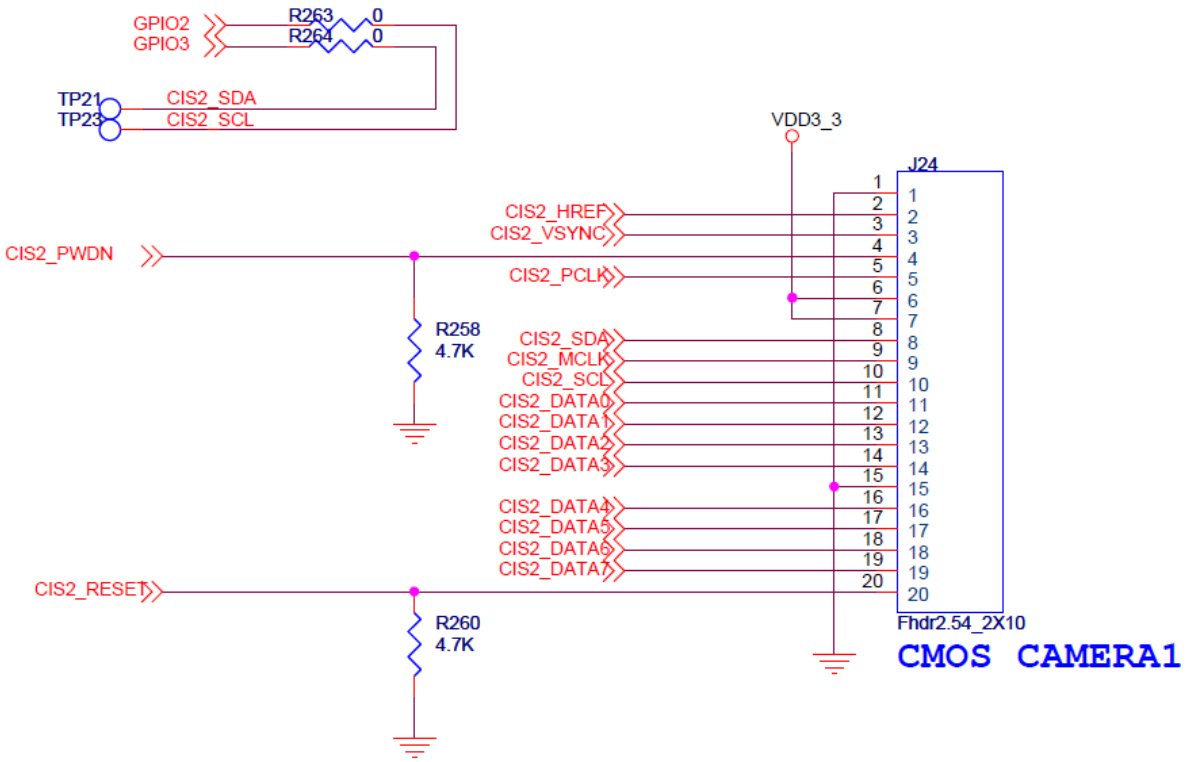

NET	PS Pin	CONNECTOR	Device	IP	MIO
FPGA_CR46	W6	QTH1-46	J24-4	CIS2_PWDN	13
FPGA_CR47	W5	QTH1-48	J24-20	CIS2_RESET	13
FPGA_CR96	Y13	QTH1-97	J24-2	CIS2_HREF	33
FPGA_CR97	AA13	QTH1-99	J24-3	CIS2_VSYNC	33
FPGA_CR98	AB14	QTH1-101	J24-5	CIS2_PCLK	33
FPGA_CR99	AB15	QTH1-103	J24-9	CIS2_MCLK	33
FPGA_CR100	W15	QTH1-105	J24-11	CIS2_DATA0	33
FPGA_CR101	Y15	QTH1-107	J24-12	CIS2_DATA1	33
FPGA_CR102	Y14	QTH1-109	J24-13	CIS2_DATA2	33
FPGA_CR103	AA14	QTH1-111	J24-14	CIS2_DATA3	33
FPGA_CR104	V13	QTH1-113	J24-16	CIS2_DATA4	33
FPGA_CR105	W13	QTH1-115	J24-17	CIS2_DATA5	33
FPGA_CR106	V14	QTH1-117	J24-18	CIS2_DATA6	33
FPGA_CR107	V15	QTH1-119	J24-19	CIS2_DATA7	33

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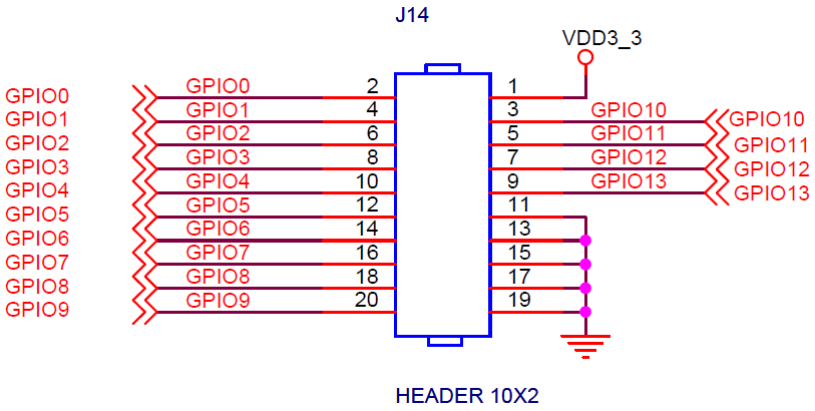
2.13. 14 GPIO Connector

GPIO Connector는 범용으로 사용할 수 있는 Zynq PL 핀이다. 단, GPIO0, GPIO1, GPIO2, GPIO3 핀들은 Camera I2C 인터페이스에 사용되기도 한다.



NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CL0	F16	QTH2-1	J14-2	GPIO0	35
FPGA_CL1	E16	QTH2-3	J14-4	GPIO1	35
FPGA_CL2	D16	QTH2-5	J14-6	GPIO2	35
FPGA_CL3	D17	QTH2-7	J14-8	GPIO3	35
FPGA_CL4	E15	QTH2-9	J14-10	GPIO4	35
FPGA_CL5	D15	QTH2-11	J14-12	GPIO5	35
FPGA_CL82	P20	QTH2-70	J14-14	GPIO6	34
FPGA_CL83	P21	QTH2-72	J14-16	GPIO7	34
FPGA_CL84	N15	QTH2-74	J14-18	GPIO8	34
FPGA_CL85	P15	QTH2-76	J14-20	GPIO9	34
FPGA_CL86	P17	QTH2-78	J14-3	GPIO10	34
FPGA_CL106	V18	QTH2-117	J14-5	GPIO11	33
FPGA_CL107	V19	QTH2-119	J14-7	GPIO12	33
FPGA_CL71	L19	QTH2-95	J14-9	GPIO13	34

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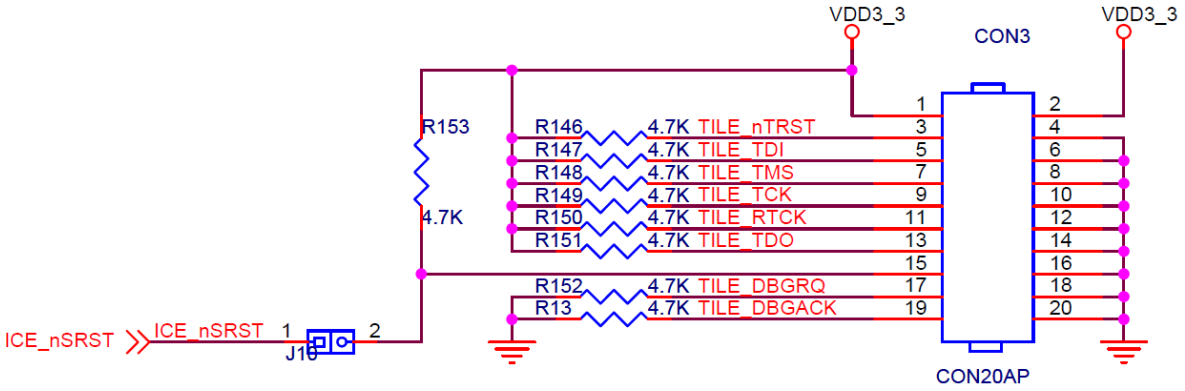
2.14. ARM JTAG connector

ARM JTAG connector는 PS의 Dual Cortex-A9 코어를 D-Stream 장비로 디버깅할 수 있도록 해준다. ICE_nSRST 신호는 RPS-Zynq7000M의 Reset 버튼과 연결되어 있다.



NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CL78	N22	QTH2-62	CON3-5	TILE_TDI	34
FPGA_CL79	P22	QTH2-64	CON3-7	TILE_TMS	34
FPGA_CL80	R20	QTH2-66	CON3-9	TILE_TCK	34
FPGA_CL81	R21	QTH2-68	CON3-13	TILE_TDO	34

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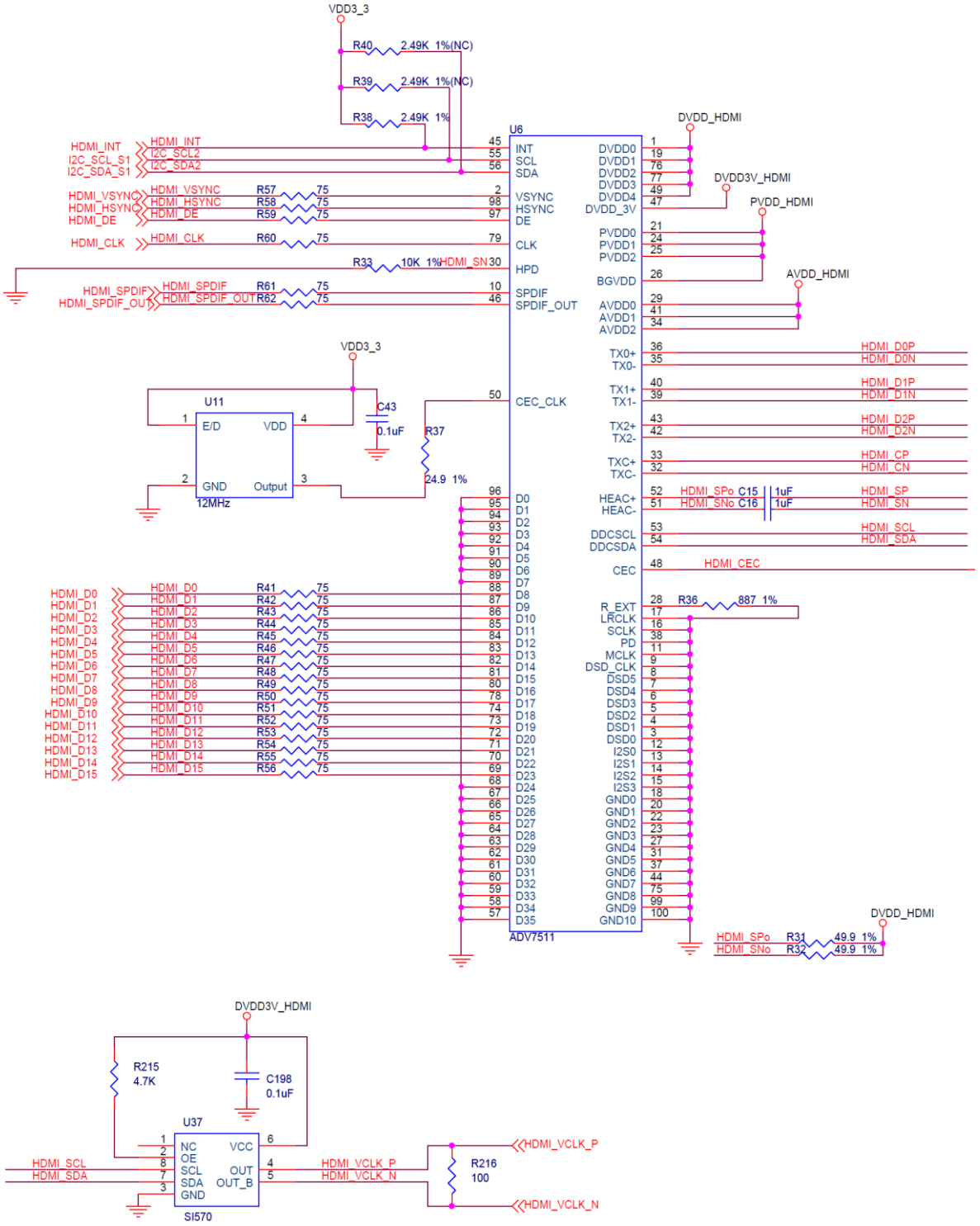
2.15. HDMI output port

HDMI output port를 이용하면, HDMI Interface가 있는 모니터에 영상을 출력시킬 수 있다.



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NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CL73	M20	QTH2-52	U6-46	HDMI_SPDIF_OUT	34
FPGA_CR0	V10	QTH1-1	U6-88	HDMI_D0	13
FPGA_CR1	V9	QTH1-3	U6-87	HDMI_D1	13
FPGA_CR2	V8	QTH1-5	U6-86	HDMI_D2	13
FPGA_CR3	W8	QTH1-7	U6-85	HDMI_D3	13
FPGA_CR4	W11	QTH1-9	U6-84	HDMI_D4	13
FPGA_CR5	W10	QTH1-11	U6-83	HDMI_D5	13
FPGA_CR6	V12	QTH1-13	U6-82	HDMI_D6	13
FPGA_CR7	W12	QTH1-15	U6-81	HDMI_D7	13
FPGA_CR8	U12	QTH1-17	U6-80	HDMI_D8	13
FPGA_CR9	U11	QTH1-19	U6-78	HDMI_D9	13
FPGA_CR10	U10	QTH1-21	U6-74	HDMI_D10	13
FPGA_CR11	U9	QTH1-23	U6-73	HDMI_D11	13
FPGA_CR12	AA12	QTH1-25	U6-72	HDMI_D12	13
FPGA_CR13	AB12	QTH1-27	U6-71	HDMI_D13	13
FPGA_CR14	AA11	QTH1-29	U6-70	HDMI_D14	13
FPGA_CR15	AB11	QTH1-31	U6-69	HDMI_D15	13
FPGA_CR16	AB10	QTH1-33	U6-45	HDMI_INT	13
FPGA_CR17	AB9	QTH1-35	U6-2	HDMI_VSYNC	13
FPGA_CR18	Y11	QTH1-37	U6-98	HDMI_HSYNC	13
FPGA_CR19	Y10	QTH1-39	U6-97	HDMI_DE	13
FPGA_CR20	AA9	QTH1-41	U6-79	HDMI_CLK	13
FPGA_CR21	AA8	QTH1-43	U6-10	HDMI_SPDIF	13
FPGA_CR22	Y9	QTH1-45	U37-4	HDMI_VCLK_P	13
FPGA_CR23	Y8	QTH1-47	U37-5	HDMI_VCLK_N	13

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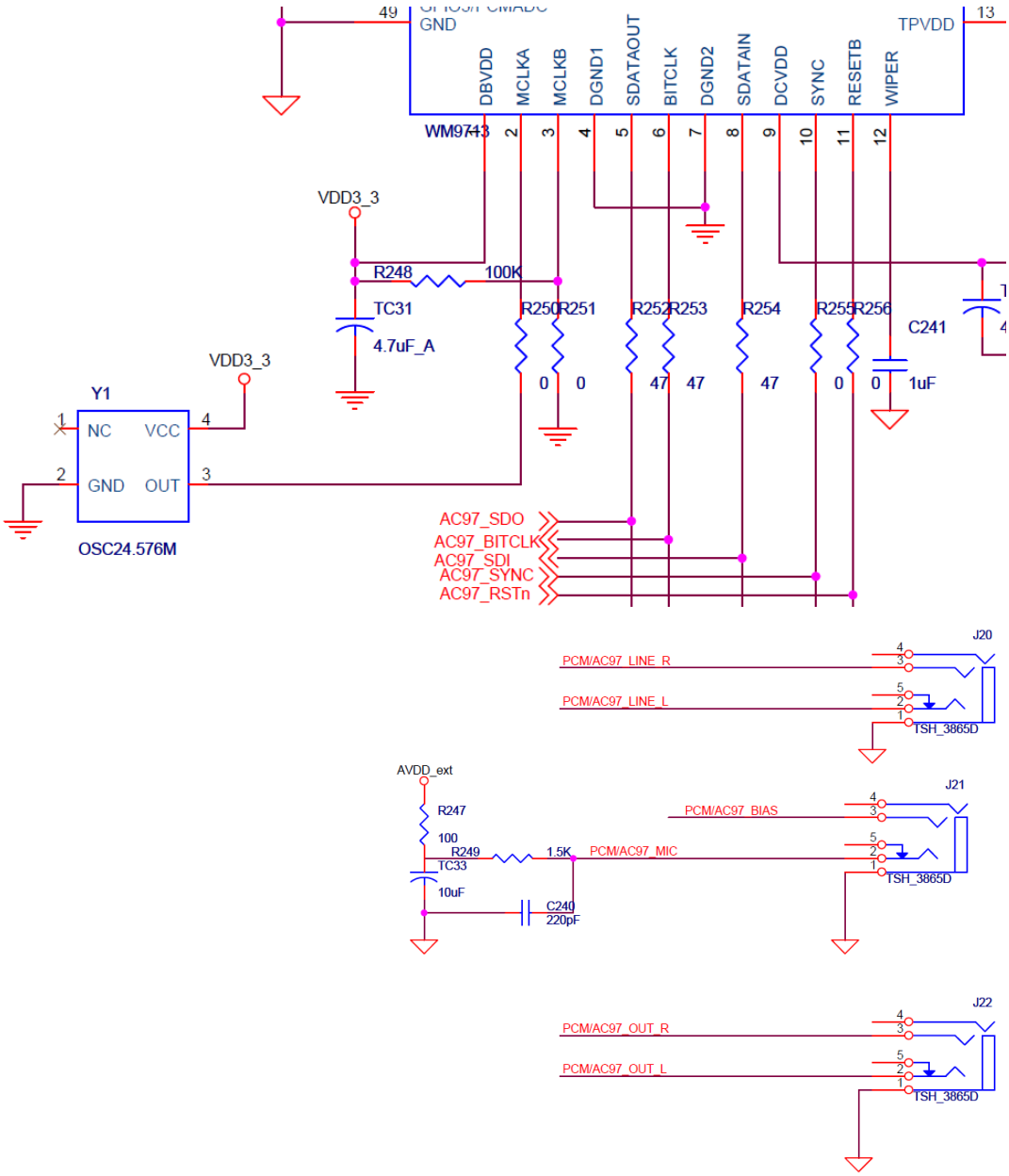
2.16. Audio port

Audio Codec은 AC97 인터페이스를 가진 WM9713 칩을 사용한다. RPS-Z7020-TK 보드는 2개의 Audio 출력 포트와 1개의 Audio 입력 포트를 포함한다.



NET	PL(FPGA) Pin	CONNECTOR	Device	Signal Name	BANK
FPGA_CL24	B19	QTH2-2	U40-11	AC97_RSTn	35
FPGA_CL25	B20	QTH2-4	U40-10	AC97_SYNC	35
FPGA_CL26	D20	QTH2-6	U40-8	AC97_SDI	35
FPGA_CL27	C20	QTH2-8	U40-6	AC97_BITCLK	35
FPGA_CL28	A21	QTH2-10	U40-5	AC97_SDO	35

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