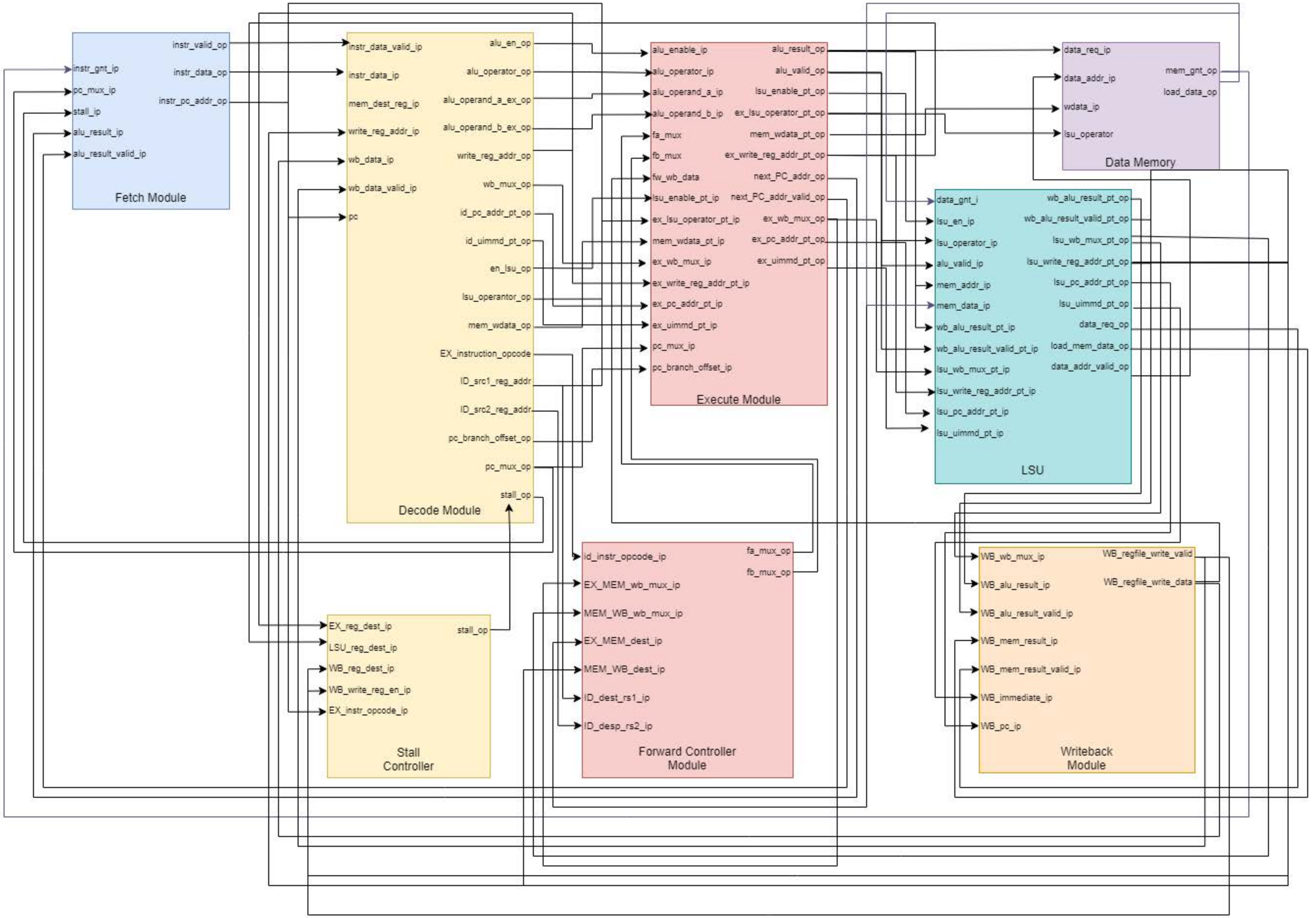
Jose Johnson



Design Task 2

Consider the following instructions on a pipelined processor. Explain why the add will have an issue and what possible solutions could be used to solve the issue.

	3	4	5	6	7	8	9	10	11	12	13	14	15	16
lw $2, 0	F	D	E	M	WB									
lw $3, 0x4		F	D	E	M	WB								
add $1, $2, $3			F	D	E	[illegible]	WB							

The add will cause issues due to the need of the data in register $3, which is currently being retrieved from data. To solve this, we can stall the pipeline until the register $3 holds the data needed to continue the program's execution.