ECE 3058
Architecture, Systems, Concurrency, and Energy in Computation
Lab 4: Virtual Memory

Acronym Table

Acronym	What it actually means
VA	Virtual Address
VPN	Virtual Page Number
PA	Physical Address
PPN	Physical Page Number
PT	Page Table
PTE	Page Table Entry
PCB	Process Control Block
PID	Process ID

Questions

Question 1 (4 pts)

At work this week you sat in on an engineering meeting. In this meeting they discussed a cache that has the following specifications:

- Cache Line Size = 8 Bytes
- Number of sets = 8
- Number of ways per set = 2 (i.e., 2-way set associative cache).

Additionally, you know that the target machine is byte-addressed, has a page size of 256 bytes, and uses 16-bits for both virtual and physical addresses. What is the size of this cache?

Cache Size = 8*8*2 = 128 bytes

Question 2 (6 pts)

Use the system described in Question 1 to answer the following questions.

(a) What is the value of A from the following diagram? [3 pts]

A = 7

(b) What is the value of B from the following diagram? [3 pts]

B = 7

Question 3 (4 pts)

Recall that a virtual address is interpreted as:

A page table is a structure that holds VPNs and maps them to their corresponding PPNs. Given the following specifications, what is the size of this process's page table?

- Virtual and Physical addresses are 16 bits. 2^4
- Page Sizes are 64 Bytes. 2^6
- Each Page Table Entry is 2 bytes (16-bits) wide.

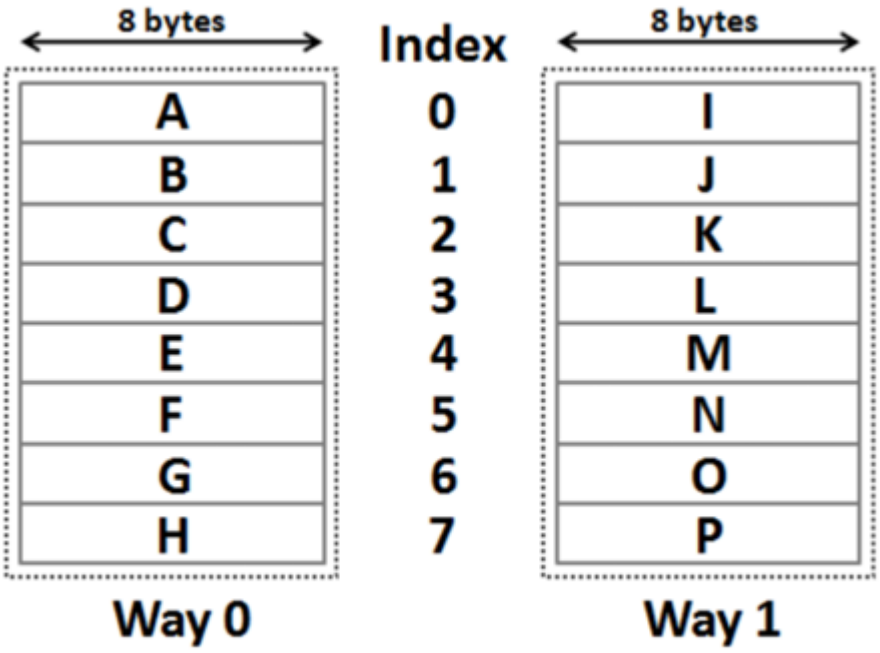
Page Table Size = 2048 B => 2KB

6 bits for the offset, 16 - 6 = 10 bits for the VPN.
The number of pages is 2^10 = 1024
1024 * 2 bytes => 2048 | 2KB

Question 4 (6 pts)

Given the following information, fill out the table at the bottom.

Consider the cache your coworkers described in question 1. Suppose we label the 16 cache lines from A to P, as shown in the figure below. Recall that our cache is 2-way set associative and the cache line size is 8 bytes.



Cache Configuration

A program wants to read from virtual address 0x6E, but the corresponding physical address is unknown (could be arbitrary). Enumerate all entries (A,B,C,D,...) that can possibly hold the content of the virtual address 0x6E, for each given page size in the next table.

Hint: the page offset bits remain the same in the virtual and physical addresses.

0x6E => 0110 1110

TAG | INDEX | OFFSET

2^4 01 XX1 110

2^5 01 X01 110

2^6 01 101 110

Page Size	Line(s) to which VA 0x6E can be mapped to	
16 bytes	B, J, D, L, F, N, H, P	index = 1, 3, 5, 7
32 bytes	B, J, F, N	Index = 1, 5
64 bytes	F, N	Index = 5