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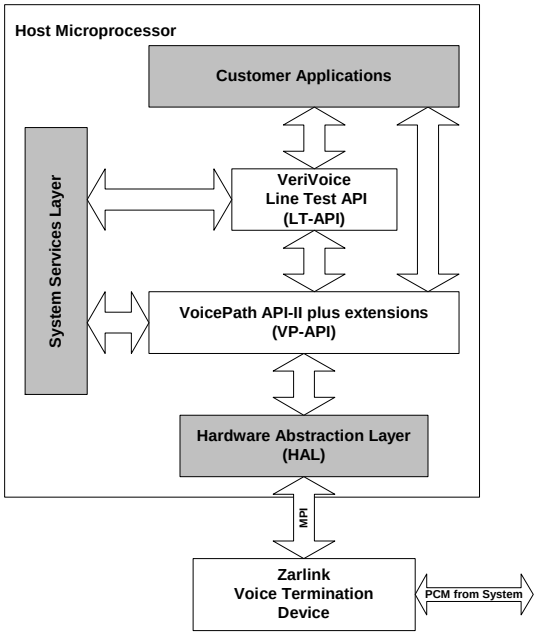
Features

- VeriVoice™ Professional Test Suite
  - Returns Pass/Fail and quantitative results with user defined thresholds to the limits specified by Telcordia GR-909-CORE, Section 12.4
  - Additional inward and outward tests including Line Capacitance and Master Socket detection
  - No Math Libraries required
  - Extension of established Zarlink VoicePath™ API-II line control software interface

Applications

- Line Testing for:
  - Fiber to the Premise/Home (FTTP/H)
  - Voice Enabled Cable Modems (EMTA)
  - Integrated Access Devices (IAD)
  - Residential VoIP Gateways and Routers
  - Wireless Local Loop (WLL), PBX
  - Set-Top Boxes

Figure 1 - Block Diagram



Description

In combination with Zarlink's VE890 Series products, Zarlink's VeriVoice™ Test Suite—a subscriber line test software package for VoIP equipment—provides the market's most cost-effective and reliable solution for VoIP line and self test, minimizing the cost of ownership for service providers.

VoIP service providers are expected to provide traditional carrier class voice quality and reliability to consumer equipment in a wide geographical distribution. The automated, remote testing capability of the VeriVoice™ Test Suite eliminates the need for costly truck rolls, which minimizes maintenance costs, improves reliability of service, and decreases the mean time to repairs. In addition, VeriVoice™ software removes any requirement to include expensive test equipment inside the low line count VoIP equipment.

The VeriVoice Test Suite software currently consists of two distinct test packages corresponding to two different levels of coverage. The VeriVoice Auditor package consists of outward looking line tests, while the VeriVoice Professional package consists of both outward looking line tests and inward looking self tests. The outward looking tests, or drop tests, are intended to check the customer equipment and copper pair leading to it while the inward looking self tests check the VoIP equipment itself.

With Zarlink's VeriVoice Test Suite software, service providers can reduce their cost of ownership while improving the reliability of their network at the same time.

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1.0 Product Description

Zarlink's VeriVoice™ Test Suite is a C-language extension of the libraries provided in the VoicePath™ API-II (VP-API-II). The VeriVoice™ test libraries and the VP-API-II are typically compiled into the customer's application, all of which runs on a host processor controlling one or more Zarlink Voice Termination Devices (VTDs). Refer to the Block Diagram on page 1.

This VeriVoice Professional Test Library is available for the VE890 series FXS devices.

VeriVoice Auditor is available upon signing a licence agreement. Access is then granted to Zarlink's software distribution system where the package may be downloaded.

VeriVoice Professional is available upon purchase and signing a licence agreement. Access is then granted to Zarlink's software distribution system where the package may be downloaded.

1.1 VeriVoice Professional Test Library

The VeriVoice Professional Test Library returns Pass/Fail based on user defined thresholds and quantitative results with accuracies similar to what is required in the line test section of Telcordia GR-909-CORE, Section 12.4 for Locally Switched Services. The Professional library returns Pass/Fail results in accordance with the limits specified by GR-909-CORE, Section 12.4.2. The Professional package adds several more tests which also return quantitative results where appropriate.

The Professional package is specified to work with loop length up to 3 kft.

The VeriVoice Test Libraries offer the following key features:

- Convenient, single-function call implementation of line test
- One common line testing interface for different Zarlink devices
- ANSI C compliant source code
- Supports different line circuit topologies
- Automatic pass/fail determination
- Portable - can be ported to any operating system or a non-operating system platform

2.0 System Architecture

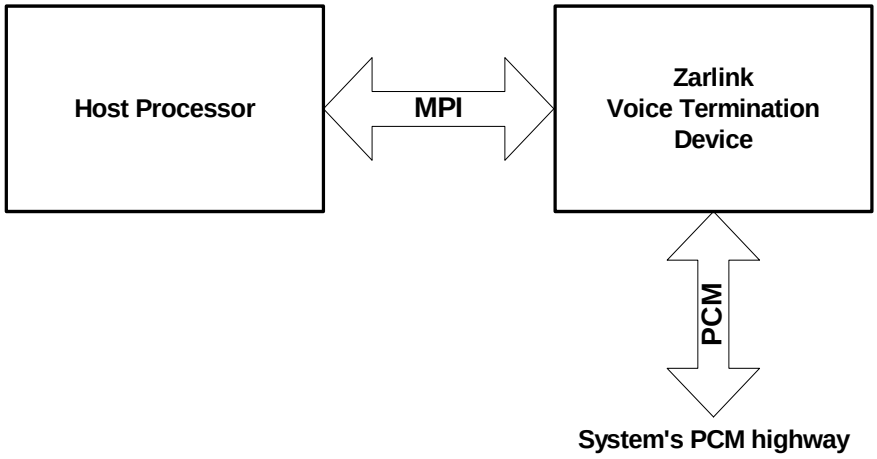
The VeriVoice Test Libraries are flexible to support a range of potential applications and enable the end user to select the most efficient means of data collection for the specific system architecture. The VE890 Series devices will measure test data and route it to the PCM highway or an MPI register.

2.1 Simple System Controller Architecture

In the configuration shown in Figure 1, the host processor acquires the test data from MicroProcessor Interface (MPI) reads (EZ Mode). The VE890 Series devices are configured to route data samples at a periodic rate to a register that can be read via MPI transactions. All data acquisition, storage and manipulation is done by the Host Processor.

In order to use EZ Mode and still meet the required 500 Hz sampling rate for VeriVoice measurements, the VP-API-II VpApiTick() function must be called at a minimum of 10 ms intervals in narrowband or 5 ms intervals in wideband sampling mode.

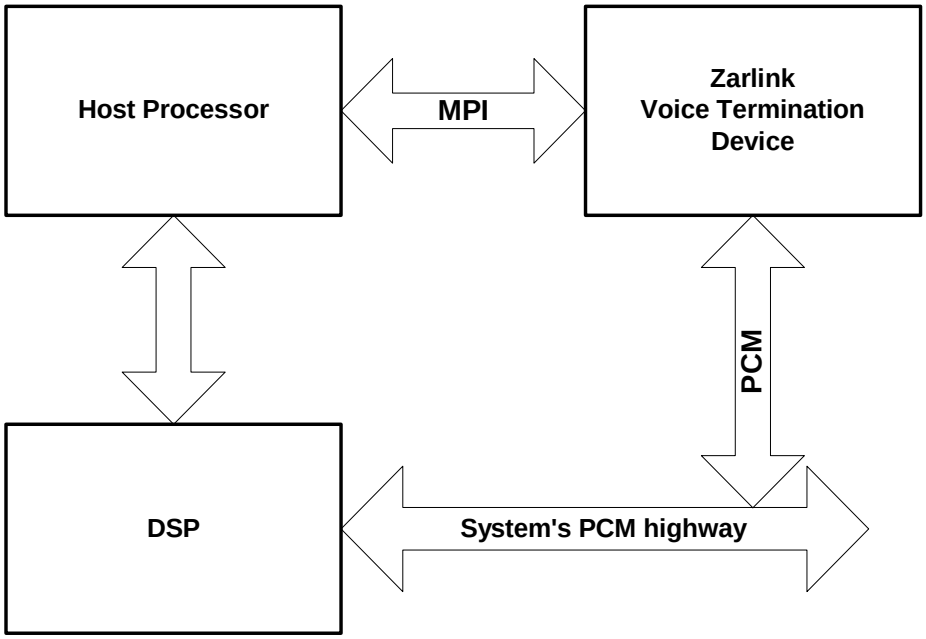
Figure 1 - Simple System Controller Architecture



2.2 System Configuration Architecture that Enables Data Collection from the PCM Highway

The configuration shown in Figure 2 contains a DSP. The DSP has direct access to the VE890 Series devices and collects test data from the PCM highway. The advantage of collecting the test data from the PCM highway compared to collecting it via the MPI bus is that the sampling rate on PCM bus is at least 8 kHz compared to typically 500 Hz on the MPI bus. The DSP is not needed if the host processor can collect data directly from the PCM highway.

Figure 2 - System Configuration Architecture that Enables Data Collection from the PCM Highway



The VeriVoice test libraries are based on the Zarlink Line Test Application Programming Interface (LT-API). The LT-API provides an abstracted function prototype named **VpSysPcmCollectAndProcess ()** that allows the user to define the method by which the test data is acquired. All tests in the Auditor or Professional packages assume the existence of this function and can run regardless of the topology in use. The interface specification for the LT-API is included in both the Auditor and the Professional packages.

3.0 Software Architecture

Refer to the *Block Diagram*, on page 1.

3.1 Customer Applications

This block represents user's line management module that performs task such as system initialization, configuring lines, service events, line testing, and any other customer specific complex operations.

3.2 Operating System

This block represents the operating system running on the host microprocessor. The Zarlink software does not directly utilize any operating system resources. However, depending of the user's application the developer may wish to use operating system specific features. For more information, please see the VP-*API-II Reference Guide*.

3.3 System Services Layer

The System Services Layer abstracts platform-specific functions. This layer derives the functions required by the VP-API-II and the LT-API from the facilities provided by the underlying hardware or operating system. This layer is platform dependent and it is implemented by the customer. Zarlink provides implementation examples of this layer with the VeriVoice software package.

There are three functions specified as part of the System Services Layer to enable these tests.

Scratch pad memory allocation and release functions:

- **VpSysTestHeapAcquire ()**
- **VpSysTestHeapRelease ()**

Test Data Acquisition and Conditioning:

- **VpSysPcmCollectAndProcess ()**

This function is not needed if the system can meet the tick rate requirements for EZ Mode operation. See *Simple System Controller Architecture*, on page 3

3.3.1 Hardware Abstraction Layer

This layer is required by the VP-API-II which is a prerequisite to run the VeriVoice Test packages. The Hardware Abstraction Layer (HAL) provides a means for the host processor to communicate with the Zarlink voice termination devices via the Micro Processor Interface (MPI). The HAL software is also platform dependent and must be implemented by the customer. Zarlink provides implementation examples of this layer with the VoicePath API-II software package.

3.3.2 Line Test Library and VoicePath API

The Line Test Library and the VP-API-II source codes are supplied by Zarlink, and should not be modified by the application developer. The customer application accesses the line testing resources through the LT-API. It also accesses the VP-API-II to implement call control and other line management functions.

3.4 Supported Hardware Configurations

Table 1 - LT-API Supported Devices

Device, VP-API Name	Supported Line Termination Types	Supported Devices
VP_DEV_890_SERIES	*VP_TERM_FXS_GENERIC* *VP_TERM_FXS_LOW_PWR* *VP_TERM_FXS_ISOLATE* *VP_TERM_FXS_ISOLATE_LP* *VP_TERM_FXS_SPLITTER* *VP_TERM_FXS_SPLITTER_LP*	VE890 Series • VE8911 • VE8910 • VE8911-HV • VE8910-HV

The following hardware configurations are supported (refer to Figure 3, on page 7):

3.4.1 Circuit Configuration "C1" PTC Isolation

API termination types –
VP_TERM_FXS_GENERIC, VP_TERM_FXS_LOW_PWR

The advantage of these configurations is low cost and good performance within the battery voltage range. The disadvantages are that the subscriber loop is never fully isolated from the SLIC drivers and the over voltage protection. For a fault that is significantly out of the battery range, the PTC will go to a high impedance state, at which point a voltage measurement can be made at the TIP and RING terminals. The measurement made at the TIp/Ring interface depends on the relative impedances of the foreign voltage source and the activated PTC. See Note 1. of *Test Range and Accuracy with Circuit Configuration C1 and C2.*, on page 9.

3.4.2 Circuit Configuration "C2" Relay Isolation of the Sense Path

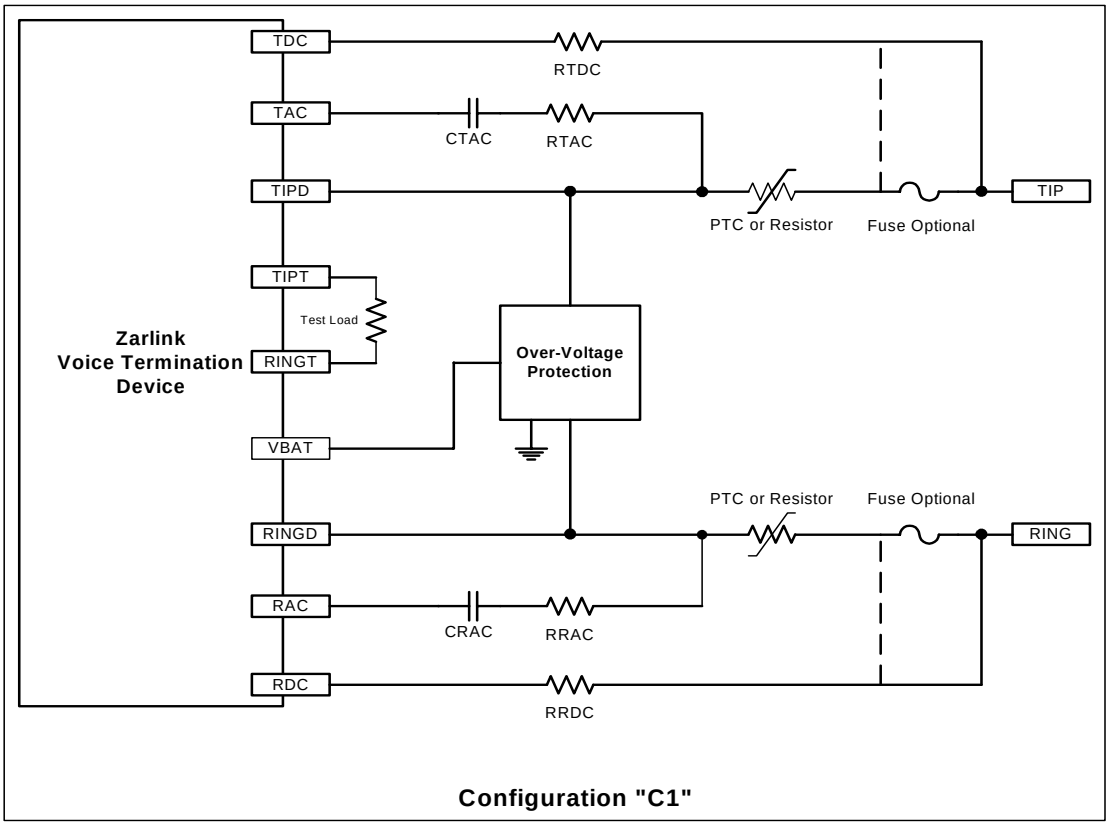
API termination types –
VP_TERM_FXS_ISOLATE, VP_TERM_FXS_ISOLATE_LP
VP_TERM_FXS_SPLITTER, VP_TERM_FXS_SPLITTER_LP

The advantage of this configuration is better foreign voltage testing accuracy. In this configuration, the subscriber loop is fully isolated from the SLIC drivers and the over voltage protection by a relay. This meets CR12-193 of GR-909-CORE.

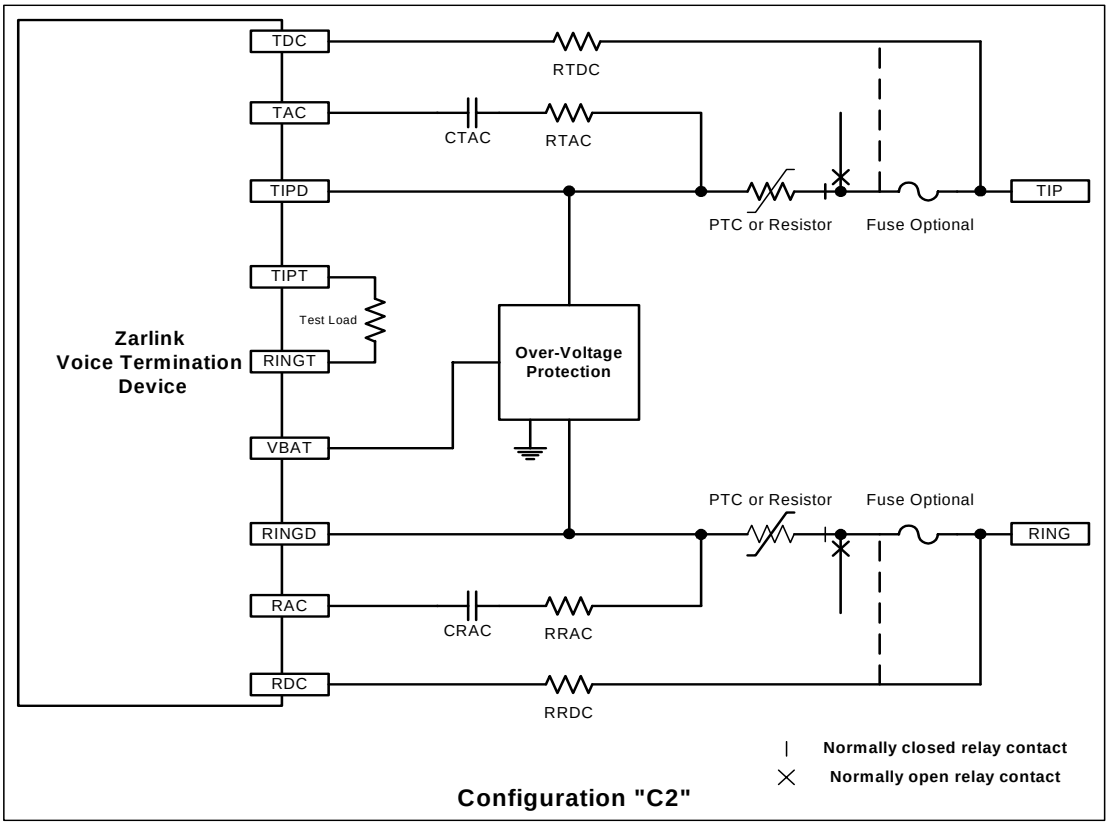
The diagram in Figure 3, on page 7 represents the *ISOLATE* and *ISOLATE_LP* configuration, where the normally closed contacts of the relay connect the line driver outputs to Tip and Ring. During the line voltage test, the relay is energized to disconnect the line from the protection and line driver outputs to allow a high impedance measurement.

For the *SPLITTER* and *SPLITTER_LP* configurations, the normally open contacts of the relay connect the line driver outputs to Tip and Ring. This supports an application where it is required to keep the line isolated during initialization, and only activate the relay at some later time. In this case, during the line voltage test, the relay is de-energized to disconnect the line from the protection and line driver outputs to allow a high impedance measurement.

Figure 3 - Configurations C1 and C2



Configuration "C1"



Configuration "C2"

NOTE: VE890 series devices offer internal test termination but no external test load.

4.0 Verivoice™ Software Package

The package contains the following: The Line Test Library source code, The *Line Test API Reference Guide defining the interfaces,* Source example code for **VpSysPcmCollectAndProcess ()**

5.0 Test Coverage

Two distinct test packages correspond to two different levels of coverage.

Table 2 - Test Coverage for the VeriVoice Auditor and Professional Packages

Test Procedures	Test Packages and OPNs		
	VeriVoice™ Auditor (Le880SLVV and Le890SLVV)	VeriVoice™ Professional (Le880SLVVP and Le890SLVVP)	Description
OUTWARD TESTS			
Line Voltage	Pass/Fail	Pass/Fail with measured results	Checks for hazardous and foreign AC and DC voltages on the drop
Receiver Off-Hook	Pass/Fail	Pass/Fail with measured results	Tests for longitudinal fault, off hook resistive fault and receiver off hook.
Ringer Equivalence Number (Regular)	Pass/Fail T-R	Measures REN impedance Pass/Fail with measured results T-R, R-G and T-G	Tests the impedance of the line and returns a fail if the T-R REN is too low or high.
Ringer Equivalence Number (Electronic)	Not Included	Measures ringer capacitance Pass/Fail with measured results T-R, R-G and T-G	Tests the capacitance of the line and returns a fail if the T-R REN is too low or high.
Resistive Fault Test	Pass/Fail	Pass/Fail with measured results	Measures three element resistance
Capacitance Test	Not Included	Measured results	Measures three element capacitance
Master Socket Test	Not Included	Pass/Fail	Detect master socket terminations
Cross Connect Test	Not Included	Pass/Fail	Detect cross connected FXS
All GR-909 Tests	Pass/Fail	Pass/Fail with measured results	Performs all GR-909 outward tests in the correct sequence.
INWARD TESTS			
Loopback	Not included	Pass/Fail	Enables Receive to Transmit signal loopback. Assumes test signal is applied on the Receive PCM highway from an outside source.
Read Loop Conditions	Not included	Measured results	Measures Battery, T-R, R-G and T-G voltage and metallic and longitudinal current
Read Battery Conditions	Not included	Pass/Fail with measured results	Reads the battery voltages connected to the line circuit.
DC Voltage Self-Test	Not included	Pass/Fail with measured results	Verifies that the line circuit has the ability to drive the voltage ranges required for the normal operation of the line circuit.
DC Feed Self-Test *	Not included	Pass/Fail with measured results	Measures the voltage and current across a known test termination using the DC feed profile that has been programmed.
Ringing Self-Test *	Not included	Pass/Fail with measured results	Verifies ring signal generation, drive capability, and ring trip.
On/Off Hook Self-Test *	Not included	Pass/Fail	Creates on-hook and off-hook conditions on the line using the test termination and verifies that they are properly reported.

Note: *Tests requiring test termination supported with Internal Test Termination on Le88266, VE8820, VE8830 or VE890 series devices. External test load or internal test termination can be used on Le88276 and Le88286 devices. External test load required on Le88231 or Le88241 devices.

6.0 Specifications

6.1 Test Range and Accuracy with Circuit Configuration C1 and C2.

The VeriVoice™ Professional Test Suite returns Pass/Fail and quantitative results with user-defined thresholds

Test Description/Test ID Used	Range		Unit	Accuracy	Note
Line Voltage Test - LT_TID_LINE_V	-240	-6	Vdc	±10 %	1., 2.
	-6	+6	Vdc	±0.6 V	
	+6	+240	Vdc	±10 %	
	0	10	Vrms	1 Vrms	1., 3.
	10	165	Vrms	±10 %	
	165	250	Vrms	±15 %	
Receiver Off-Hook Test - LT_TID_ROH LT_ROHM_OFF_HOOK loop range	0	1300	Ω	PASS / FAIL	4., 5.
LT_ROHM_RES_LOOP	0	1500	Ω	±15 %	
Ringer Equivalence Number Test LT_TID_RINGERS (REGULAR) Tip to Ring	0.0	0.175	REN	0.0175	6.
	0.175	6.0	REN	±10 %	
Ringer Equivalence Number Test LT_TID_RINGERS (REGULAR) Tip or Ring to Ground	0.0	0.5	REN	0.05	6.
	0.5	6.0	REN	±10 %	
Ringer Equivalence Number Test LT_TID_RINGERS (ELECTRONIC) Tip to Ring	0.0	0.5	REN	±0.050	6.
	0.5	6.0	REN	±10 %	
Ringer Equivalence Number Test LT_TID_RINGERS (ELECTRONIC) Tip or Ring to Ground	0.0	0.5	REN	0.05	6.
	0.5	6.0	REN	±10 %	
Resistive Faults Test - LT_TID_RES_FLT Tip to Ring	0.1	150	KΩ	±10 %	7.
	150	500	KΩ	±20 %	
	500	1000	KΩ	±40 %	
Resistive Faults Test - LT_TID_RES_FLT Tip or Ring to Ground	0.5	20	KΩ	±10 %	7.
	20	40	KΩ	±20 %	
	40	150	KΩ	±10 %	
	150	500	KΩ	±20 %	
	500	1000	KΩ	±40 %	
Capacitance Test - LT_TID_CAP Tip to Ring	0	1200	nF	±3 nF & +/-10%	8.
Capacitance Test - LT_TID_CAP Tip or Ring to Ground	0	1200	nF	±3.5 nF & +/-10%	9., 10. 11.
Read Loop Conditions - LT_TID_RD_LOOP_COND Voltage measurements, vab, vag, vbg, vbatx	-100	-10	Vdc	±10 %	
	-10	+10	Vdc	±1.0 V	
	+10	+100	Vdc	±10 %	
Read Loop Conditions - LT_TID_RD_LOOP_COND Current measurements, imt, ilg	-20	+20	mA	+/-2 mA	
	-40	+40	mA	+/-10 %	
Read Loop Conditions - LT_TID_RD_LOOP_COND Resistance measurement, rloop	0	100	Ω	+/-25 Ω	
	0.1	25	kΩ	+/-25 %	

The VeriVoice™ Professional Test Suite returns Pass/Fail and quantitative results with user-defined thresholds

Test Description/Test ID Used	Range		Unit	Accuracy	Note
LT_TID_RD_BAT_COND - Read Battery Conditions	-150	-25	V	±10 %	
LT_TID_DC_VOLTAGE DC Voltage Self-Test	-140	-6	V	±10 %	12.
	-6	+6	Vdc	±0.6 V	
	+6	+140	V	±10 %	
LT_TID_DC_FEED_ST DC Feed Self-Test - external test load resistance	1	1	KΩ	±15%	
DC Feed Self-Test - Internal test termination current Accuracy relative to programmed ILA	20	45	mA	±10%	
LT_TID_RINGING_ST - Ringing Self-Test				Pass/Fail	
Ringing Frequency	14	55	Hz	±10%	
Ringing Voltage	6	50	Vrms	±10%	13.
External Test Load Resistance	1	1	KΩ	±15%	
Ringing Current	5	60	mArms	±10%	14.
LT_TID_ON_OFF_HOOK_ST On/Off Hook Self-Test				Pass/Fail	
LT_TID_LOOPBACK - Loopback Test	0.0	16.0	s	Pass/Fail	
LT_TID_MSOCKET - Master Socket Detection				Pass/Fail	15.
LT_TID_XCONNECT - Detection of PSTN Cross Connection				Pass/Fail	

Note:

1. *The test range and accuracy criteria is for Configuration C2. Protection devices in Configuration C1 will limit the range of measurement if the foreign voltage has a high impedance, and the test results might not represent the actual source voltage.*
2. *Due to reference voltages generated from the VTD driving the line through the sense network, a voltage of 1.5 volts will be read on an unloaded loop in configuration C2. Configuration C1 will read in the range of a few hundred millivolts due to the positive voltage protection diode.*
3. *AC foreign voltage measurements assume a sinusoidal signal at a frequency of either 50 or 60 Hz.*
4. *For off hook loops beyond the specified ranges, the test may not be able to determine if there is an off hook phone. These conditions will be reported with an LT_ROHM_OUT_OF_RANGE_LOOP fault mask.*
5. *In the presence of longitudinal currents that would compromise the measurement, the test will return LT_ROHM_MSRMNT_STATUS with EXCESSIVE_ILG error.*
6. *The regular REN test measures the AC impedance at 20 Hz and uses 2408 Ω + 1.21 μF as 1 REN by default. The electronic REN test measures ringer capacitance and assumes 1 REN = 1.21 μF. These values are derived from the requirements for a REN load specified in FCC part 68. Use of input conditions other than the default values may degrade measurement accuracy.*
   When performing 3 element tests, up to 1% of the value measured on one lead may add to the value returned on the other two leads
7. *When a resistive fault below the pass criteria is measured, only the lowest value lead is reported, The other leads are reported as "impedance not measured". Resistance to ground measured below 500 Ω is reported as a short circuit.*
8. *For Tip to Ring capacitance, an additional error term of +/-0.5 % of the measured Tip or Ring to ground capacitance can be present.*
9. *For Tip or Ring to ground capacitance, the accuracy defined assumes that the contribution of the on board capacitance to ground due to the SLIC and EMI capacitors are calibrated out of the result. This can be achieved by obtaining open circuit tip and ring to ground measurements during production and applying these values to subsequent tests. If this calibration is not performed, the EMI capacitance (nominally 22 nF) and SLIC capacitance (typically 10 nF, but can vary with device type) will be part of the result, and accuracy will be reduced*

directly proportional to the EMI capacitor tolerance and SLIC capacitance variance (+/-2 nF).

10. *An additional error term of +/-2 % of the measured Tip to Ring capacitance can be present on either leg to ground.*
11. *Up to 0.5 % of the capacitance measured on one lead can appear as an error term on the other lead to ground.*
12. *The maximum voltage that can be generated is limited by the programmed ringing voltage in fixed ringing applications.*
13. *To avoid ringing the telephone, a low voltage ring profile with DC offset should be used.*
14. *Ringing current measured depends on the load, test voltage and ringing current limit. When using the internal test termination, the expected current is calculated from this data and used as a pass/fail condition instead of the external test load resistance.*
15. *Master Socket Test (LT_TID_MSOCKET) is capable of detecting Type 1 (470 kΩ + diode) and Type 2 (470 kΩ + 1.8 υF capacitor) M-Sockets. Valid detection is possible when the total leakage (Rtr || Rtg || Rrg) resistance is >= 150 kΩ as shown in Figure 4 and Figure 5. The test passes if the specified master socket is identified, and in the case of Type 1, is in the correct polarity. Type 1 master socket has additional fault mask values including not present, reversed, and two networks in parallel,*

Figure 4. M-Socket (Type 1)

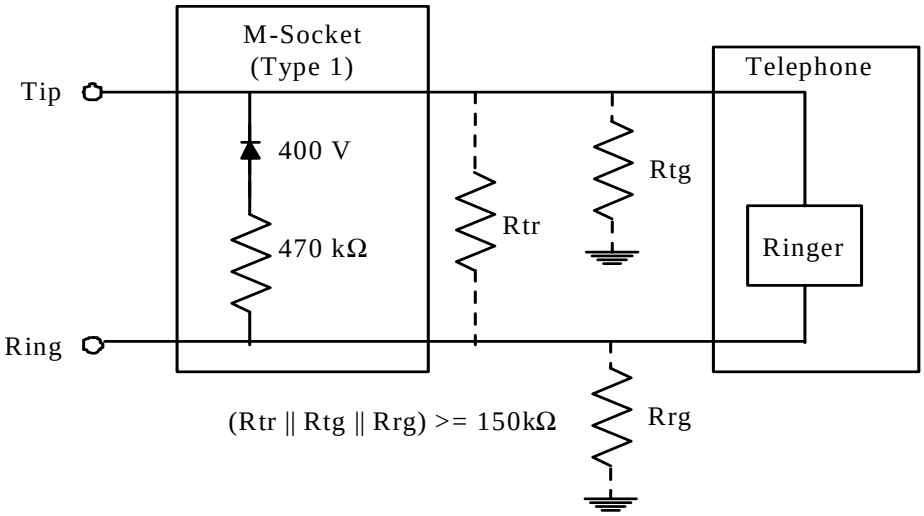
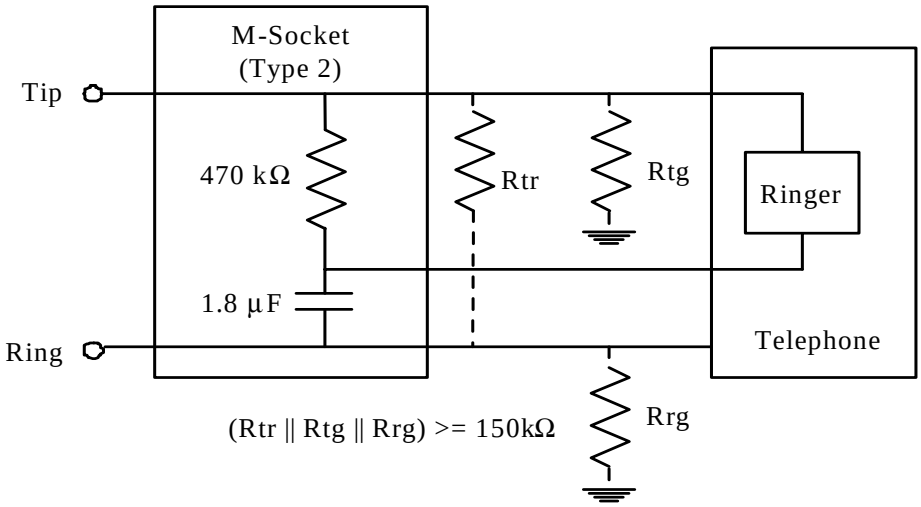


Figure 5. M-Socket (Type 2)



16. *Cross connect test verifies the absence of a cross connection to another FXS line. If a cross connection is detected, the test fails and returns the polarity of the cross connection.*

6.2 Default Pass/Fail Criteria and Accuracy

For tests with programmable pass fail criteria.

Test Description	Pass Criteria	Accuracy of Pass/ Fail Threshold	Note
Line Voltage Test LT_TID_LINE_V Hazardous EMF	|V(T-G)| < 135 VDC	± 10 %	1., 2.
	|V(R-G)| < 135 VDC	± 10 %	
	|V(T-R)| < 135 VDC	± 10 %	
	V(T-G) < 50 Vrms	± 10 %	1., 2.
	V(R-G) < 50 Vrms	± 10 %	
	V(T-R) < 50 Vrms	± 10 %	
Line Voltage Test LT_TID_LINE_V Foreign EMF	V(T-G) < 10 Vrms	± 10 %	1., 2.
	V(R-G) < 10 Vrms	± 10 %	
	V(T-R) < 10 Vrms	± 10 %	
	|V(T-G)| < 6 VDC	± 10 %	1., 2.
	|V(R-G)| < 6 VDC	± 10 %	
	|V(T-R)| < 6 VDC	± 10 %	
Ringer Equivalence Number Test LT_TID_RINGERS (REGULAR) - Tip to Ring	0.175 < REN(T-R) < 5.0	± 10 %	3.
Ringer Equivalence Number Test LT_TID_RINGERS (ELECTONIC) - Tip to RING	0.175 < REN(T-R) < 5.0	Greater of +/- 0.05 REN or ± 10 %	3.
Resistive Faults Test LT_TID_RES_FLT	R(T-G) > 150 KΩ	± 10 %	
	R(R-G) > 150 KΩ	± 10 %	
	R(T-R) > 150 KΩ	± 10 %	
DC Voltage Self-Test - LT_TID_DC_VOLTAGE	56 V	± 10 %	4.
All GR 909	All tests are performed		5.

Note:

1. *The pass/fail and accuracy criteria is for Configuration C2. Protection devices in Configuration C1 will limit the range of measurement if the foreign voltage has a high impedance, and the test results might not represent the actual source voltage.*
2. *Any type of foreign voltage failure will leave the line circuit in the Disconnect state at the end of the test. For Configuration C2, the line relay will be in the Reset state, disconnecting Tip/Ring from the line driver.*
3. *The regular REN test measures the AC impedance at 20 Hz and uses 2408 Ω + 1.21 μF as 1 REN by default. The electronic REN test measures ringer capacitance and assumes 1 REN = 1.21 μF. These values are derived from the requirements for a REN load specified in FCC part 68. Use of input conditions other than the default values may degrade measurement accuracy.*
   When performing 3 element tests, up to 1 % of the value measured on one lead may add to the value returned on the other two leads
4. *For the pass/fail threshold, the generated voltage requested is assumed to have up to an additional ±3.6 V offset.*
5. *All outward tests except capacitance are performed to individual test limits.*

6.3 VeriVoice™ Professional Outward Test Suite Typical Timings

Test Description	Test Time Generic, Isolate or Splitter Termination Types	Test Time Low Power Termination Types	Note:
Line Voltage AC, DC, EMF and frequency	1460 ms	1440 ms	2.
Receiver Off-Hook or Resistive Loop:	740 ms	770 ms	
Ringer Equivalence (Regular)	990 ms	1170 ms	
Ringer Equivalence (Regular, 3 Element)	2790 ms	3030 ms	
Ringer Equivalence (Electronic)	1610 ms	1780 ms	
Ringer Equivalence (Electronic, 3 Element)	3580 ms	3750 ms	
Resistive fault - High Resistance	2960 ms	3052 ms	2.
Resistive fault - Low Resistance	1620 ms	1480 ms	2.
Capacitance	2440 ms	2560 ms	
Master Socket Detection, Type 1	3050 ms	2940 ms	
Master Socket Detection, Type 2	3460 ms	3830 ms	
Cross Connect Detection	530 ms	700 ms	
All GR 909	5320 ms	5440 ms	

Note:

1. *The Timing in the above table is based on 10 ms API tick rate and 2 ms (500 Hz) PCM collection rate in Narrowband mode. On-hook tests initiated from the Standby system state, off-hook from the Talk state.*
2. *Test time is determined by the resistive and capacitive load applied to tip-ring. Small or large resistances in conjunction with larger capacitive loads will take longer to settle and auto range to the appropriate gain settings. High resistance means test ran only using low gain range. Low resistance means test used the high gain range to obtain a result. For resistive faults, a 5 REN load as specified in note 3. can increase test time up to 8 seconds. With a 5 REN load as described in GR909 (1396 Ω + 40 μF) the test time can be further increased to 10 seconds, and accuracy can be degraded for high resistance loads.*

6.4 VeriVoice™ Professional Inward Test Suite Typical Timings

Test Description	Test Time Generic, Isolate or Splitter Termination Types	Test Time Low Power Termination Types	Note:
DC Feed Self-Test (48 V)	730 ms	940 ms	3.
DC Voltage Self-Test	1610 ms	1830 ms	4.
Loopback test	150 ms	150 ms	5.
On/Off Hook Self-Test	270 ms	630 ms	3.
Read Battery Conditions	450 ms	620 ms	6.
Read Loop Conditions	460 ms	320 to 460 ms	7.
Ringing Self-Test	1980 ms	2160 ms	3.

1. *The Timing in the above table is based on 10 ms API tick rate and 2 ms (500 Hz) PCM collection rate in Narrowband mode. On-hook tests initiated from the Standby system state, using internal test termination where necessary.*
2. *Low Power termination types typically add 120 ms to each test.*
3. *Ringing, DC Feed and On/Off Hook self-tests use internal test termination to implement these tests.*
4. *Duration dependent on input voltage parameter.*
5. *Time is the test setup overhead. Need to add the user programmable wait time and loopback time, each of which can be up to 8 s, and be in an active state (OHT, Active or Talk). Four loopback types can be enabled, TIMESLOT, BFILTER, CODEC and ANALOG.*
6. *Read battery Conditions exits low power standby for Low Power Termination types before making the measurement.*
7. *Test time depends on the system state and the number of parameters measured.*

7.0 Ordering Information

Device	Package
Le890SLVVP	VeriVoice Professional Test Software Library

8.0 Related Literature

- **081535 VeriVoice™ Test Suite Software Product Preview**
- **081301 VoicePath™ API-II CSLAC Reference Guide for VE790, VE880 and VE890 Series Devices**
- **081470 Line Test Application Programming Interface**
- **081560 VE890 Series - VE8911 1 FXS + 1 FXO Chipset Data Sheet**
- **081575 VE890 Series - VE8910 1FXS Chipset Data Sheet**
- **135302 VE890 Series - VE8911-HV 1 FXS + 1 FXO Chipset Data Sheet**
- **135264 VE890 Series - VE8910-HV 1FXS Chipset Data Sheet**
- **129850 Reference Design User's Guide for Le71HR8921G**
- **135594 Reference Design User's Guide for Le71HR8922G**
- **136022 Reference Design User's Guide for Le71HR8923G**

9.0 System Requirements

- Two contiguous PCM highway timeslots for 16-bit linear data per channel under test
- Channel under test must be in linear mode
- Data Acquisition of 16-bit linear words must be done at a 2 ms rate or faster. Options are:
  - Use EZ-Mode with an appropriate tick rate. This collects data from the MPI interface using one of two methods:
    1. Read by MPI access of the devices' Test Data Buffer which returns 14 bytes, or up to 6 samples. Test Data Buffer requires a corresponding tick rate of 10 ms or less for narrowband operation, or 5 ms or less for wideband operation.
    2. Read by MPI access of the devices' XDAT register which returns one, 2 byte sample. Tick rate must be 2 ms.
  - Implement the **VpSysPcmCollectAndProcess ()** system service function, and collect the data from two contiguous timeslots on the PCM highway.
- 32-bit fixed point arithmetic implementation
  - Floating point libraries are not required
- Battery Voltage Requirements - VE890 Series devices
  - Ringing Battery must be at least 75 V
- Code memory size approximately 165 kB
  - As compiled by GCC 3.4.5 for an ARM 920T
  - Includes base API-II Lite plus test extensions (127 kB) and LT-API interface (38 kB)
- Data memory requirements
  - An additional 380 bytes to each existing API device object
  - 604 bytes for each LT-API object

10.0 Revision History

10.1 Version 1 to 2

- Included additional termination types in *Supported Hardware Configurations,* on page 6
- Added limits for Receiver Off Hook test return values, adjusted limits for the read loop conditions and resistive faults test on page 9
- Added and updated various notes to the specifications on page 12

10.2 Version 2 to 3

- Added FXS_ISOLATE_LP termination type support
- Added and updated various notes to the specifications on page 12
- Updated Outward test timings, including low power termination type support on page 13
- Updated Inward test timings, including low power termination type support on page 13
- Updated code and memory size estimates on page 15

10.3 Version 3 to 4

- Clarified the requirements for EZ Mode operation vs. **VpSysPcmCollectAndProcess ()** in *Simple System Controller Architecture,* on page 3 and *System Requirements,* on page 15
- Added new 3 element capacitance test - see *Specifications,* on page 9 supported in P1.1 or later
- Added support for internal test termination, enabling inward tests requiring a test termination to be run. See *Test Range and Accuracy with Circuit Configuration C1 and C2.,* on page 9. Supported in P1.1 or later
- Rearranged and updated various notes on the specifications, see notes on page 10 and page 12
- Added support for VE890-HV devices. Some of the test ranges have been expanded to allow the full capability of the high voltage devices to be used.
- Updated test timings on page 13 for P1.1
- Updated related literature to reference VE890-HV high voltage datasheets on page 14
- Updated code and memory size estimates on page 15 for P1.1

10.4 Version 4 to 5

- Add new Master Socket and Cross Connect tests supported in P1.2 or later
- Added BFILTER and TIMESLOT loopback test options (see note 5.) supported in P1.2 or later
- Improved test times for most tests, especially worst case 909 ALL test - see *VeriVoice™ Professional Outward Test Suite Typical Timings,* on page 13 for P1.2
- Updated code size information in *System Requirements,* on page 15 for P1.2

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