

K. J. Somaiya College of Engineering, Mumbai-77

(A Constituent College of Somaiya Vidyavihar University) **Department of Computer Engineering**



Course Name:	Digital Design Laboratory	Semester:	III
Date of	17 / 10 / 2023	Batch No:	B2-2
Performance:	1771072023		
B2-2Faculty Name:	Mrs. Bharathi H N	Roll No:	16010122151
Faculty Sign &		Grade/Marks:	/25
Date:		Graue/Marks:	123

Experiment No: 8

Title: 1-bit adder on VHDL

Aim and Objective of the Experiment:
To implement 1-bit adder on VHDL
COs to be achieved:

Tools used:

Quartus, ModelSim

CO4: Implement digital networks using VHDL

Theory:

A 1-bit adder, a fundamental component of digital circuits, performs binary addition of two 1-bit numbers. It utilizes logic gates to generate the sum and carry-out outputs. A half-adder adds two bits without considering the carry from the previous stage, while a full-adder accounts for the carry input. Using VHDL, a hardware description language, the 1-bit adder can be designed as a combinational circuit. VHDL facilitates the creation of a structural and behavioral description of the adder. In practice, this simple unit serves as a building block for constructing larger multi-bit adders, enabling arithmetic operations in microprocessors and digital systems.

Implementation Details		

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1
                  library IEEE;
            2
                  use IEEE.std logic 1164.all;
            3
                mentity Onebitadder is
                mort (num1, num2, carryin : in std_logic;
            4
            5
                  Sum, Carryout : out std logic);
            6
                  end Onebitadder;
            7
                marchitecture behavior of Onebitadder is
            8
                  signal S1, S2, S3 : std logic;
            9
                begin
          10
                  Sum <= num1 xor num2 xor carryin;
          11
                  S1 <= num1 and num2;
                  S2 <= num1 and carryin;
          12
          13
                  S3 <= carryin and num2;
                  Carryout <= S1 or S2 or S3;
          14
          15
                  end behavior;
                                                    Simulation Report - Simulation Waveforms | 🕅 Waveform2.vwf
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nebitadder.vhd
                 Compilation Report - Flow Summary onebitadder.vwf
                     Page Title: onebitadder
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  Hierarchy List
   onebitadder
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    □ Primitives

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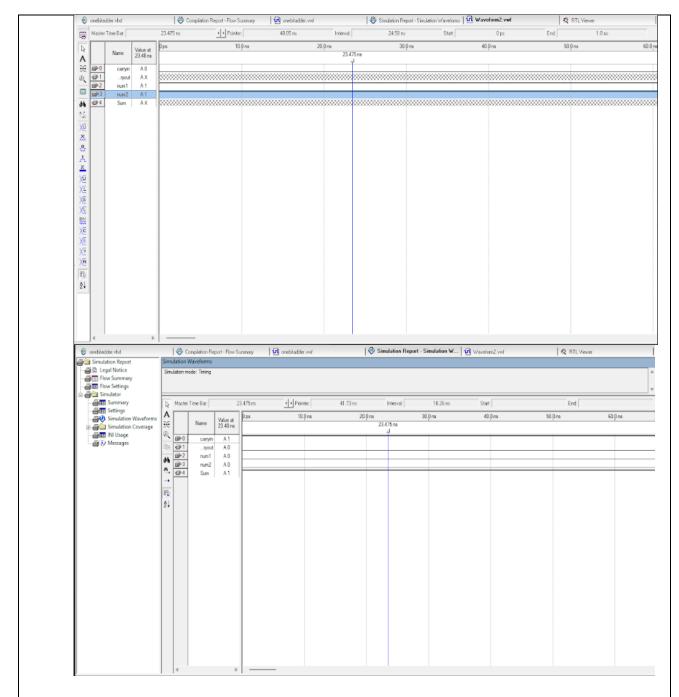


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Post Lab Subjective/Objective type Questions:

1. How can 1-bit adder be used to implement a 4-bit adder?

Ans) A 1-bit adder can be used to implement a 4-bit adder by cascading four 1-bit adders together to perform addition on 4-bit binary numbers. Each 1-bit adder is responsible for adding one bit of the input numbers, and the carry-out from one stage is propagated to the carry-in of the next stage. This creates a ripple-carry adder.

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2. What is VHDL used for?

Ans) Digital Circuit Design: VHDL is commonly used to describe and design digital circuits, including combinatorial logic circuits (e.g., multiplexers, decoders) and sequential logic circuits (e.g., flip-flops, state machines). Designers use VHDL to create models of digital circuits, simulate their behavior, and synthesize them into actual hardware.

Simulation: VHDL is used for simulating digital circuits before they are physically implemented. Designers can use VHDL to create testbenches and verify the functionality of their designs. This helps catch errors and bugs early in the design process.

Verification and Testing: VHDL can be used to create testbenches and test vectors to verify the correctness and performance of digital designs. It allows for thorough testing and debugging of digital systems.

Education: VHDL is a valuable teaching tool in electronics and digital design courses, helping students understand the concepts of digital logic and design.

Research and Prototyping: Researchers in the field of electronics and digital design use VHDL to prototype and experiment with novel digital designs, as it provides a standardized and rigorous way to describe hardware behavior.

Conclusion:
In this experiment, we learned to implement 1-bit adder on VHDL

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Signature of faculty in-charge with Date:

Academic Year: 2023-24

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