2-12-2023 (E)

SOMAIYA VIDYAVIHAR UNIVERSITY

Semester: July 2023 –October 2023		Duration:3 Hrs.
Maximum Marks: 100 Examination: ESE Examination		
Programme code: 01 Programme: B Tech Computer Engineering	Class: SY	Semester:III (SVU 2020)
Name of the Constituent College: K. J. Somaiya College of Engineering	Name of the department: COMP	
Course Code: 116U01C303	Name of the Course: Computer Organization & Architecture	

Instructions: 1)Draw neat diagrams 2) All questions are compulsory
3) Assume suitable data wherever necessary

Que. No.	Question	Max. Marks
Q1	Solve any **Four**	20
i)	List the functions of I/O Module for interaction with peripherals and CPU.	5
ii)	What will be contents of register PC and SP after execution of **CALL function1** instruction? Assume suitable values for contents of registers and address of label "function1"	5
iii)	Explain following features of PCI Bus • Burst transfers for better data Transfer rate • Hidden Bus Arbitration	5
iv)	Explain Bit pair recoding of Booth Multiplier with suitable example	5
v)	Discuss Memory Hierarchy in Computer Systems	5
vi)	Explain how BCD numbers are added with example as **19 + 25** (by Representing these numbers in BCD)	5

Que. No.	Question	Max. Marks
Q2 A	Solve the following	10
i)	Explain tasks performed by CPU for instruction execution with a neat diagram	5
ii)	For the register set of intel X86 family explain specific function of each of following register CX,CS, IP, SI and Flags	5
	OR	
Q2 A	Explain restoring Division Algorithm and solve **37 / 13** using binary representations of these numbers using the same	10
Q 2 B	Solve any **One**	10
i)	Explain with neat diagram basic components in IAS architecture with its functionality	10
ii)	Draw the formats for single precision and double precision. Represent 0.00635 in single precision and in double precision format.	10

Que. No.	Question	Max. Marks
Q3	Solve any **Two**	20
i)	With reference to Virtual Memory implementation write whether following are true or false and justify your answer with suitable explanation • Virtual memory address generated by processor gives reference to page frame in page table.	10

	• Translation Lookaside buffer helps in reducing memory references • Page fault is a tool used by the Memory Management Unit for getting pages from secondary storage devices. • Main memory pages are copy of Secondary storage • LRU replacement algorithm can be applied to page replacement	
ii)	A two-way set-associative cache has lines of 16 bytes and a total size of 8 kB. The 64-MB main memory is byte addressable. Show the format of main memory addresses. Show cache organization with a neat diagram. Comment on Look up penalty when compared with 4 way set associative cache.	10
iii)	Explain write policy used in cache memory	10

Que. No.	Question	Max. Marks
Q4	Solve any **Two**	20
i)	Explain following parameters considered in designing Instruction Format of a microprocessor. • Addressing Modes • number of Operands • Registers • Address range	10
ii)	With neat diagram explain Microprogrammed Control Unit and its functions	10
iii)	Explain the term RAID Explain all possible RAID levels, with neat diagrams and examples.	10

Que.	Question	Max. Marks
Q5	Write notes on any **four**	20
i)	MESI Protocol with possible situations for state changes	5
ii)	Interrupt driven I/O mechanism and its advantages.	5
iii)	Hazards in Pipelining	5
iv)	Data transfer techniques used in DMA	5
v)	Analyze 2 level memory hierarchy with following specifications Calculate Average access time,	5
vi)	Explain following Instructions of X86 1. MOV AX, BX 2. MOV [SI],CX 3. DIV CL 4. PUSH BX 5. CALL N1	5

	Cache Memory (M1)	Main Memory (M2)
Size	4K	64K
Hit ratio	0.9	
Access time	10 ns	110 ns