27-11-2018 (E)

K. J. Somaiya College of Engineering, Mumbai-77
(Autonomous College Affiliated to University of Mumbai)

End Semester Exam
Nov – Dec 2018

Max. Marks: 100 | **Duration: 3 Hrs**
Class: S.Y.B.Tech | Semester: III
Name of the Course: Computer Organization and Architecture | Branch: COMP
Course Code: UCEC304

Instructions:
(1) All Questions are Compulsory
(2) Draw neat diagrams
(3) Assume suitable data if necessary

Question No.		Max. Marks
Q 1 (a)	Define computer organization and computer architecture. Draw a neat diagram with explanation of the expanded structure of IAS computer developed by Von Neumann.	10
Q 1 (b)	Represent $(-0.001750)_{10}$ in single precision and in double precision format.	10
Q2 (a)	What are the advantages of Booth's recoding algorithm over Booth's algorithm? Solve (9)*(6) using Booth's recoding algorithm.	10
Q2 (b)	Explain restoring division method for signed numbers. Hence perform (-7)/(-3).	10
Q3 (a)	What is cache coherence problem? How it is overcome by using MESI protocol in uniprocessor and multiprocessor system?	10
Q3 (b)	What is memory interleaving? Compare and contrast its types.	10
Q4 (a)	List and explain registers of 8086.	10
Q4 (b)	Write the microprogram for ADD R1,(R3). Explain significance of each step along with the role of register involved.	10
	OR	
Q4(a)	Draw instruction cycle state diagram. Explain execution of instruction in detail.	10
Q4(b)	Explain different methods to design control unit of computers. Differentiate between them.	10
Q5 (a)	Explain programmed I/O. What are two modes of addressing of programmed I/O?	10
Q5 (b)	What are pipeline hazards? How to avoid them?	10
	OR	
Q5(a)	What is an Interrupt? What processor does if an interrupt occurs? Explain Interrupt driven I/O?	10
Q5(b)	What is pipelining? Discuss various design issues of pipeline architecture.	10