

(A Constituent College of Somaiya Vidyavihar University) **Department of Computer Engineering**



Course Name:		Digital Design Laboratory	Semester:	III	
Date	of	21/ 08 /_23	Batch No:	B-2	
Performance:		21_ / 00 / _23	Daten 140.	D- 2	
Faculty Name:			Roll No:	16010122151	
Faculty Sign	&		Grade/Marks:	/25	
Date:			Graue/Marks:		

Experiment No: 4

Title: 4-bit magnitude comparator

Aim and Objective of the Experiment:

To design and implement 1-bit comparator using logic gates and verify 4-bit magnitude comparator using IC 7485

COs to be achieved:

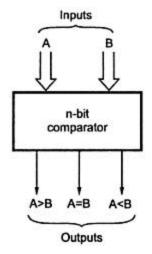
CO2: Use different minimization techniques and solve combinational circuits.

Tools used:

Trainer kits

Theory:

Comparator: The comparison of two numbers is an operator that determines one number is greater than, less than (or) equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers A and B and determines their relative magnitude. The outcome of the comparator is specified by three binary variables that indicate whether A>B, A=B (or) A<B.



Semester: III

Academic Year: 2023-24

Roll No:_____



(A Constituent College of Somaiya Vidyavihar University) **Department of Computer Engineering**



1-bit Comparator Implementation Details:

Truth Table

Inp	out	Output			
A	В	YA=B	YA>B	YA <b< td=""></b<>	
0	0	1	0	0	
0	1	0	0	1	
1	1	0	1	0	
1	1	1	0	0	

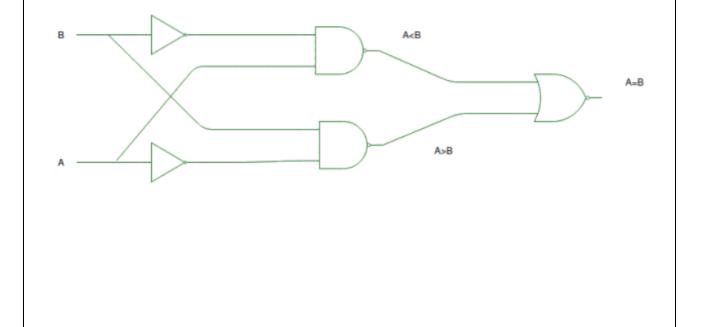
From the Truth Table:

$$(A < B) = A'B$$

$$(\mathbf{A} = \mathbf{B}) = \mathbf{A}'\mathbf{B}' + \mathbf{A}\mathbf{B}$$

$$(A>B) = AB'$$

Logic Diagram of 1-bit Comparator



Semester: III

Digital Design Laboratory

Academic Year: 2023-24

Roll No:_____

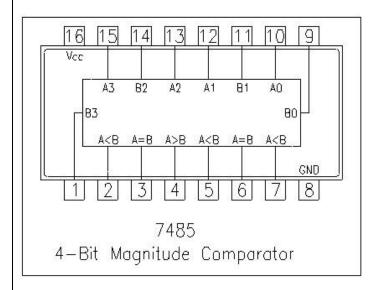


(A Constituent College of Somaiya Vidyavihar University) **Department of Computer Engineering**

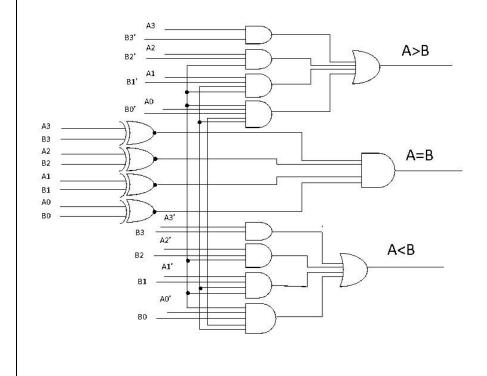


Four Bit Magnitude Comparator Implementation Details

Pin Diagram of IC 7485



Logic Diagram of IC 7485



Semester: III

Academic Year: 2023-24

Digital Design Laboratory

Roll No:____



(A Constituent College of Somaiya Vidyavihar University) **Department of Computer Engineering**



Comparing Table

INI	PUTS of 4 k	OUTPUT				
A3, B3	A2, B2	A3, B3	A2, B2	A3, B3	A2, B2	A3 B3
A3 > B3	X	X	X	H	L	L
A3 < B3	X	X	X	L	н	L
A3 = B3	A2 > B2	X	X	Н	L	L
A3 = B3	A2 < B2	X	X	L	Н	L
A3 = B3	A2 = B2	A1 > B1	X	Н	L	L
A3 = B3	A2 = B2	A1 < B1	X	L	Н	L
A3 = B3	A2 = B2	A1 = B1	A0 >B0	н	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	L	Н	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	н	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	Н	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	Н

Where H = High Output, L = Low Output, X = Don't Care

Implementation Details

Procedure:

- 1) Locate the IC 7485 on the trainer kit.
- 2) Connect 1st input no. to A3-A0 input slot and 2nd to B3-B0.
- 3) Connect the output $Y_{A>B}$, $Y_{A< B}$ and $Y_{A=B}$ to the output indicators.
- 4) Switch ON the power supply and monitor the output for various input combinations.

Semester: III Academic Year: 2023-24
Roll No:_____



(A Constituent College of Somaiya Vidyavihar University) **Department of Computer Engineering**



Post Lab Subjective/Objective type Questions:

1. Design 2-bit magnitude comparator.

A1	A0	B1	В0	A > B	A = B	A < B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

From the Truth Table:

$$(A < B) = A_1'B_1 + A_0'B_1B_0 + A_1'A0'B0$$

$$(A=B) = A_1'A_0'B_1'B_0' + A_1'A_0B_1'B_0 + A_1A_0B_1B_0 + A_1A_0'B_1B_0'$$

$$(A>B) = A_1B_1' + A_0B_1'B_0' + A_1A_0B_0'$$

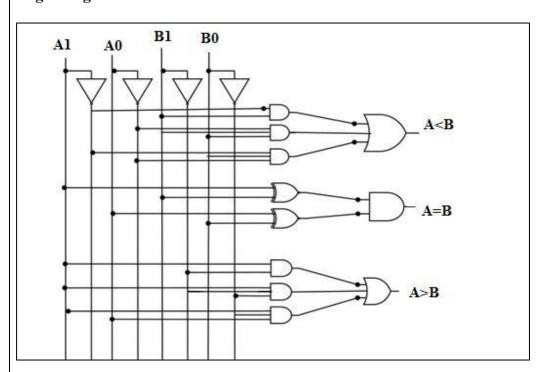
Semester: III Academic Year: 2023-24
Roll No:_____



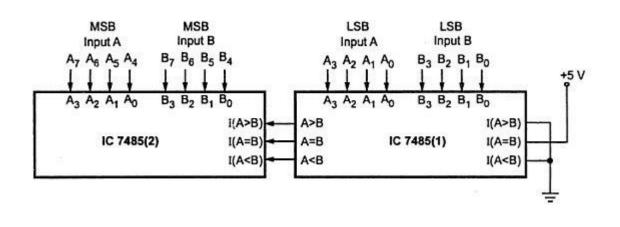
(A Constituent College of Somaiya Vidyavihar University) **Department of Computer Engineering**



Logic Diagram:



2. How can we implement 5-bit magnitude comparator using IC 7485.



Semester: III

Conclusion:

From this experiment we learnt the concept of comparators.



K. J. Somaiya College of Engineering, Mumbai-77 (A Constituent College of Somaiya Vidyavihar University)

Semester: III

Constituent College of Somaiya Vidyavihar University

Department of Computer Engineering



Signature of faculty in-charge with Date:

Academic Year: 2023-24 Roll No: