27.01.2023 (E)

SOMAIYA VIDYAVIHAR UNIVERSITY

Semester: August 2022 – December 2022 – (Jan-2023)		
Maximum Marks: 100 Examination: ESE Examination DSY (Reg+RT) Duration:3 Hrs.		
Programme code: 01 Programme: Computer Engineering	Class: SY	Semester:III (SVU 2020)
Name of the Constituent College: K. J. Somaiya College of Engineering	Name of the department: Computer	
Course Code: 116U01C303	Name of the Course: Computer Organization and Architecture	
Instructions: 1)Draw neat diagrams 2) All questions are compulsory 3) Assume suitable data wherever necessary		

Que. No.	Question	Max. Marks
Q1	Solve any **Four**	20
i)	Represent 43.8765 in single and double precision floating point formats	5
ii)	Compare Vertical and Horizontal microinstructions of control unit	5
iii)	Write the microinstructions for the following instruction ADD R1,(R2)	5
iv)	Assume that there are 3 page frames which are initially empty. If the page reference string is 1,2,3,4,2,1,5,3,2,4,6,5, what will be the number of page faults using the optimal page replacement policy?	5
v)	Explain different Cache write policies	5
vi)	Give five important features of a PCI bus	5

Que. No.	Question	Max Marks
Q2 A	Solve the following	10
i)	Explain the stages of a 6 stage pipeline. Briefly explain when does a pipeline stall.	5
ii)	Explain any two pipelining hazards that need to be avoided for correct program execution	5
	OR	
Q2 A	What is interrupt? Explain the interrupt cycle in an instruction cycle execution. Hence explain Interrupt driven I/O	10
Q 2 B	Solve any **One**	10
i)	Multiply 18 with -18 using Booth's Multiplication algorithm	10
ii)	Explain the restoring division and solve using restoring division 121/5	10

Que. No.	Question	Max. Marks
Q3	Solve any **Two**	20
i)	Compare Paging with Segmentation	10
ii)	What is Cache Coherence problem, Explain MESI Protocol to solve cache coherence problem in uniprocessor and multiprocessor systems	10
iii)	A computer system has main memory consisting of 16GB and 4K cache organized in 4 way-set-associative manner, and 32 bytes per block. Calculate the number of bits in each of TAG, SET and WORD fields of the main memory format.	10

Que. No.	Question	Max. Marks
Q4	Solve any **Two**	**20**
i)	Explain instruction format and basic instruction cycle with the help of neat diagram	10
ii)	Explain microprogrammed Control unit in detail	10
iii)	Compare Bit recoding and Booth's multiplication algorithm for multiplication, Which ot the two is faster. Demonstrate giving one example	10

Que. No.	Question	Max. Marks
Q5	Write short notes on any **four**	**20**
i)	Non restoring Division and its advantages over restoring division	5
ii)	Comparison of RISC vs CISC architectures	5
iii)	Page Replacement Algorithms	5
iv)	MIMD and SIMD with one practical example of each	5
v)	DMA data transfer modes	5
vi)	RAID Memory levels	5