30/11/2019 (E)

K. J. Somaiya College of Engineering, Mumbai-77
(Autonomous College Affiliated to University of Mumbai)

End Semester Examinations
Nov-Dec 2019

Max. Marks: 100 **Duration: 3Hrs**
Class: S.Y. BTECH Semester: III
Name of the Course: Computer Organization and Architecture Branch: COMPUTER ENGG
Course Code: 2UCC303

Instructions:
(1) All Questions are Compulsory
(2) Draw neat diagrams
(3) Assume suitable data if necessary

Note:
1. **Attempt any two in each Question.**

Question No.		Marks
Q 1 (a)	Define i. Clock speed/clock rate ii. Clock cycle iii. CPI iv. MIPS rate A bench mark program is run on a 200MHz machine. The executed program consists of 1million instruction executions with the instruction mix and clock cycle count: Instruction Type | Instruction Count | CPI Arithmetic | 4,00,000 | 1 Data Transfer | 3,50,000 | 2 Floating point | 2,00,000 | 3 Control Transfer | 50,000 | 2 Determine the effective CPI.	10
(b)	What is a stored program computer? Draw and explain the four main components of any general-purpose computer?	10
(c)	Explain following registers used in IAS computer: Memory Buffer Register (MBR), Memory Address Register (MAR), Instruction Register (IR), program Counter (PC) and Accumulator (AC). Show the content stored in each register after executing instruction, SUB M (1000): Subtract M(X) from AC; put the result in AC. The opcode of SUB M(X) is 00000110.	10
Q2 (a)	Draw flow chart for Booth's Algorithm for twos complement multiplication Multiply 7 * 3 using Booth's algorithm.	10
(b)	Write algorithm for restoring algorithm for division operation. Solve 7/5 using restoring algorithm for division operation.	10
(c)	Write algorithm for non-restoring algorithm for division operation. Solve 10/3 using non-restoring algorithm for division operation.	10

Q3 (a)	Explain the formats of IEEE 754 floating point number representation. The following bit pattern represents a floating point number in IEEE 754 single precision format 1 10000011 10100000000000000000000 Find the value of the number in decimal	10
(b)	Explain any two cache write policies.	10
(c)	What are the differences among direct mapping, associative mapping, and set-associative mapping? A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory addresses.	10
Q4 (a)	Differentiate between Programmed I/O, Interrupt driven I/O, DMA	10
(b)	Explain softwired and hardwired control unit design. Write the micro-operations and control signals for the instruction add R1, [R2].	10
(c)	Draw and explain a timing diagram for a PCI read operation.	10
Q5 (a)	Illustrate the need of virtual memory and relate concept of paging with virtual memory.	10
(b)	Explain Flynn's classification in parallel processing.	10
(c)	Explain the concept of instruction pipeline. Assume that there is only a two-stage pipeline (fetch, execute). Draw the timing diagram to show how many time units are needed for four instructions.	10