

(A Constituent College of Somaiya Vidyavihar University)



Department of Computer Engineering

Batch:-B2-2	Roll Number:-16010122151
-------------	--------------------------

Experiment Number: -1

TITLE: Study of PCI and SCSI.

AIM: To Study and learn PCI and SCSI

Expected OUTCOME of Experiment: (Mention CO/CO's attained here)

Books/ Journals/ Websites referred:

- 1. <u>https://www.techopedia.com/definition/8815/peripheral-component-interconnect-bus-pci-bus</u>
- 2. <u>https://www.techopedia.com/definition/331/small-computer-system-interface-scsi</u>
- 3. http://www.csun.edu/ edaasic/roosta/BUS Structures.pdf
- 4. W.Stallings William "Computer Organization and Architecture: Designing for Performance", Pearson Prentice Hall Publication, 7thEdition. C.

Pre Lab/ Prior Concepts:

Microcomputer buses which communicate with a peripheral devices or a memory location through communication lines called buses.

The major parts of microcomputers are central processing unit (CPU), memory, and input and output unit. To connect these parts together through three sets of parallel lines, called buses. These three buses are Address bus, data bus, and Control bus.

Address Bus:

The address bus consists of 16, 20, 24, or more parallel signal lines, through which the CPU sends out the address of the memory location. This memory location is used for to written to or read from. The number of memory location is depends on 2 to the power N address lines. Example, a CPU with 16 address lines can address 216 or 65,536 memory locations. When the CPU reads data from or writes data to a port. The port address is also sent out on the address bus. This is unidirectional. This means that the CPU can send data to a memory location or I/O ports.

Data Bus:

The data bus consists of 8, 16, 32 or more parallel signal lines. The data bus lines are bidirectional. This means that the CPU can read data from memory or from a I/O port as well as send data to a memory location or to a I/O port. In a system, many output



(A Constituent College of Somaiya Vidyavihar University)



Department of Computer Engineering

devices are connected to the data bus, but only one device at a time will be enabled to the output.

Control Bus:

The control bus consists of 4-10 parallel signal lines. The CPU sends out signals on the control bus to enable the outputs of addressed memory devices or port devices. Typically control bus signals are memory read, memory write, I/O read and I/O write. To read a data from a memory location, the CPU sends out the address of the desired data on the address bus and then sends out a memory read signal on the control bus. The memory read signal enables the addressed memory device to output the data onto the data bus where it is read by the CPU.

PCI Bus

The PCI local bus is a high-performance bus designed for high-speed data transfer. The PCI bus resides on the system board and is normally used as an interconnect mechanism between highly integrated peripheral components, peripheral add-on boards, and host processor or memory systems. The host processor, main memory, and the PCI bus itself are connected through a PCI host bridge. PCI devices can be connected to one or more of these secondary buses. In addition, other bus bridges, such as SCSI or USB, can be connected.

Types of PCI:

These are various types of PCI:

- PCI 32 bits have a transport speed of 33 MHz and work at 132 MBps.
- PCI 64 bits have a transport speed of 33 MHz and work at 264 MBps.
- PCI 32 bits have a transport speed of 66 MHz and work at 512 MBps.
- PCI 64 bits have a transport speed of 66 MHz and work at 1 GBps.

Function of PCI:

PCI slots are utilized to install sound cards, Ethernet and remote cards and presently strong state drives utilizing NVMe innovation to supply SSD drive speeds that are numerous times speedier than SATA SSD speeds. PCI openings too permit discrete design cards to be included to a computer as well.

PCI openings (and their variations) permit you to include expansion cards to a motherboard. The extension cards increment the machines capabilities past what the motherboard may create alone, such as: upgraded illustrations, extended sound, expanded USB and difficult drive controller, and extra arrange interface options, to title a couple of.

Advantages of PCI:

- You'll interface a greatest of five components to the PCI and you'll be able moreover supplant each of them by settled gadgets on the motherboard.
- You have different PCI buses on the same computer.



(A Constituent College of Somaiya Vidyavihar University)



Department of Computer Engineering

- The PCI transport will improve the speed of the exchanges from 33MHz to 133 MHz with a transfer rate of 1 gigabyte per second.
- The PCI can handle gadgets employing a greatest of 5 volts and the pins utilized can exchange more than one flag through one stick.

Disadvantages of PCI:

- PCI Graphics Card cannot get to system memory.
- PCI does not support pipeline.

SCSI bus:

The SCSI bus design for the library provides a peer-to-peer, I/O interface that supports up to 16 devices and accommodates multiple hosts.

Peer-to-peer interface communication can be from:

- Host to host
- Host to peripheral device
- Peripheral device to peripheral device

SCSI terms defining communication between devices on the SCSI bus include:

- Initiator is the device that requests an operation.
- Target is the device that performs the operation requested.

Benefits

A small computer system interface also provides these benefits:

- Low overhead
- High transfer rates
- A high-performance buffered interface
- Conformance to industry standards
- Plug compatibility for easy integration
- Error recovery, parity, and sequence checking provides high reliability
- Provisions in the command set for vendor-unique fields
- Standard or common command sets with an intelligent interface that provides device independence



(A Constituent College of Somaiya Vidyavihar University)



Department of Computer Engineering

Implementation

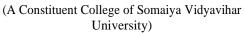
Implementation of the SCSI bus for the library supports:

- 8-bit wide transfers, asynchronous; 16-bit wide selection
- Disconnect and reselect
- Multiple initiator
- Hard resets
- Single-ended LVD
- SCSI-3, 68-pin P-cable

Implementation for the library does not support:

- Soft resets
- Command queuing
- Command linking
- Asynchronous event notification
- Extended contingent allegiance







Department of Computer Engineering

Post Lab Descriptive Questions Q1 . Differentiate between PCI and SCSI Bus

PCI BUS	SCSI BUS
Peripheral Component Interconnect (PCI),	
as its name implies is a standard that	SCSI is standard electronic interfaces that
describes how to connect the peripheral	allow personal computers to communicate
components of a system together in a	with peripheral hardware such as disk
structured and controlled way	drives, tape drives etc.
PCI bus can transfer 32 or 64 bits at one	It has a data rate of 160 MB/s.
time. PCI bus can run at 33 Mhz.	
PCI can be used for a variety of	SCSI is only used for storage devices and
peripherals. For example Graphics cards	must have an interface controller.
and NICs.	

Q2. List two applications each of PCI and SCSI Bus

PCI

Install sound cards, Ethernet and remote cards and presently strong state drives utilizing NVMe innovation to supply SSD drive speeds that are numerous times speedier than SATA SSD speeds.

SCSI

Examples of devices having SCIC bus: hard drives, CD-ROM drives, tape drives , and Scanners.