Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:	**5/ 10/ 2023**	**Batch No:**	**B-2**
Faculty Name:		**Roll No:**	**16010122151**
Faculty Sign & Date:		**Grade/Marks:**	**___/25**

Experiment No: 7
Title: Asynchronous Counter

Aim and Objective of the Experiment:

To design and implement 3 bit Asynchronous up counter using JK Flip Flop

COs to be achieved:

CO3: Design synchronous and asynchronous sequential circuits.

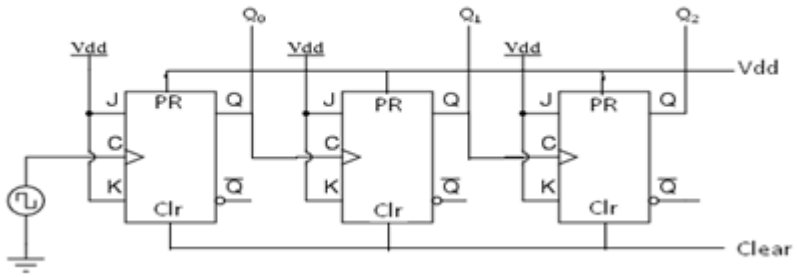
Tools used:

Trainer kits

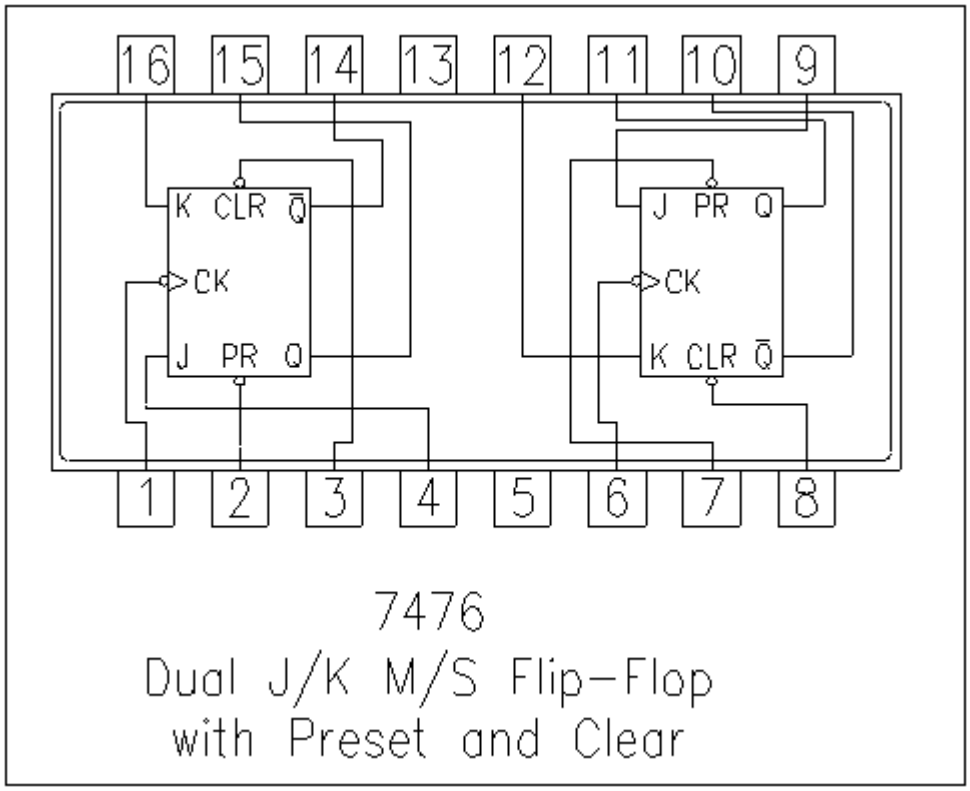
Theory:

Circuit diagram of 3 bit Asynchronous Up counter using JK FF (IC 7476)

Logic Diagram for 3- bit Up Counter:



Pin diagram of JK FF (IC 7476)



Implementation Details

Procedure

1) Locate IC 7476 JK FF on Digital trainer kit
2) Apply various inputs to appropriate pins as per the circuit diagram of the 3 bit Asynchronous up counter with reference to the pin configuration of the IC.
3) Make sure of Reset and Clear Pins connections with reference to data sheet information.
4) Connect a pulsar switch to the clock input.
5) Verify the working and prepare a truth table.

Post Lab Subjective/Objective type Questions:

1. **How JK FF need to be configured to use for counter operation?**
   To configure a JK flip-flop for use in a counter operation, you typically connect multiple JK flip-flops in a cascade (also known as a ripple counter) and connect their J and K inputs appropriately. In a simple up-counter, you connect the J and K inputs of each JK flip-flop as follows:

   The J input of the first flip-flop is set to 1, and the K input is set to 0.
   The J input of each subsequent flip-flop is connected to the Q output of the previous flip-flop.
   The K input of each subsequent flip-flop is also connected to the Q output of the previous flip-flop, but through an inverter (NOT gate).

2. **What changes are required to use the same counter as 3 bit asynchronous down counter**?
   To use the same counter as a 3-bit asynchronous down counter, you need to modify the connections as follows:
   a. The J input of the first flip-flop remains set to 1, and the K input is set to 0.
   b. The J and K inputs of each subsequent flip-flop are connected to the complement (opposite) of the Q output of the previous flip-flop.
3. **Draw the timing diagram of 3 bit Asynchronous up counter**
   Clock: _|‾‾‾‾|_|‾‾‾‾|_|‾‾‾‾|_|
   Bit 0: 0 1 0 1 0 1 0 1
   Bit 1: 0 0 1 1 0 0 1 1
   Bit 2: 0 0 0 0 1 1 1 1
   Each bit changes state on the rising edge of the clock signal, resulting in an increment by 1 for each clock cycle.
4. **What is mod n concept used in counters?**
   The "mod n" concept in counters refers to the counting range of the counter. A counter can count from 0 to (n-1) before it resets to 0. For example, in a mod-5 counter, the counter will count from 0 to 4 and then reset to 0, effectively having 5 unique states. The modulo value (n) determines the counting range, and it's also the number of different states the counter can represent.
5. **For Mod-5 counter how many JK FFs are required?**
   For a Mod-5 counter, you would need three JK flip-flops. This is because a 3-bit counter can represent values from 0 to 7 (2^3 = 8), but for a Mod-5 counter, you only need to count from 0 to 4. Therefore, a 3-bit counter can be used, and it will require three JK flip-flops to represent these 5 states.

Conclusion:

The experiment effectively demonstrated the configuration, operation, and practical implementation of a 3-bit asynchronous up counter using JK flip-flops, providing valuable insights into digital counter circuits and their applications.

Signature of faculty in-charge with Date: