Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:		**Batch No:**	**B2**
Faculty Name:		**Roll No:**	**16010122151**
Faculty Sign & Date:		**Grade/Marks:**	**/25**

Experiment No: 5
Title: Flip Flops

Aim and Objective of the Experiment:

To Verify truth table of JK Flip flop using IC 7476 and study conversion of JK FF to D FF and T FF

COs to be achieved:

CO3: Design synchronous and asynchronous sequential circuits.

Tools used:

Trainer kits

Theory:

Flip-flop is the common name given to two-state devices which offer basic memory for sequential logic operations. Flip-flops are heavily used for digital data storage and transfer and are commonly used in banks called "registers" for the storage of binary numerical data.

JK-flip flop: has two inputs, traditionally labeled J and K. IC 7476 is a dual JK master slave flip flop with preset and clear inputs. If J and K are different then the output Q takes the value of J at the next clock edge. If J and K are both low then no change occurs. If J and K are both high at the clock edge, then the output will toggle from one state to the other. It can perform the functions of the set/reset flip-flop and has the advantage that there are no ambiguous states.

D Flip Flop: tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell. D flip-flop can be made from J-K flip-flop by connecting both inputs through a not gate.

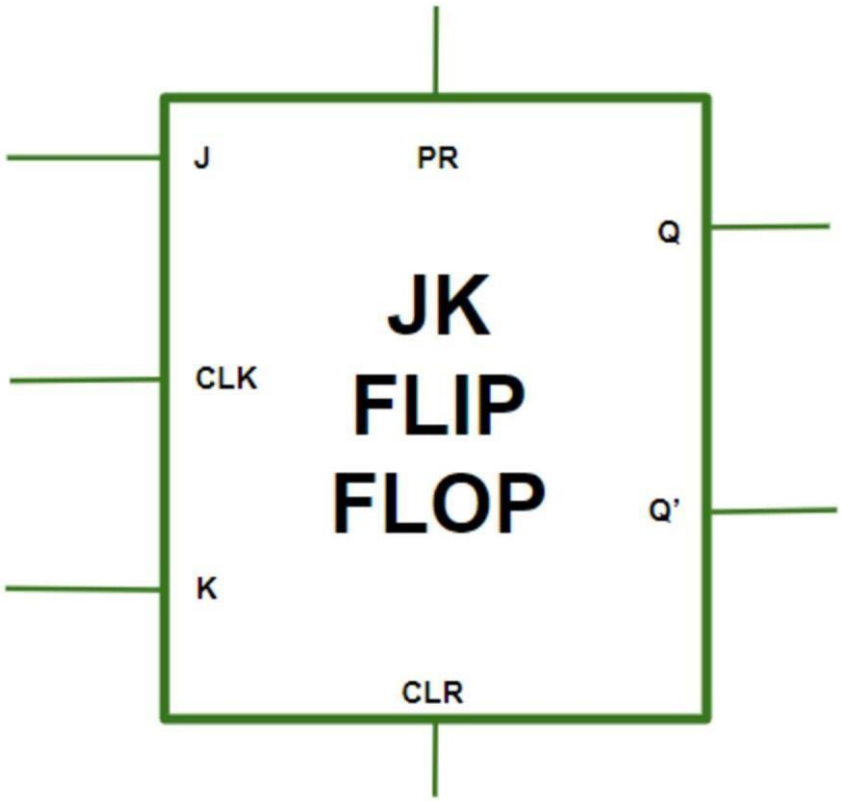
T Flip Flop: T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

Implementation Details:

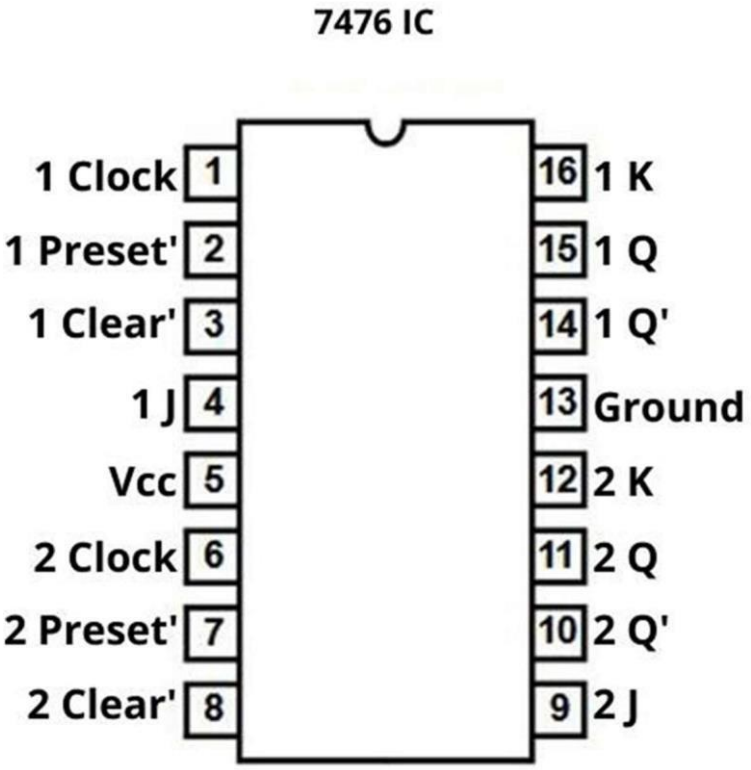
Procedure

1) Locate IC 7476 on Digital trainer kit
2) Apply various inputs to J & K pins by means of the output on logic output indicator.
3) Connect a pulsar switch to the clock input.
4) Connect the J&K as D and T flip flop as shown in diagrams and verify the respective Truth tables.

Logic Symbol



Pin Diagram of IC 7476



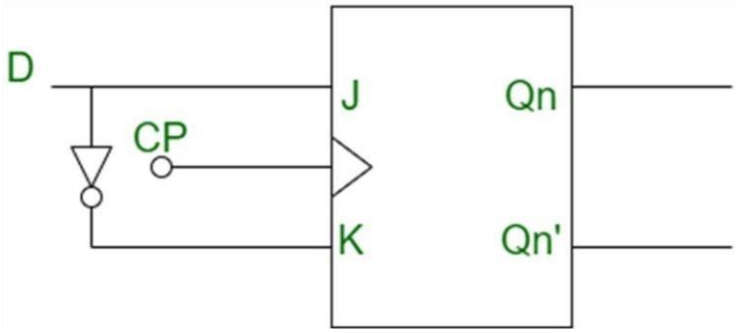
Truth Table of JK FF

J	K	Q	Q’	Q n +1	Qn+ 1’
0	0	0	1	0	1
0	0	1	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	1	0	1	1	0
1	1	1	0	0	**1**

Conversion of FFs

1) JK to D FF

Conversion Diagram

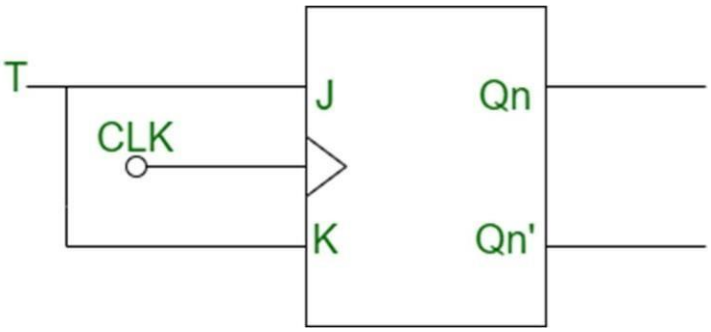


Truth Table of D FF

clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

1) JK to T FF

Conversion Diagram



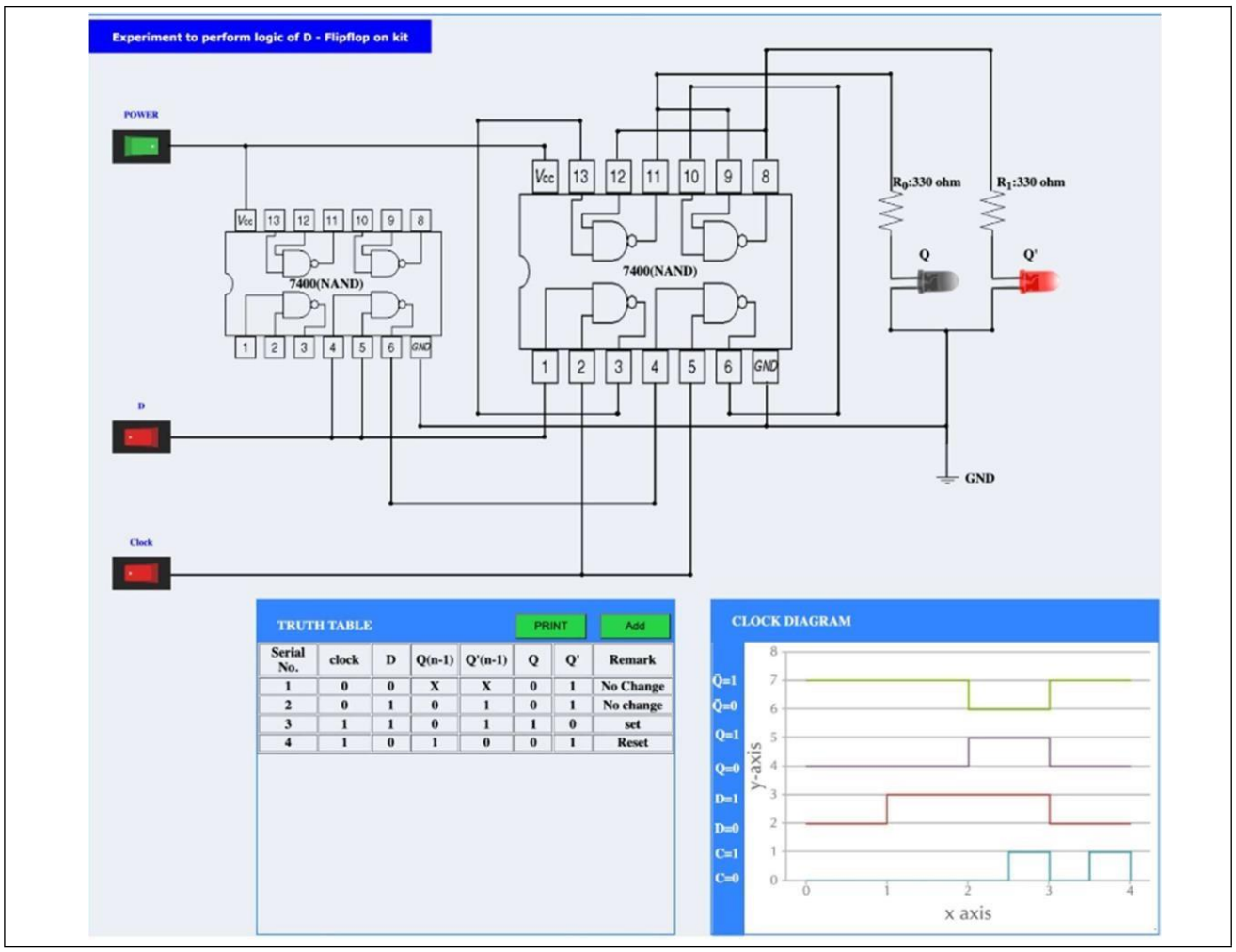
Truth Table of T FF

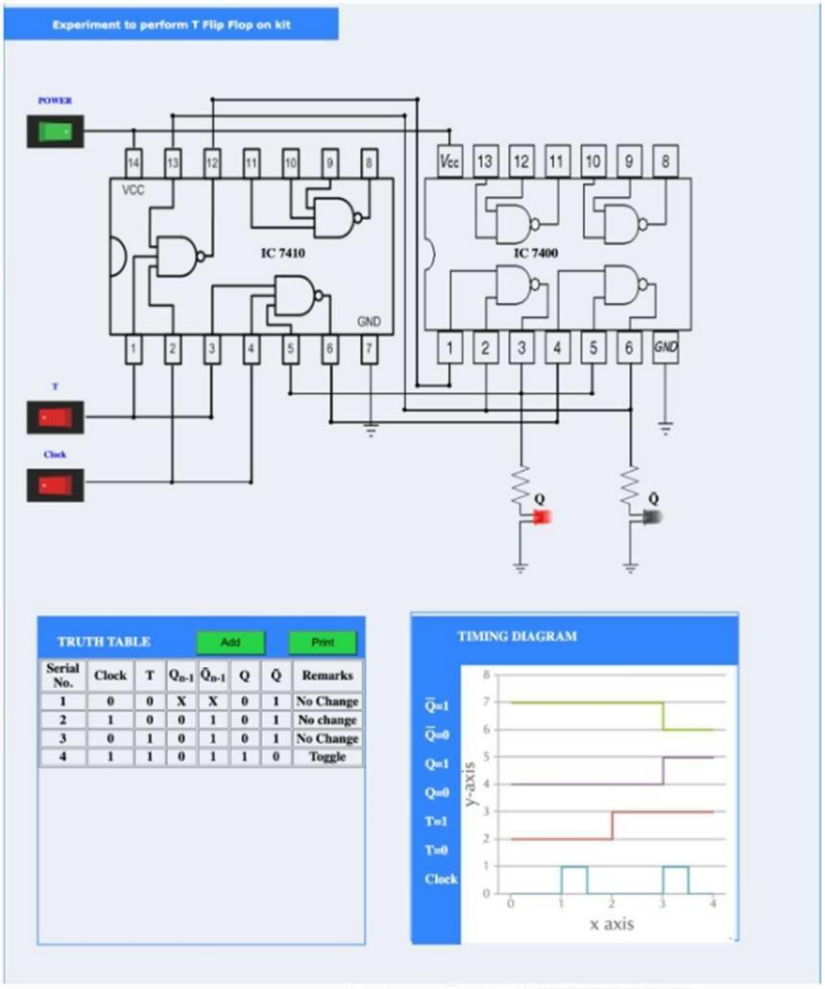
clk	T	Q(t)	Q(t+1)
0	x	Q	Q
1	0	Q	Q
1	1	Q	~Q

Implementation Details

Procedure:

1) Locate the IC 7476 and place the IC on trainer kit.
2) Connect VCC and ground to respective pins of IC trainer kit.
3) Implement the circuit as shown in the circuit diagram.
4) Connect the inputs to the input switches provided in the trainer kit.
5) Connect the outputs to the switches of O/P LEDs
6) Apply various combinations of inputs according to the truth table and observe the condition of LEDs.
7) Note down the corresponding output readings for various combinations of inputs.


Experiment to perform logic of D - Flipflop on kit
POWER
D
Clock
Vcc
13
12
11
10
9
8
7400(NAND)
1
2
3
4
5
6
GND
R0:330 ohm
R1:330 ohm
Q
Q'
GND
TRUTH TABLE
PRINT
Add
Serial No.
clock
D
Q(n-1)
Q'(n-1)
Q
Q'
Remark
1 0 0 X X 0 1 No Change
2 0 1 0 1 0 1 No change
3 1 1 0 1 1 0 set
4 1 0 1 0 0 1 Reset
CLOCK DIAGRAM
Q̄=1
Q̄=0
Q=1
Q=0
D=1
D=0
C=1
C=0
y-axis
x axis



Serial No.	Clock	T	Q_{n-1}	$\bar{Q}_{n-1}$	Q	$\bar{Q}$	Remarks
1	0	0	X	X	0	1	No Change
2	1	0	0	1	0	1	No change
3	0	1	0	1	0	1	No Change
4	1	1	0	1	1	0	Toggle

Post Lab Subjective/Objective type Questions:

1. How does a JK flip-flop differ from an SR flip-flop in its basic operation?

SR flip flop is also known as set reset FF (flip flop).
When set (S) terminal is at high state and reset (R) is at low state, it's Q (output) terminal is at high stateWhen set (S) terminal is at low state and reset (R) is at high state, it's Q (output) terminal is at low state. But if both S and R, are at high state, output is unpredictable.
To come over this situation, JK FF was designed. To S terminal, output of AND gate is connected. Inputs ofgate are J and complement of Q output of same FF is connected.
To R terminal output of another AND gate is connected, whose inputs are K and Q terminal of same FF.NOW FF is called as JK FF. advantage of JK FF is that even when both inputs are at high state, output iscomplement of previous output and is predictable.
However simple JK FF suffers from race around condition and to avoid this edge triggered master slave FF isused.
So, the advantage of JK FF over SR FF is that even if both inputs are at high state, output is complement of previous output.

2. What is the use of characteristic and excitation table?

   Characteristic table: It defines the state of each flip-flop as a function of its inputs and previous state. Q refers to the present state and Q(next) refers to the next state after the occurrence of the clock pulse. Excitation table: During the design process we usually know the transition from present state to the next state and wish to find the flip-flop input conditions that will cause the required transition. For this reason, we will need a table that lists the required inputs for a given change of state. Such a list is called the excitation table.

3. How many flip flops do you require storing the data 1101?

   4 flip flops are required.

Conclusion:

In conclusion, our experiment successfully verified the truth table of a JK flip-flop using the IC 7476 and demonstrated its functionality. Additionally, we explored the conversion of a JK flip-flop into both a D flip-flop and a T flip-flop, showcasing the adaptability and versatility of flip-flop circuits in digital logic design. This knowledge is essential for understanding and designing sequential circuits.

Signature of faculty in-charge with Date: