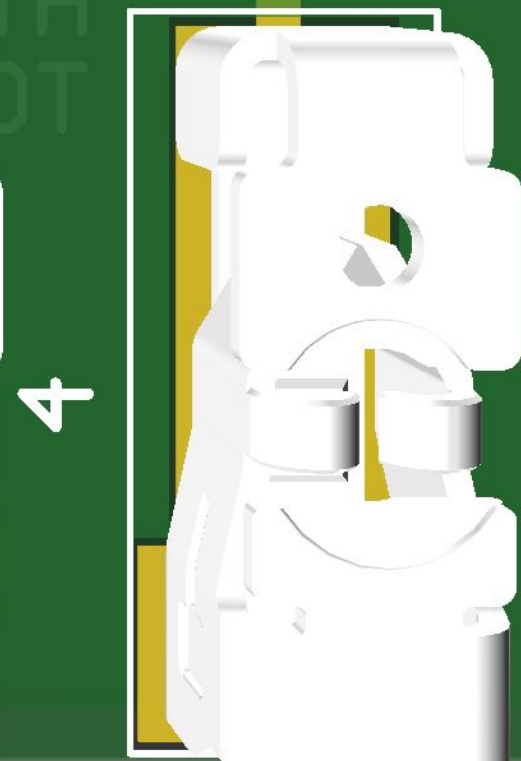
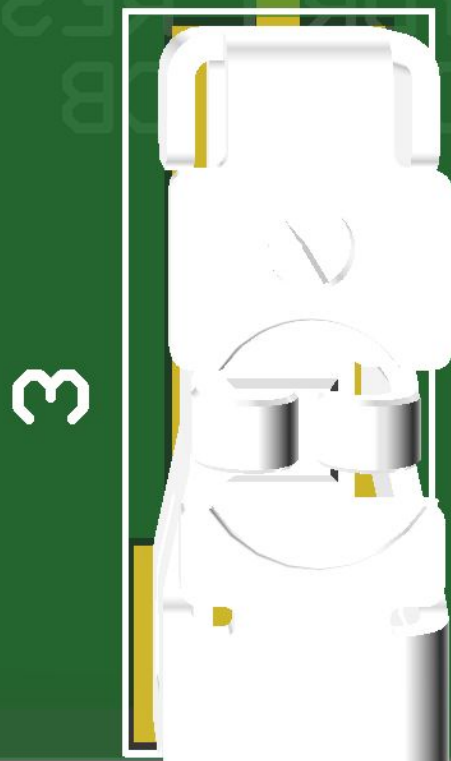
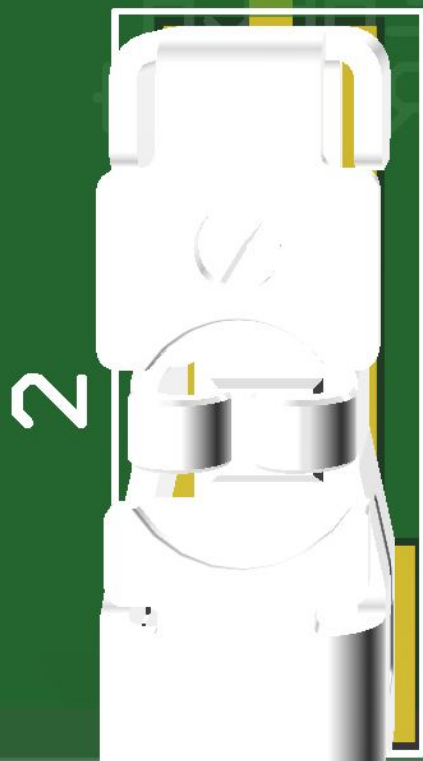
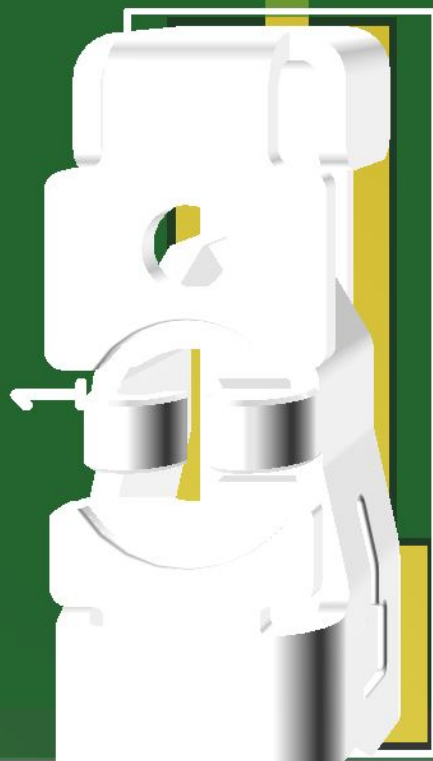
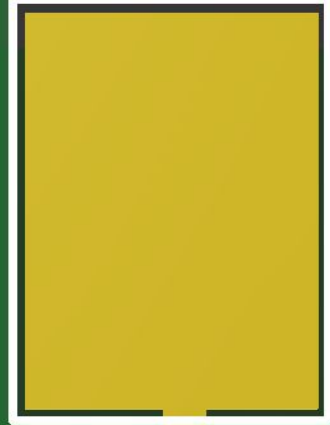
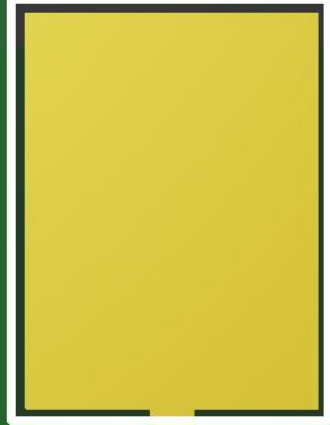


HEAT

TEMP





J4

J3

J2

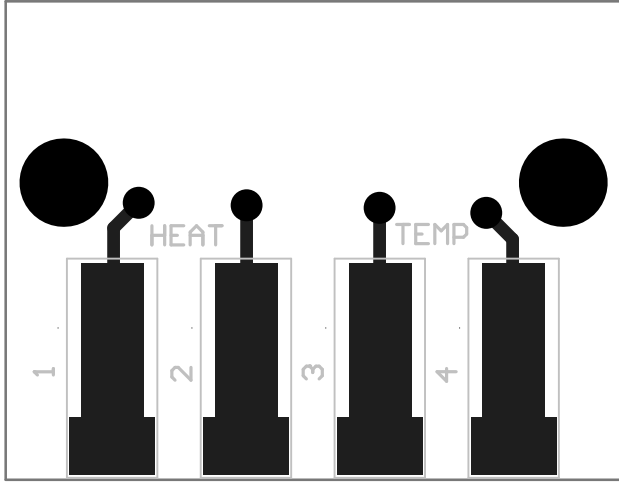
J1

TEMP

HEAT



HYDRA RESEARCH
TOOL PCB REV0.4





1



2



3



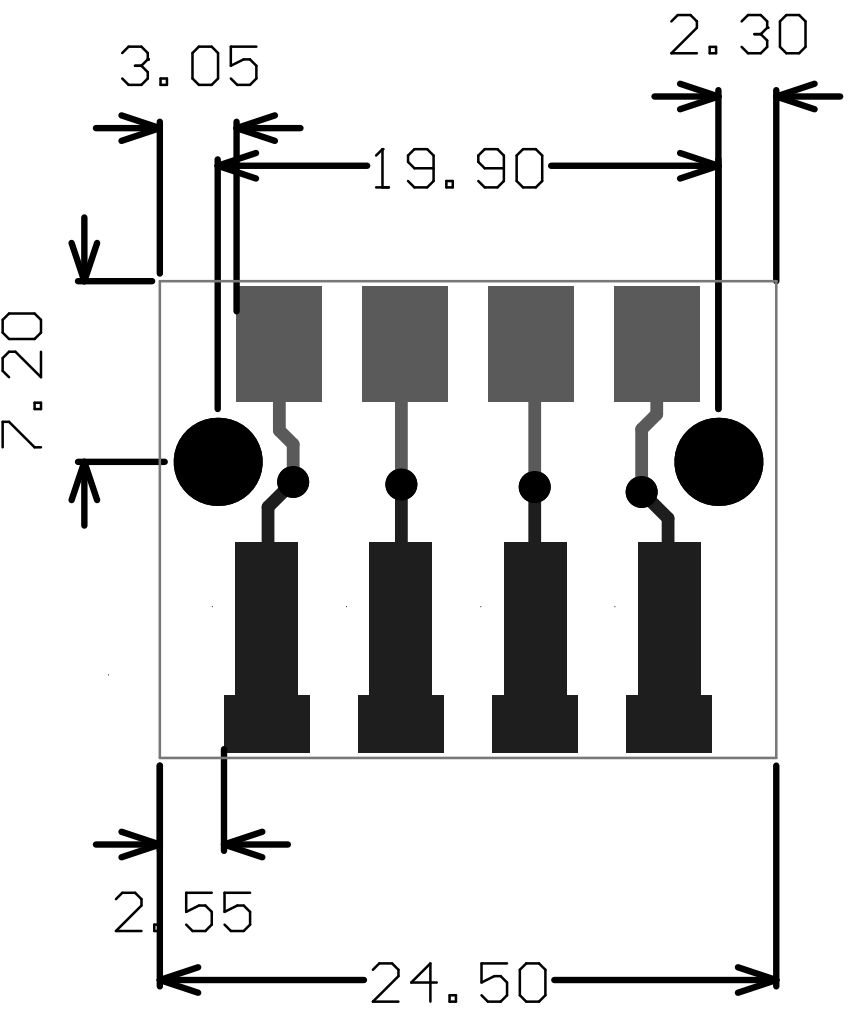
4

HEAT

TEMP

HYDRA RESEARCH
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Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Description	Hole Tolerance (+)	Hole Tolerance (-)
□	2	98.43mil (2.500mm)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c350h250			
○	4	28.00mil (0.711mm)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v127h71			
	6 Total										



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.39mil	3.5	
3	Top Layer	Copper	1.38mil		
4	Dielectric 1	FR-4	59.06mil	4.8	
5	Bottom Layer	Copper	1.38mil		
6	Bottom Solder	Solder Resist	0.39mil	3.5	
7	Bottom Overlay				

HEAT

TEMP

J1

J2

J3

J4



CONTACT

CONTACT

CONTACT

CONTACT



1

2

3

4

WM17990CT

WM17990CT

WM17990CT

WM17990CT

HEAT

TEMP

HYDRA RESEARCH
TOOL PCB REV0.4

Title		
Size	Number	Revision
A		
Date:	10/3/2018	Sheet of
File:	C:\Project\...\REV04.SchDoc	Drawn By: