Haroutun Haroutunian
Professor Berhe
ECE 442L
27 October 2021

Lab 1 MyDAQ

Schematic Lab 1 MyDAQ:

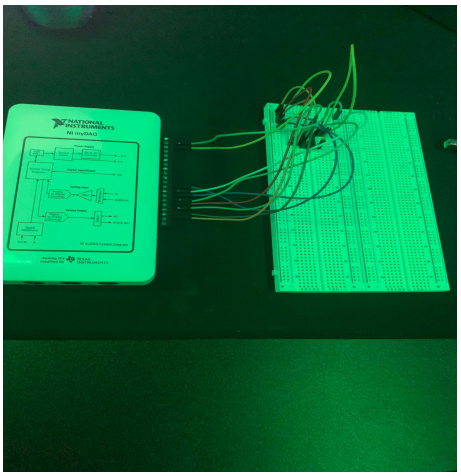


Figure 1.1 MyDAQ Circuit

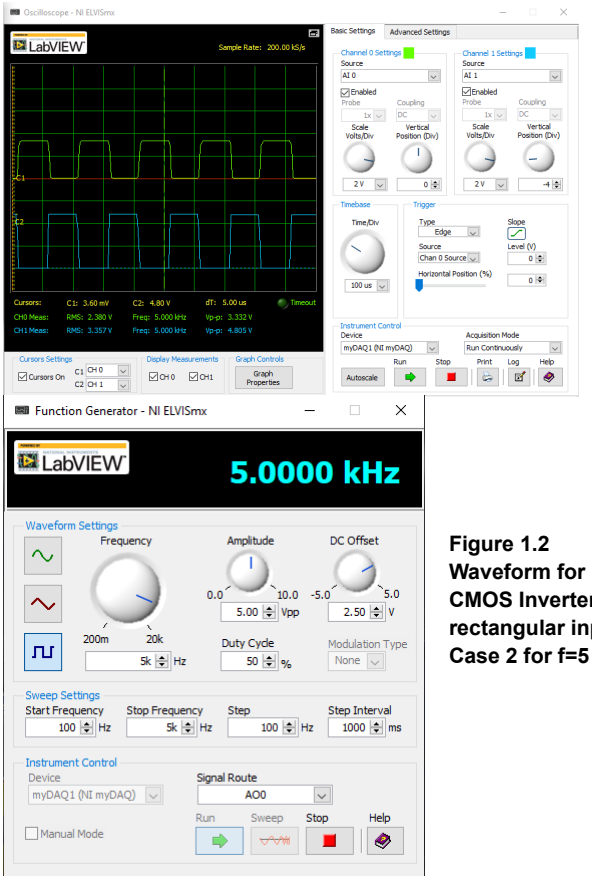


Figure 1.2 Waveform for CMOS Inverter 5V rectangular input Case 2 for f=5 kHz

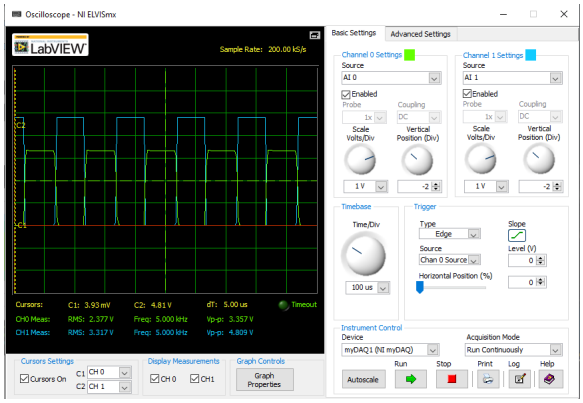


Figure 1.3Overlapped Waveform for CMOS Inverter 5V rectangular Input Case 2 for f = 5kHz

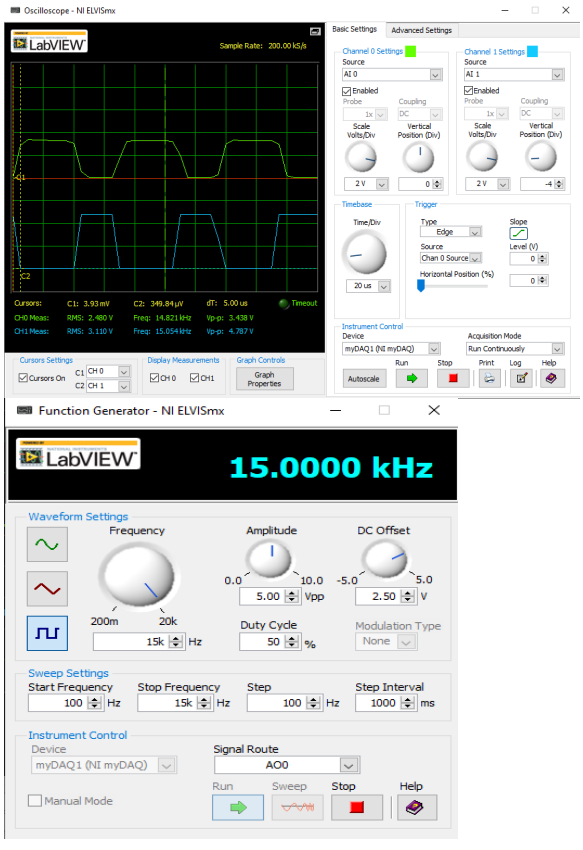


Figure 1.4 Waveform for CMOS Inverter 5V rectangular input case 4 for f=15kHz

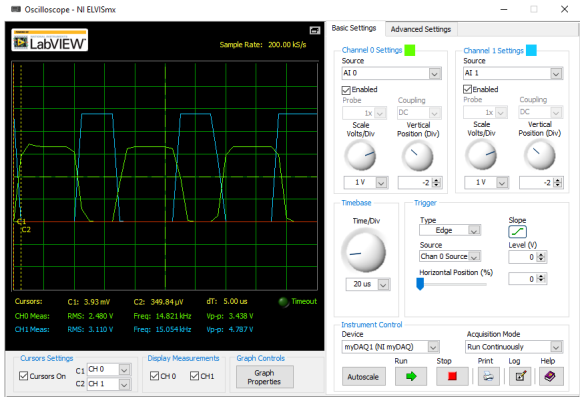
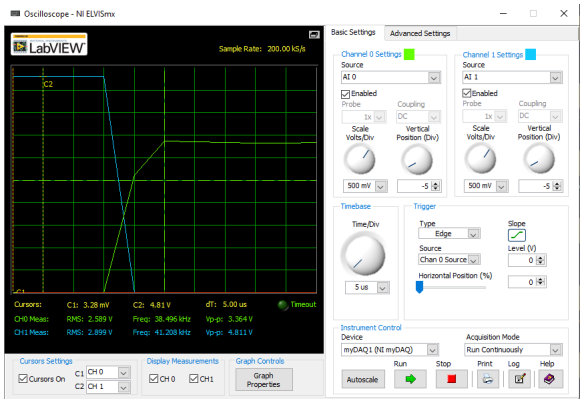


Figure 1.5 Overlapped Waveform for CMOS inverter 5V rectangular input case 4 for f=15kHz



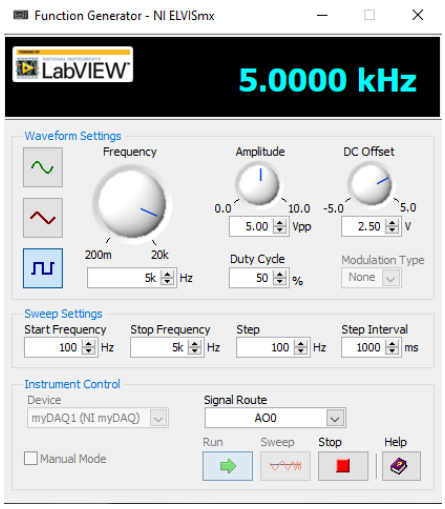
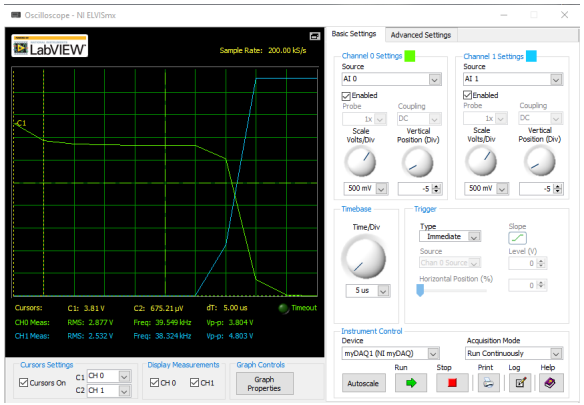


Figure 1.6 Waveform for Case 2 CMOS inverter Propagation Delay HIGH to LOW for f=5kHz



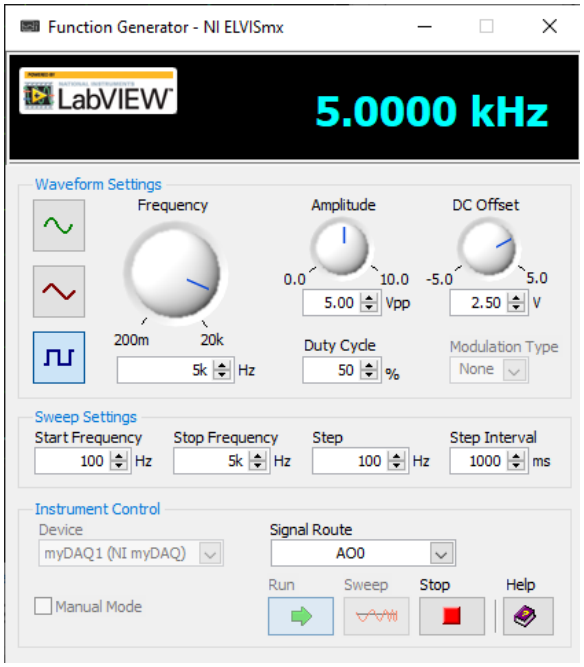


Figure 1.7 Waveform for Case 2 CMOS inverter Propagation Delay LOW to HIGH for f=5kHz

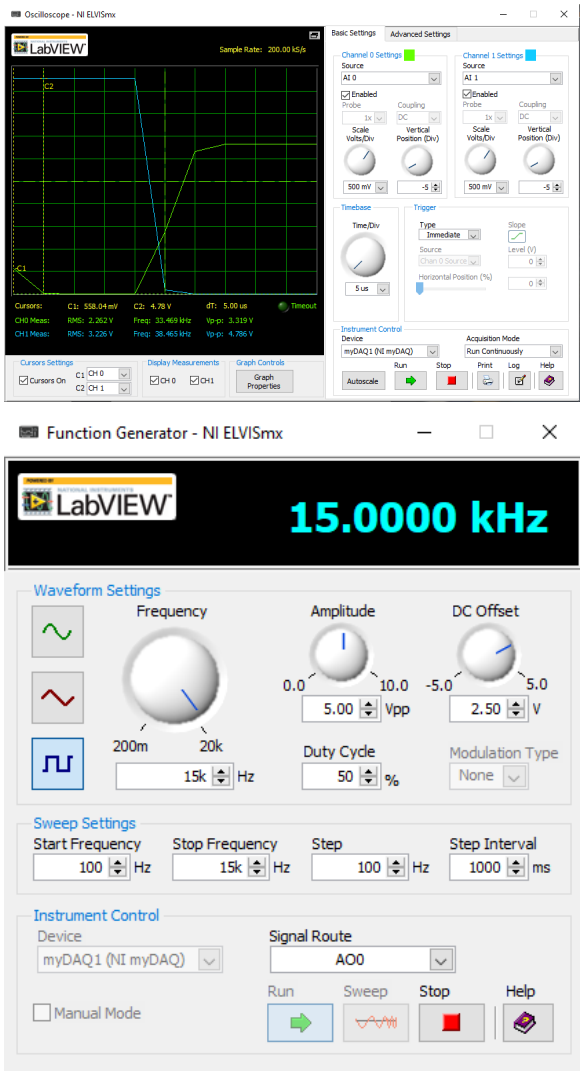


Figure 1.8 Waveform for Case 4 CMOS inverter Propagation Delay HIGH to LOW for f=15kHz

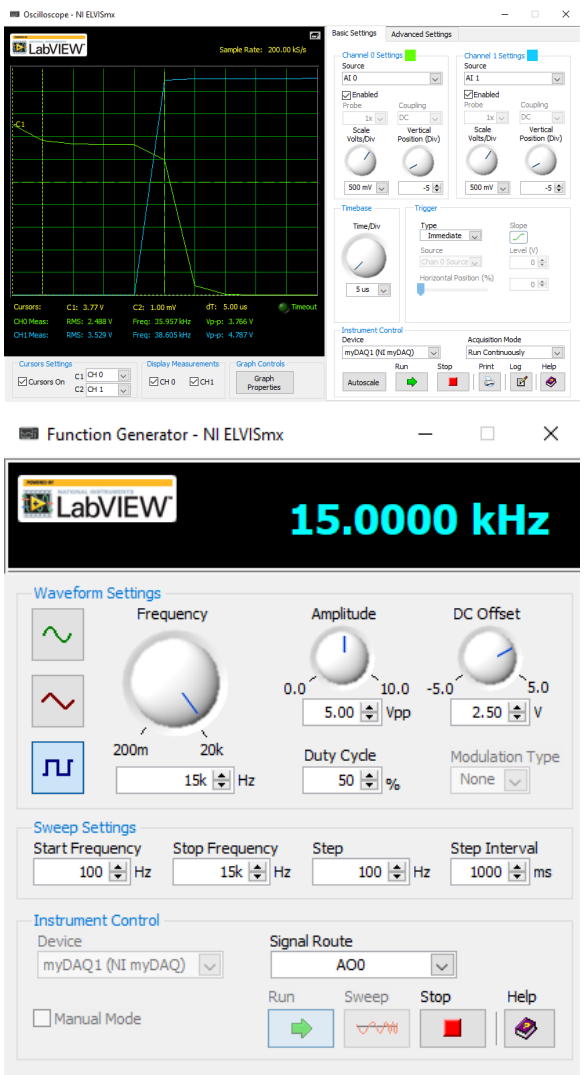


Figure 1.9 Waveform for Case 4 CMOS inverter Propagation Delay LOW to HIGH for f=15kHz

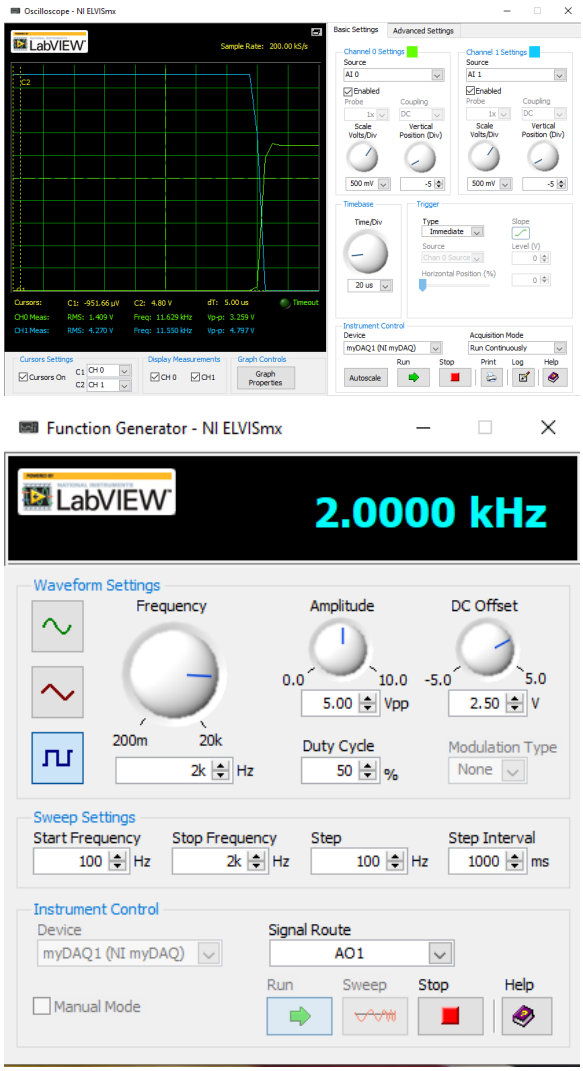


Figure 1.10 Waveform for ramp case 2 CMOS Inverter voltage transfer for triangular Wave for f = 2kHz and Slope = 4.14V

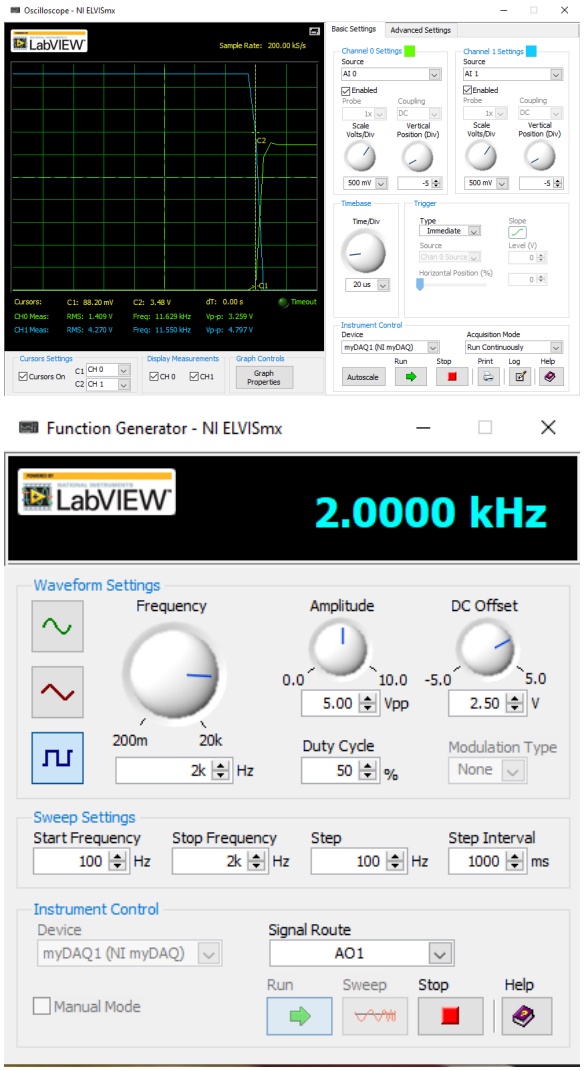


Figure 1.11 Waveform for ramp case 2 CMOS Inverter voltage transfer for triangular Wave for f = 2kHz and Slope = 0.3 V