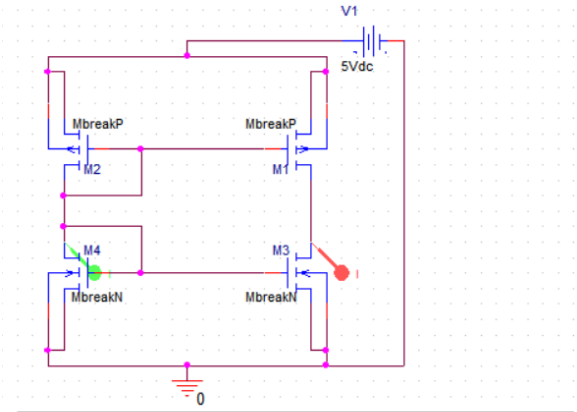
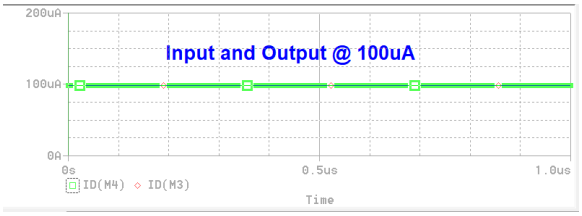
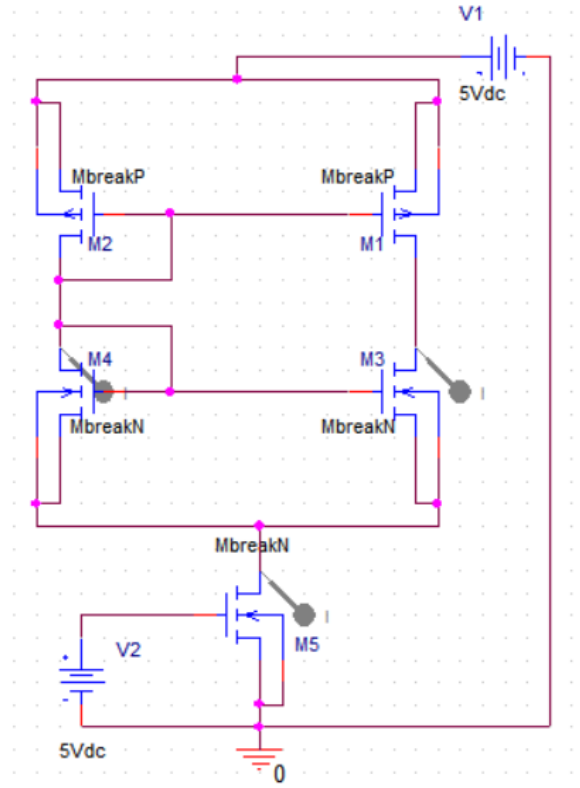
Assignment for Lab 2 Weekly Lab Report Demo CMOS Transistor Level Current Source Design, Simulation and Experimental Test as well as Analysis



Case 1 CMOS Mirror Normal Sizing



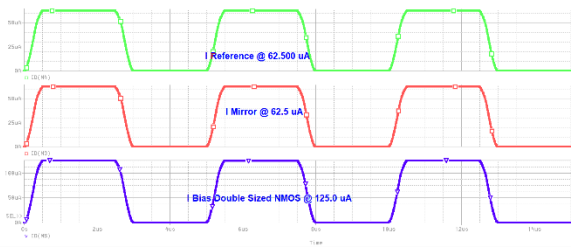
Trace Color	Trace Name	X1	X2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		0.000		
	X Values	0.000	0.000	0.000		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	ID(M4)	98.640u	98.640u	0.000		0.000	0.000	98.640u	98.640u	98.640u
	ID(M3)	98.640u	98.640u	0.000		0.000	0.000	98.640u	98.640u	98.640u



Case 3 NMOS Bias Double Sizing

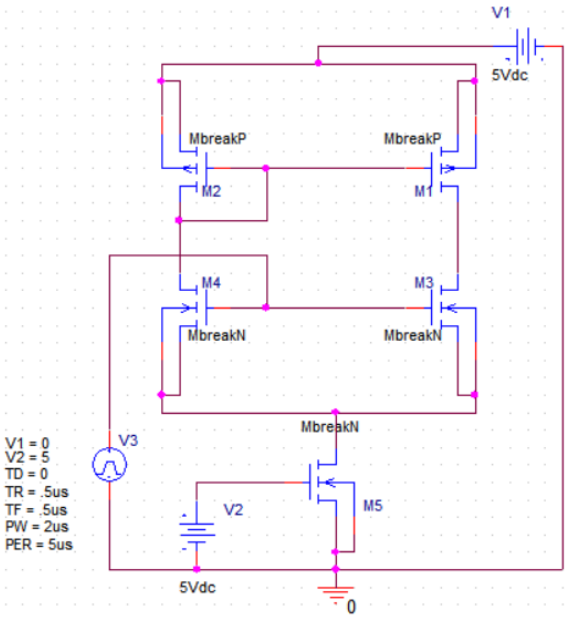
Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)	0.000		
	X Values	0.000	0.000	0.000		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	ID(M5)	231.028u	231.028u	0.000		0.000	0.000	231.028u	231.028u	231.028u
	ID(M3)	115.514u	115.514u	0.000		-115.514u	-115.514u	115.514u	115.514u	115.514u
	ID(M4)	115.514u	115.514u	0.000		-115.514u	-115.514u	115.514u	115.514u	115.514u

Graph of NMOS BIAS Double Sizing



Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)	125.000u		
	X Values	1.9273u	0.000	1.9273u		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	ID(M5)	125.000u	10.019p	125.000u		0.000	0.000	125.000u	10.019p	62.500u
	ID(M3)	62.500u	5.1091p	62.500u		-62.500u	-4.9095p	62.500u	5.1091p	31.250u
	ID(M4)	62.500u	5.1091p	62.500u		-62.500u	-4.9095p	62.500u	5.1091p	31.250u

Graphical representation of AC current Applied to Double Sized Biased NMOS Circuit



Case 5 AC Current Mirror with Bias NMOS @ 2(W/L) @ 200 kHz