Haroutun Haroutunian Professor Berhe ECE 443L 17 February 2022

## Lab 2: CMOS Transistor Level Current Source

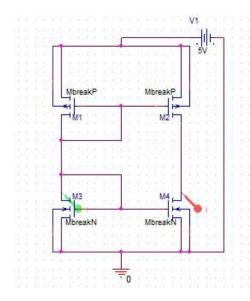


Figure 2.1: <u>Case 2</u> DC Current Mirror with Double NMOS sizing schematic

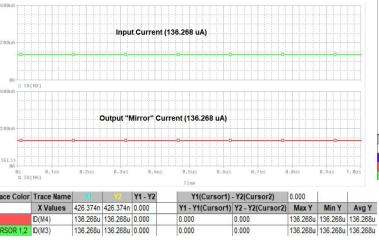


Figure 2.2: DC Current Mirror with Double NMOS sizing waveform and cursor, I/O current @ 136.268 uA

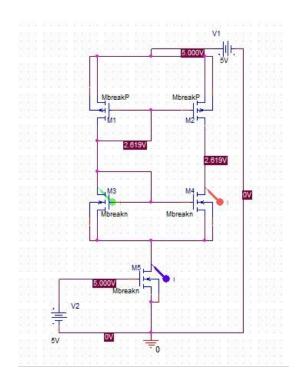


Figure 2.3: <u>Case 4</u> DC Current Mirror with Bias NMOS and 3 \* (W/L) for NMOS sizing schematic

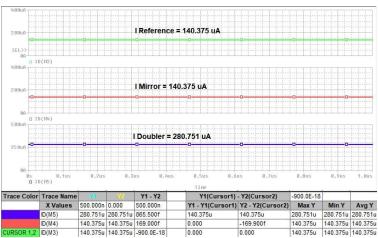


Figure 2.4: DC Current Mirror with Bias NMOS and 3 \* (W/L) for NMOS sizing waveform and cursor. Reference and Mirror currents @ 140.375 uA and Doubler current @ 280.751 uA

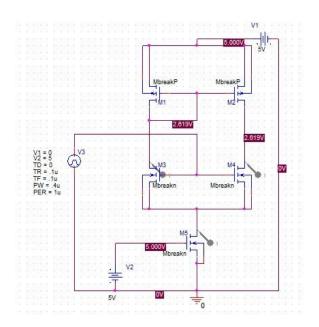


Figure 2.5: <u>Case 6</u> AC Current Mirror with Bias NMOS and 2 \* (W/L) for NMOS sizing schematic, v\_in(t) = 5V square wave with f = 1 MHz

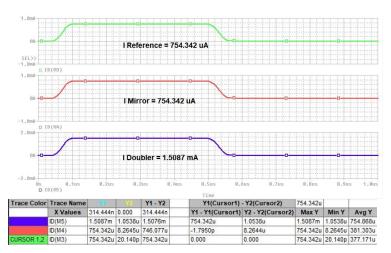


Figure 2.6: AC Current Mirror with Bias NMOS and 2 \* (W/L) for NMOS sizing waveform, v\_in(t) = 5V square wave with f = 1 MHz.Reference and Mirror currents @ 754.342 uA and Doubler current @ 1.5087 mA