California State University, Northridge
College of Engineering & Computer Science
Electrical and Computer Engineering Department

ECE 443L Digital Electronics Laboratory
Report 3

CMOS Transistor Level Amplifier Design, Simulation and Experimental Test as well as Analysis

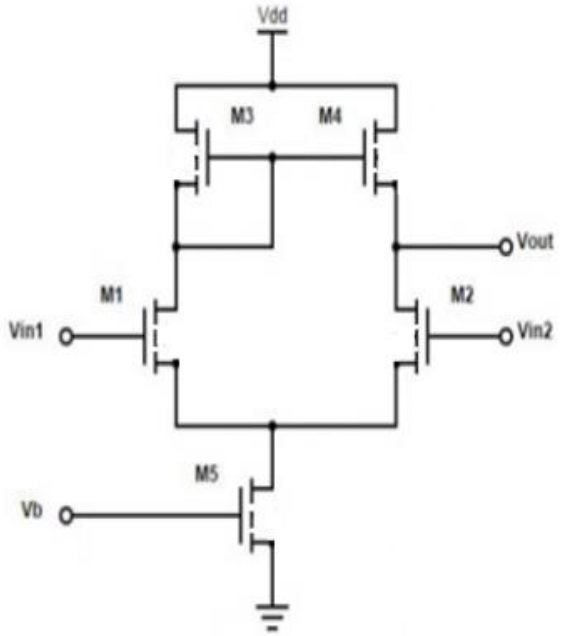
By Evan Thomas, Haroutun Haroutunian

Abstract:

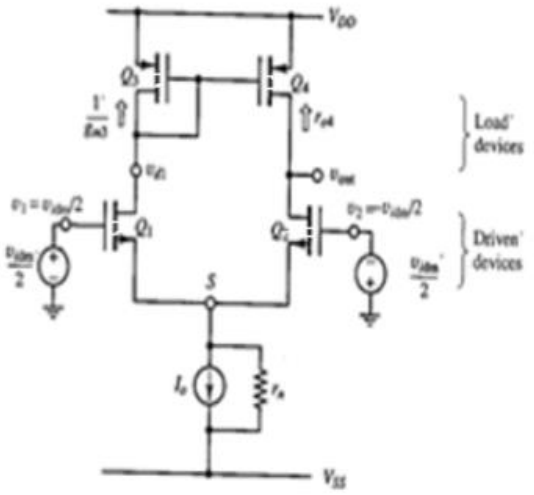
After designing any CMOS transistor level differential amplifier. We needed to model it after certain specifications. These specifications are as follows. V offset needs to be around 3V with a frequency in the range of 20 kHz to 50kHz. The input voltage needs to be between 10mV and 50mV. We also need to have three different voltages as well as three different frequencies.

Introduction:

The CMOS transistor level differential amplifier is an amazing device. The earth would not be what it is today without it! The CMOS transistor level differential amplifier topology is as shown.

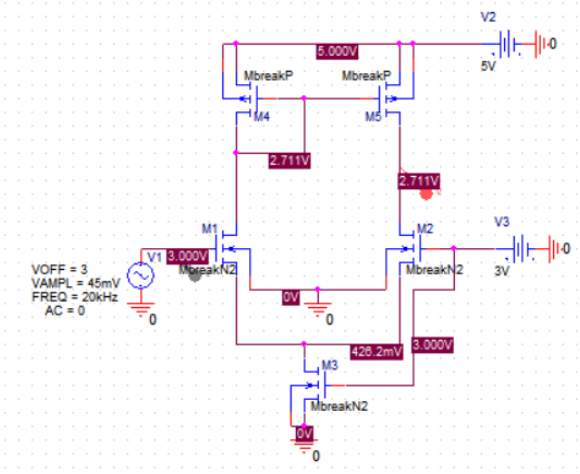


If this view was not enough to understand the topology of the wonderful CMOS device then another look is offered here.

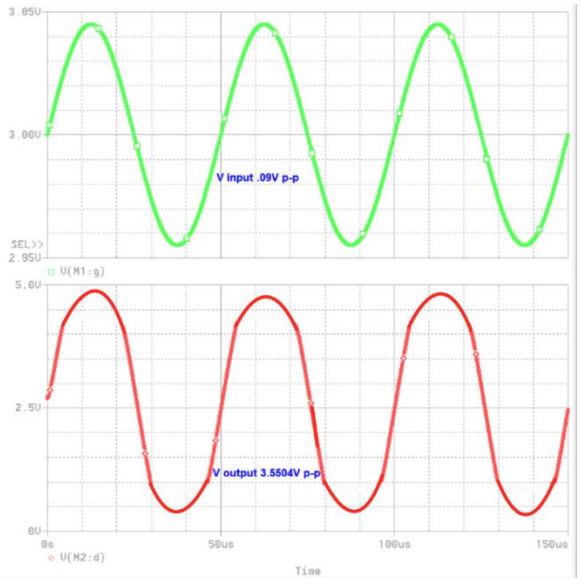


In this lab it is required to simulate this differential amplifier under the given constraints.

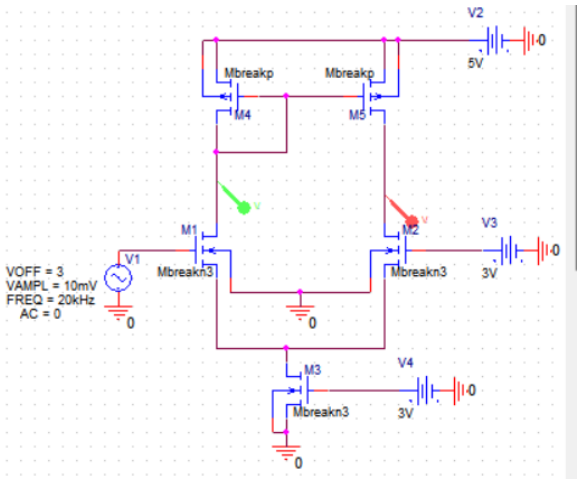
Lab 3: CMOS Transistor Level Utility Amplifier Design



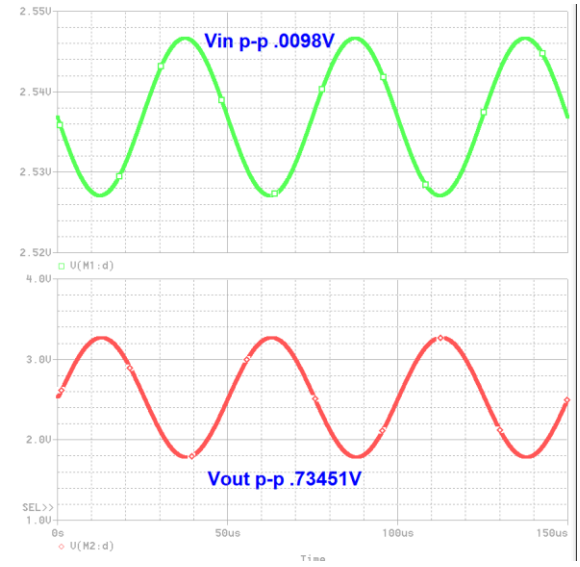
Case 1: VAMPL of 45mV with a frequency of 20kHz. AV =39.45



Graph of Case 1 with an AV of 39.45 and Frequency of 20kHz with double bias NMOS

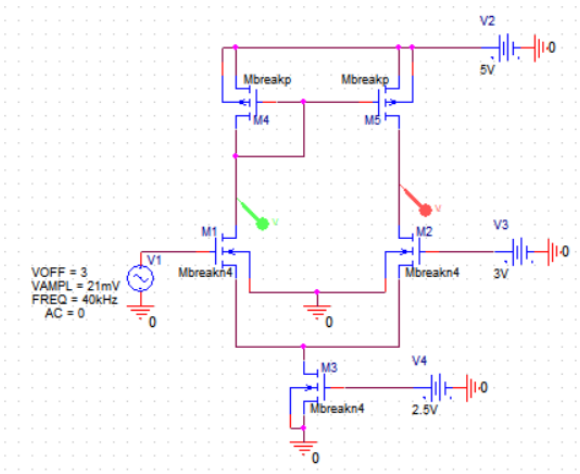


Case 3 VAMPL 10mV @ 20Khz

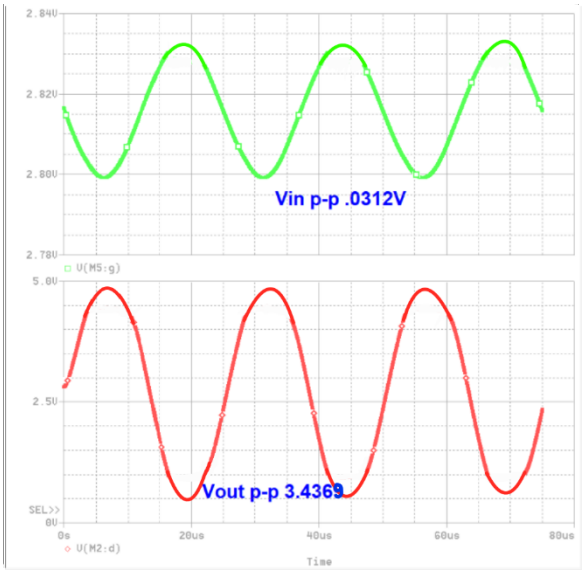


Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		0.000		
	X Values	0.000	0.000	0.000		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	V(M2:d)	2.5369	2.5369	0.000		-2.0002p	-2.0002p	2.5369	2.5369	2.5369
CURSOR 1,2	V(M1:d)	2.5369	2.5369	0.000		0.000	0.000	2.5369	2.5369	2.5369

Graphical representation of case 3 with an AV of 74.95 and Triple NMOS



Case 5 Quadruple NMOS with VAMPL of 21mV @ 40kHz



Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		1.6109		
	X Values	56.330u	41.412u	14.919u		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1	V(M2:d)	4.4413	1.0044	3.4369		0.000	-1.8261	4.4413	1.0044	2.7228
CURSOR 2	V(M5:g)	2.7992	2.8304	-31.212m		-1.6421	0.000	2.8304	2.7992	2.8148

Case 5 Graphical representation of an AV of 110.16

Lab 3: CMOS Transistor Level Utility Amplifier Design

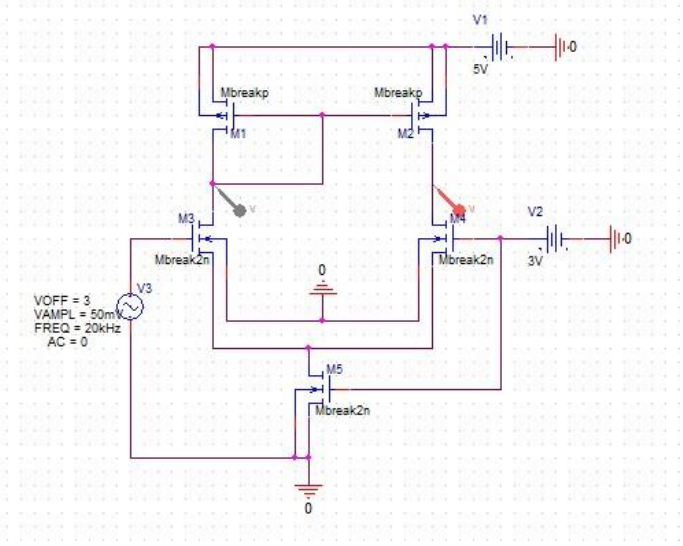
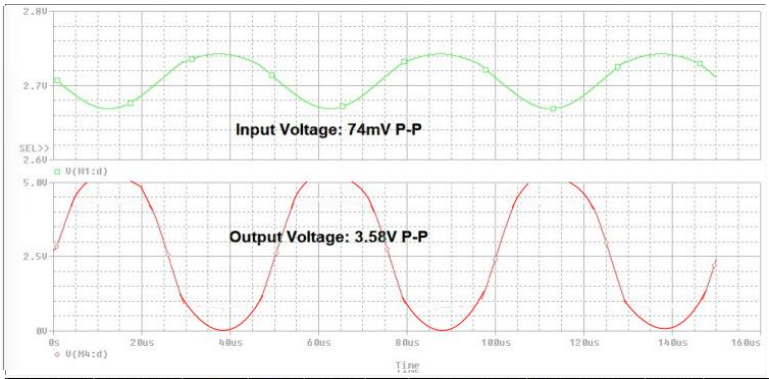


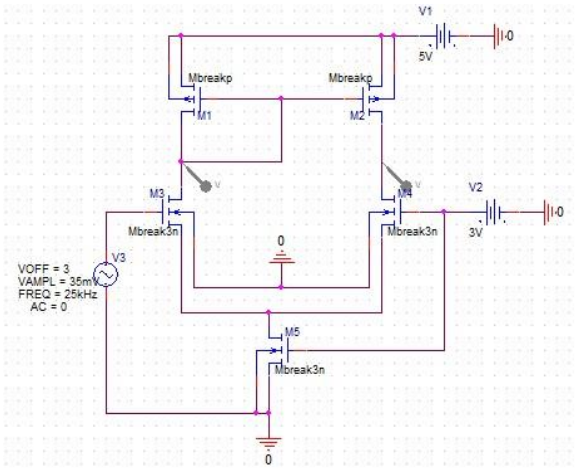
Figure 3.1: CMOS Transistor Amplifier Design with Double Sizing and V(m) @ 50mV and Freq @ 20kHz

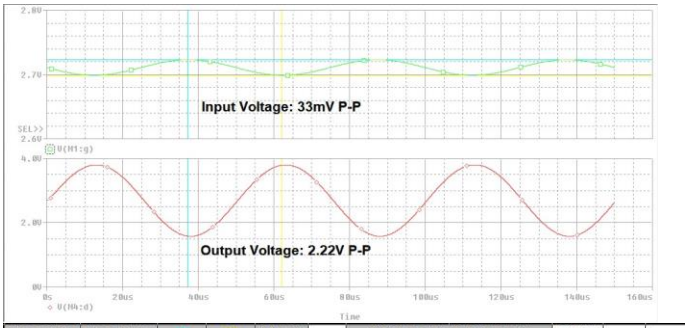


Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		73.618m		
	X Values	36.870u	62.783u	-25.912u		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	V(M4:d)	827.181m	4.4120	-3.5848		-1.9151	1.7433	4.4120	827.181m	2.6196
CURSOR 1,2	V(M1:d)	2.7423	2.6687	73.618m		0.000	0.000	2.7423	2.6687	2.7055

Figure 3.2: CMOS Transistor Amplifier Waveform and Cursor with Double Sizing and A(v) @ 48.38V

Figure 3.3: CMOS Transistor Amplifier Design with Triple Sizing and V(m) @ 35mV and Freq @ 25kHz





Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		24.142m		
	X Values	37.218u	62.088u	-24.869u		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	V(M4:d)	1.5866	3.7930	-2.2064		-1.1364	1.0942	3.7930	1.5866	2.6898
CURSOR 1,2	V(M1:g)	2.7230	2.6988	24.142m		0.000	0.000	2.7230	2.6988	2.7109

Figure 3.4: CMOS Transistor Amplifier Waveform and Cursor with Triple Sizing and A(v) @ 67.27V

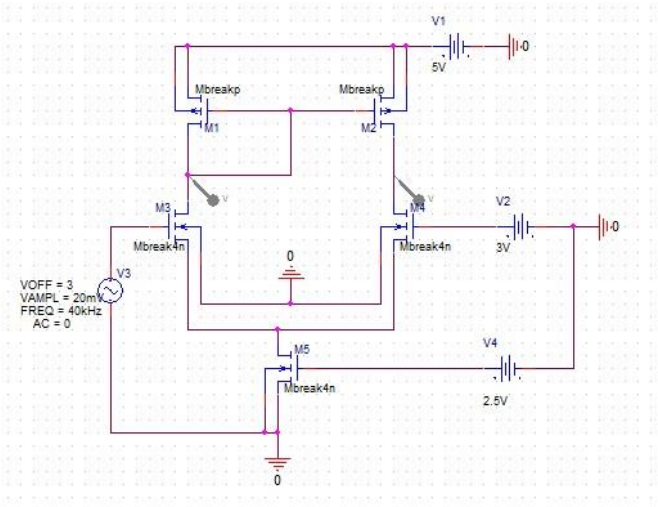
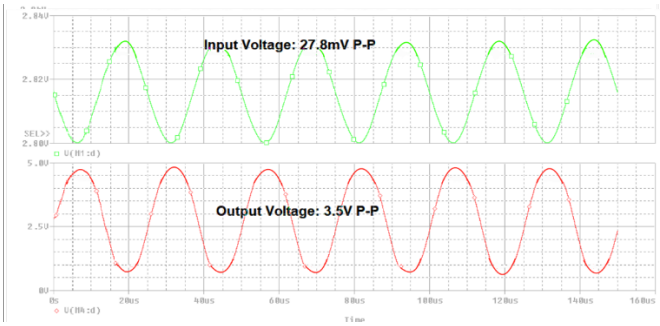


Figure 3.5: CMOS Transistor Amplifier Design with Quadruple Sizing and V(m) @



20mV and Freq @ 40kHz

Figure 3.6: CMOS Transistor Amplifier Waveform and Cursor with Quadruple Sizing and A(v) @ 125.9V

Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		-27.912m		
	X Values	56.348u	69.044u	-12.696u		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	V(M1:d)	2.8002	2.8281	-27.912m		0.000	0.000	2.8281	2.8002	2.8141
	V(M4:d)	4.4330	940.765m	3.4922		1.6328	-1.8873	4.4330	940.765m	2.6869

Conclusion:

This lab gave us the opportunity to understand the effects that certain sizing of NMOS transistors have on amplification properties of CMOS circuits. This lab is very important and needs to be taught all over the globe. This lab allowed for better understanding of how CMOS transistors function under certain constraints that were given in this lab.