California State University, Northridge

College of Engineering & Computer Science

Electrical and Computer Engineering Department

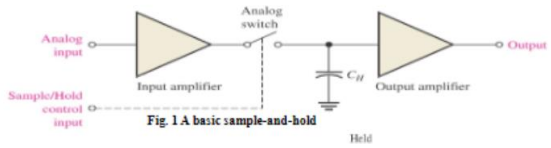
ECE 443L Digital Electronics Laboratory Report 7

CMOS based Sample and Hold Circuit Design, Simulation and Experimental Test as well as Analysis

By Evan Thomas, Haroutun Haroutunian

Abstract:

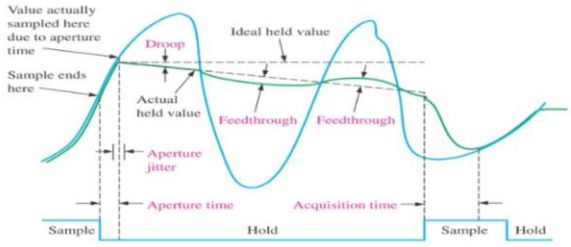
A sample and hold circuit samples an analog input voltage at a certain point in time and holds the sampled voltage for an extended time after the sample is taken. A sample and hold will keep the sampled analog voltage constant for the length of time necessary to allow an analog to digital converter (ADC) to convert the voltage to a digital form. A basic sample and hold circuit consist of an analog switch, a capacitor, and I/O-Amplifiers.



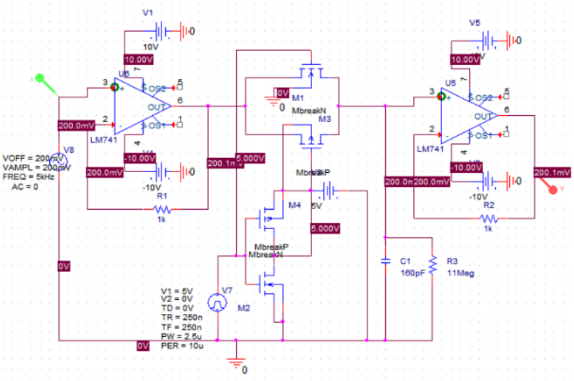
Basic Sample and hold circuit

Sample and hold specifications:

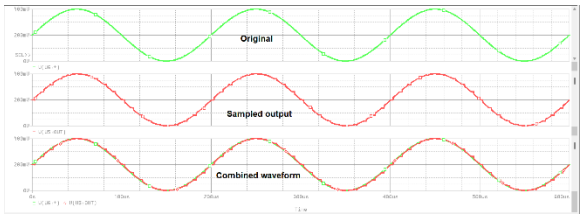
- Aperture time- the time for the analog switch to fully open after the contro voltge switches from its sample level to its hold level.
- Aperature jitter- the uncertainty in the aperature time
- Acquisition time – the time required for the device to reach its final value when the control voltage switches from its hold level to its sample level
- Droop – the change in voltage from the sampled value during the hold interval because of charge leaking off of the hold capacitor
- Feedthrough – the component of the output voltage that follows the input signal after the analog switch is opened. The inherent capacitance from the input to the output of the switches causes feedthrough



Author 1 Case 1, 3, and 5:

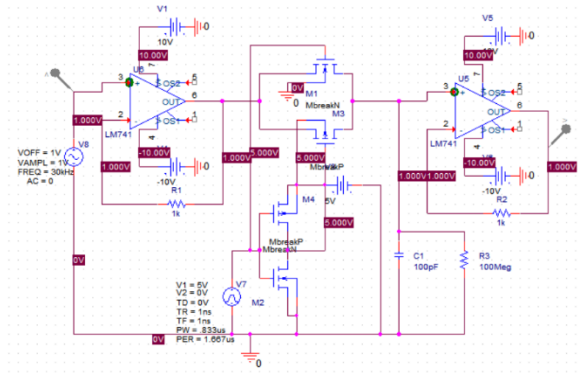


Case 1 @ 5kHz with 11Mega Ohm resistor and 160pF capacitor

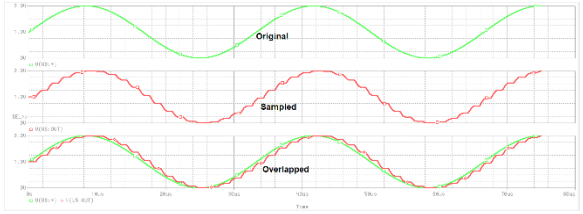


Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		0.000		
	X Values	0.000	0.000	0.000		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	V(U6:+)	200.016m	200.016m	0.000		15.708u	15.708u	200.016m	200.016m	200.016m
	V(U5:OUT)	200.078m	200.078m	0.000		78.394u	78.394u	200.078m	200.078m	200.078m
	V(U5:OUT)	200.078m	200.078m	0.000		78.394u	78.394u	200.078m	200.078m	200.078m
CURSOR 1,2	V(U6:+)	200.000m	200.000m	0.000		0.000	0.000	200.000m	200.000m	200.000m

Case 1 output when using the components from circuit

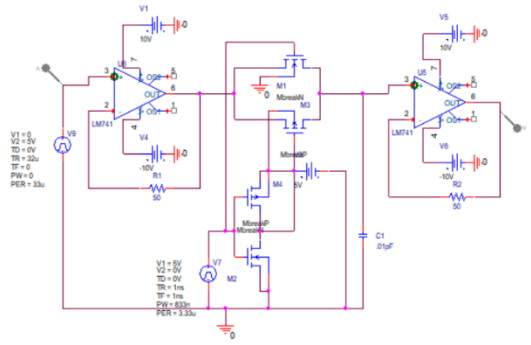


Case 3 circuit with 100pF capacitor and 100 Meg resistor running at a frequency of 30kHz

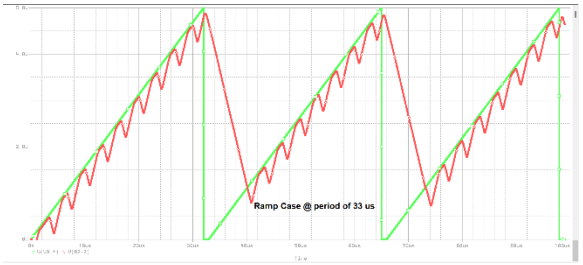


Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		0.000		
	X Values	0.000	0.000	0.000		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
	V(U6:+)	1.0000	1.0000	0.000		11.750u	11.750u	1.0000	1.0000	1.0000
	V(U5:OUT)	1.0000	1.0000	0.000		-2.2999p	-2.2999p	1.0000	1.0000	1.0000
CURSOR 1,2	V(U5:OUT)	1.0000	1.0000	0.000		0.000	0.000	1.0000	1.0000	1.0000
	V(U6:+)	1.0000	1.0000	0.000		11.750u	11.750u	1.0000	1.0000	1.0000

Case 3 waveform using the above components.



Case 5 Ramp circuit with a period of 33 micro seconds or about 30kHz and a .01pF capacitor paired with 50 ohm resistors.

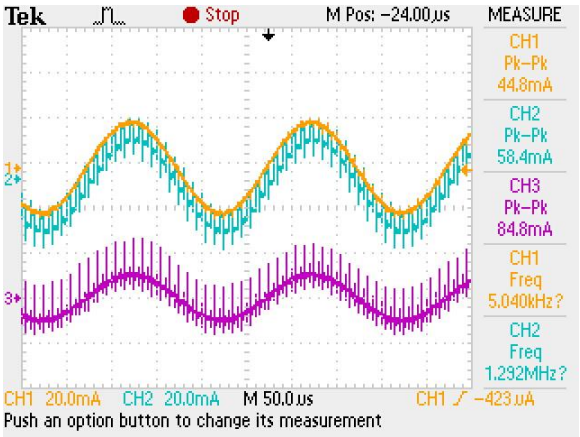


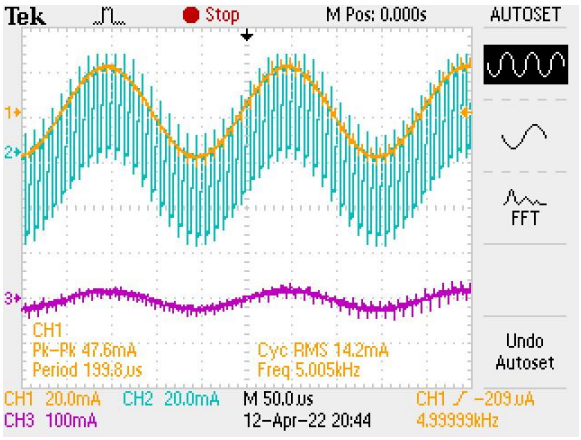
Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		5.0000		
	X Values	32.000u	0.000	32.000u		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	V(V9:+)	5.0000	0.000	5.0000		0.000	0.000	5.0000	0.000	2.5000
	V(R2:2)	4.7994	-750.655u	4.8002		-200.570m	-750.655u	4.7994	-750.655u	2.3993

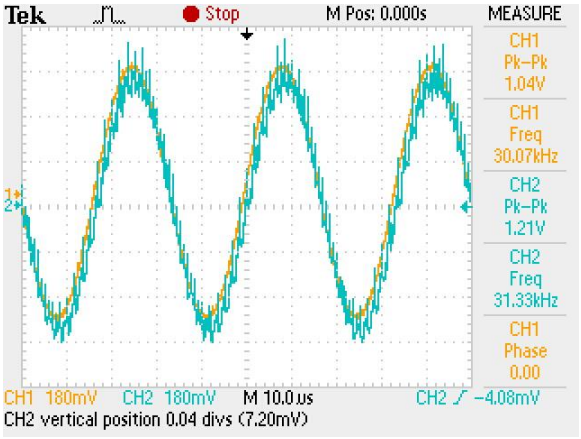
Discharge of the capacitor seems to stay constant and cannot match the ramp circuit perfectly.

Author 2 Case 2, 4, 6:

Experimental Results:







Author 1 Alternate case 1, 3, and 5:

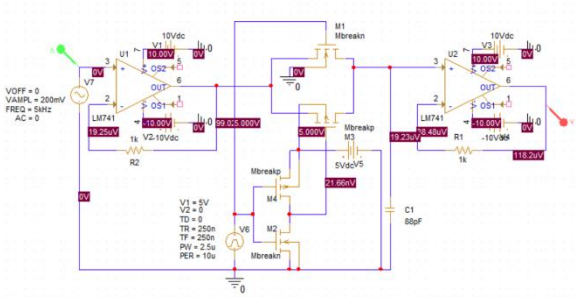
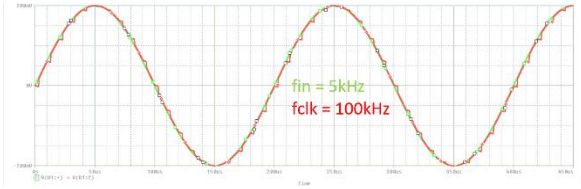


Fig 7.1 Sample and Hold Circuit, fin = 5kHz and fclk = 100khz.



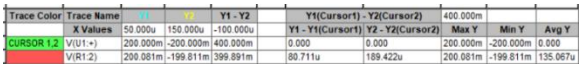


Fig 7.2 Sample and Hold simulation results, fin = 5kHz and fclk = 100khz.

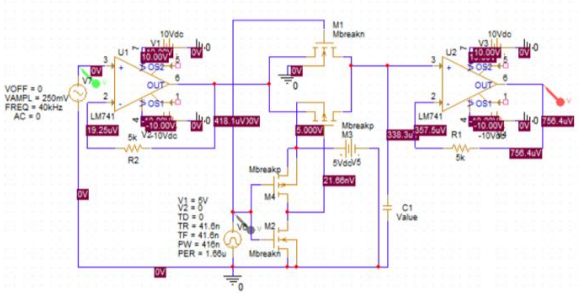
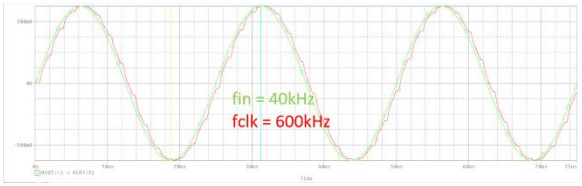


Fig 7.3 Sample and Hold Circuit, fin = 40kHz and fclk = 600khz.



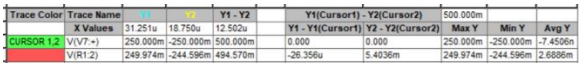


Fig 7.4 Sample and Hold simulation results, fin = 40kHz and fclk = 600khz.

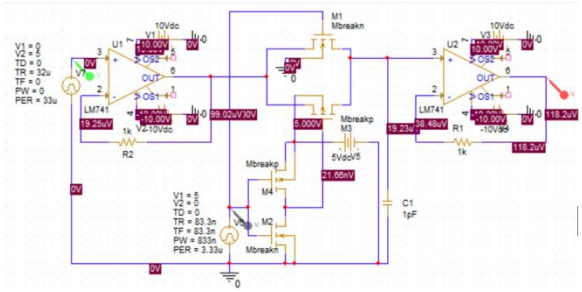
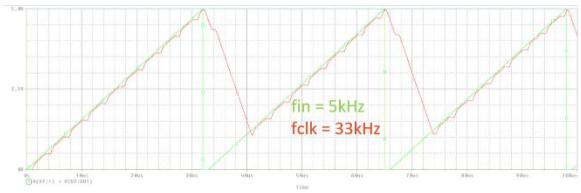


Fig 7.5 Sample and Hold Circuit, fin = 5kHz Ramp case and fclk = 33khz.



Trace Color	Trace Name	Y1	Y2	Y1 - Y2		Y1(Cursor1) - Y2(Cursor2)		5.0000		
	X Values	65.000u	0.000	65.000u		Y1 - Y1(Cursor1)	Y2 - Y2(Cursor2)	Max Y	Min Y	Avg Y
CURSOR 1,2	V(V7:+)	5.0000	0.000	5.0000		0.000	0.000	5.0000	0.000	2.5000
	V(U2:OUT)	4.9517	118.246u	4.9516		-48.330m	118.246u	4.9517	118.246u	2.4759

Fig 7.5 Sample and Hold simulation results, fin = 5kHz Ramp case and fclk = 33khz.

Conclusion:

In this lab we were able to simulate and experimentally show how a sample and hold circuit works.