USB ENGINEERING CHANGE NOTICE

Title: USB 2.0 DC Resistance

Applies to: Universal Serial Bus Specification, Revision 2.0

Summary of ECN

- Define the maximum series DC resistance (DCR) for D+ and D- in a Cable Assembly
- Define the maximum series DC resistance (DCR) for D+ and D- in high-speed capable Devices
- Define the maximum series DC resistance (DCR) for D+ and D- in high-speed capable Captive Devices
- Add a new compliance test specification for high-speed capable downstream facing ports to check for “False Connect” and “False Disconnect” events.
- Add a “Silicon Design Guide” to facilitate design of a proper disconnect threshold voltage level (V_{HSDSC}) to avoid “False Connect” and “False Disconnect” events.
- Provide new Eye Diagram Templates reflecting the impact of the new maximum DC resistance (DCR).
- Add a “Silicon Design Guide” to facilitate design of a proper Transmission Envelope Detector (Squelch Detector) based on host/device platform series DC resistance (DCR).

Reasons for ECN

The USB2.0 specification doesn’t define the DC resistance (DCR) on the D+ and D- data path between the silicon and the connector. The lack of a DCR requirement in the USB2.0 specification may cause false disconnect events when high-speed capable USB2 Hosts and Devices are connected. The excessive DCR on the D+ and D- data path may be caused by multiples crossbar switches and/or passive components such as common-mode chokes. A false disconnect event may occur when a high EOP level is present due to 1) a high reflection by high DCR of D+ and D- line and 2) a large output swing (V_{HSOH}) level being required to pass the eye diagram requirement at TP2.

A maximum DCR limit should be defined in the specification along with an appropriate disconnect threshold voltage level in the Host design to ensure the interoperability in the USB2 eco-systems when the maximum DCR channel is present.

Impact on Existing Peripherals and Systems

The DC resistance (DCR) specification for the Cable Assembly is relaxed from 0.6Ohms to 3.5Ohms. No impact on the existing Cable Assembly.

The DC Resistance (DCR) specification for high-speed capable Host/Devices or Captive Devices is new. The impact to the existing Host/Devices or Captive Devices is expected to be small as the maximum DCR limits (13ohms for Host/Dual Role Device, 17ohms for Device only Device - ie not Dual Role - and 23ohms for Captive Cable Device) were judiciously estimated to be sufficient for most implementations.

Hardware Implications:

No impact to the Cable Assembly design.

High-speed capable Device designs will have to consider the maximum DCR. Most Devices meet this requirement now.

High-speed capable Captive Device designs will have to consider the maximum DCR. Most Devices meet this requirement now.

High-speed capable Hosts will need to implement a Disconnect Threshold Voltage (V_{HSDSC}) level which interoperates in the USB2 eco-system with the maximum DCR defined in this ECN. Host designs would have already had to incorporate something similar to pass the USB2 Compliance with higher DCR between the silicon and the connector.

High-Speed capable Hosts and Devices will need to operate with potentially reduced signaling amplitude when a platform has the maximum DCR defined in this ECN. Signal detect threshold (squelch threshold) guidelines for platform DCR ranges are provided.

Software Implications:

There are no known software implications.

Compliance Testing Implications:

The following tests must be added to the compliance test specification.

- Check DCR of Cable Assembly
- Check DCR of high-speed capable Device by performing “false disconnect” test using a calibrated Golden Host
- Check DCR of high-speed capable Captive Device by performing “false disconnect” test using a calibrated Golden Host
- Perform “false disconnect” and “false connect” test for high-speed capable Host using the calibrated load which has the maximum DCR as defined in this ECN.

Specification Changes

(a). Section 6.6.3 Electrical Characteristics

Table 7-1. Description of Functional Elements in the Example Shown in Figure 7-1

From Text:

The DC resistance from plug shell to plug shell (or end of integrated cable) must be less than 0.6 ohms.

To Text:

The DC resistance from plug shell to plug shell (or end of integrated cable) must be less than 3.5 ohms.

(b). Section 7.1, Table 7-1

From Table:

Table 7-1. Description of Functional Elements in the Example Shown in Figure 7-1

Element	Description
Transmission Envelope Detector	This envelope detector is used to indicate that data is invalid when the amplitude of the differential signal at a receiver's inputs falls below the squelch threshold (V_{HSSQ}). It must indicate Squelch when the signal drops below 100 mV differential amplitude, and it must indicate that the line is not in the Squelch state when the signal exceeds 150 mV differential amplitude. The response time of the detector must be fast enough to allow a receiver to detect data transmission, to achieve DLL lock, and to detect the end of the SYNC field within 12 bit times, the minimum number of SYNC bits that a receiver is guaranteed to see. This envelope detector must incorporate a filtering mechanism that prevents indication of squelch during the longest differential data transitions allowed by the receiver eye pattern specifications.
Disconnection Envelope Detector	**This envelope detector is required in downstream facing ports to detect the high- speed Disconnect state on the line (VHSDSC). Disconnection must be indicated when the amplitude of the differential signal at the downstream facing driver's connector ≥625 mV, and it must not be indicated when the signal amplitude is ≤525 mV. The output of this detector is sampled at a specific time during the transmission of the high-speed SOF EOP, as described in Section 7.1.7.3.**
Pull-up Resistor (RPU)	**This resistor is required only in upstream facing transceivers and is used to indicate signaling speed capability. A high-speed capable device is required to initially attach as a full-speed device and must transition to high-speed as described in this specification. Once operating in high-speed, the 1.5 kΩ resistor must be electrically removed from the circuit. In Figure 7-1, a control line called RPU_Enable is indicated for this purpose. The preferred embodiment is to attach matched switching devices to both the D+ and D- lines so as to keep the lines' parasitic loading balanced, even though a pull-up resistor must never be used on the D- line of an upstream facing high-speed capable transceiver. When connected, this pull-up must meet all the specifications called out for full- speed operation.**

Pull-down Resistor (RPD)	**These resistors are required only in downstream facing transceivers and must conform to the same specifications called out for low-speed and full-speed operation.**

To Table:

Table 7-1. Description of Functional Elements in the Example Shown in Figure 7-1

Element	Description
Transmission Envelope Detector	This envelope detector is used to indicate that data is invalid when the amplitude of the differential signal at a receiver's inputs falls below the squelch threshold (V_{HSSQ}) as determined by Silicon design guide for Squelch Detection, shown in Figure 7-New3, which is a function of host/device platform DCR. The response time of the detector must be fast enough to allow a receiver to detect data transmission, to achieve DLL lock, and to detect the end of the SYNC field within 12 bit times, the minimum number of SYNC bits that a receiver is guaranteed to see. This envelope detector must incorporate a filtering mechanism that prevents indication of squelch during the longest differential data transitions allowed by the receiver eye pattern specifications.
Disconnection Envelope Detector	**This envelope detector is required in downstream facing ports to detect the high- speed Disconnect state on the line (VHSDSC). A downstream facing transceiver operating in high-speed mode must implement a proper disconnect threshold voltage (V_{HSDSC}) level to ensure the interoperability in the USB2 eco-systems with the maximum DCR channel defined in the specification. Silicon design guide for Disconnect Threshold Voltage (V_{HSDSC}) implementation is shown in Figure 7-new. The output of this detector is sampled at a specific time during the transmission of the high-speed SOF EOP, as described in Section 7.1.7.3.**
Pull-up Resistor (RPU)	**This resistor is required only in upstream facing transceivers and is used to indicate signaling speed capability. A high-speed capable device is required to initially attach as a full-speed device and must transition to high-speed as described in this specification. Once operating in high-speed, the 1.5 kΩ resistor must be electrically removed from the circuit. In Figure 7-1, a control line called RPU_Enable is indicated for this purpose. The preferred embodiment is to attach matched switching devices to both the D+ and D- lines so as to keep the lines' parasitic loading balanced, even though a pull-up resistor must never be used on the D- line of an upstream facing high-speed capable transceiver. When connected, this pull-up must meet all the specifications called out for full- speed operation.**
Pull-down Resistor (RPD)	**These resistors are required only in downstream facing transceivers and must conform to the same specifications called out for low-speed and full-speed operation.**
DC Resistance (D+, D-)	**The series DC resistance of D+ and D- lines, individually, must be equal or less than 13Ω for a high-speed host/hub or dual role device, 17Ω for a high-speed Device only Device, and equal or less than 23Ω for a high-speed capable captive cable device. Maximum total series resistance for each line (host/hub, connectors, cable, device) is 36Ω.** *** Please refer "USB Type-C Specification" for the maximum series DC resistance of D+ and D- lines of Type-C Device and Type-C Captive Device.**

(a). Section 7.1.1.3 High-speed (480Mb/s) Driver Characteristics

From Text:

A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance (Z_0) of 90 Ω ±15%, a common mode impedance (Z_{CM}) of 30 Ω ±30%, and a maximum one-way delay of 26 ns (T_{FSCBL}). The D+ and D- circuit board traces which run between a transceiver and its associated connector should also have a nominal differential impedance of 90 Ω, and together they may add an additional 4 ns of delay between the transceivers. (See Section 7.1.6 for details on impedance specifications of boards and transceivers.) The differential output impedance of a high-speed capable driver is required to be 90 Ω ±10%. When either the D+ or D- lines are driven high, V_{HSOH} (the high-speed mode high-level output voltage driven on a data line with a precision 45 Ω load to GND) must be 400 mV ±10%. On a line which is not driven, either because the transceiver is not transmitting or because the opposite line is being driven high, V_{HSOL} (the highspeed mode low-level output voltage driven on a data line with a 45 Ω load to GND) must be 0 V ± 10 mV.

To Text:

A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance (Z_0) of 90 Ω ±15%, a common mode impedance (Z_{CM}) of 30 Ω ±30%, and a maximum one-way delay of 26 ns (T_{FSCBL}). The D+ and D- circuit board traces which run between a transceiver and its associated connector should also have a nominal differential impedance of 90 Ω, and together they may add an additional 4 ns of delay between the transceivers. (See Section 7.1.6 for details on impedance specifications of boards and transceivers.) The differential output impedance of a high-speed capable driver is required to be 90 Ω ±10%. When either the D+ or D- lines are driven high, V_{HSOH} (the high-speed mode high-level output voltage driven on a data line with a precision 45 Ω load to GND) must be between 360mV and 625mV. On a line which is not driven, either because the transceiver is not transmitting or because the opposite line is being driven high, V_{HSOL} (the highspeed mode low-level output voltage driven on a data line with a 45 Ω load to GND) must be 0 V ± 10 mV.

(b). Section 7.1.2.2, Figure 7-13. Template 1

From Table:

	Voltage Level (D+ - D-)	Time (% of Unit Interval)
Level 1	525 mV in UI following a transition, 475 mV in all others	N/A
Level 2	-525 mV in UI following a transition, -475 in all others	N/A

To Table:

	Voltage Level (D+ - D-)	Time (% of Unit Interval)
Level 1	625 mV	N/A
Level 2	-625 mV	N/A

(d). Section 7.1.2.2, Figure 7-14. Template 2

From Table:

	Voltage Level (D+ - D-)	Time (% of Unit Interval)
Level 1	525 mV in UI following a transition, 475 mV in all others	N/A
Level 2	-525 mV in UI following a transition, -475 in all others	N/A

To Table:

	Voltage Level (D+ - D-)	Time (% of Unit Interval)
Level 1	575 mV	N/A
Level 2	-575 mV	N/A

(g). Section 7.1.2.2, Figure 7-17. Template 5

Note: This is an informative requirement.

(h). Section 7.1.2.2, Figure 7-18. Template 6

Note: This is an informative requirement.

In an actual USB2 link with a high DCR load, the amplitude at the local receptacle connector of the transmitter may be as high as 700mV differential.

Depending on the series DCR in an actual USB2 link and given 150mV amplitude at the local receptacle connector of the receiver, the amplitude at the receiver pins/balls may be as low as 100mV differential. Table 7-new2 provides Rx amplitude vs. series DCR with a range of AC loss of 0dB and .867dB.

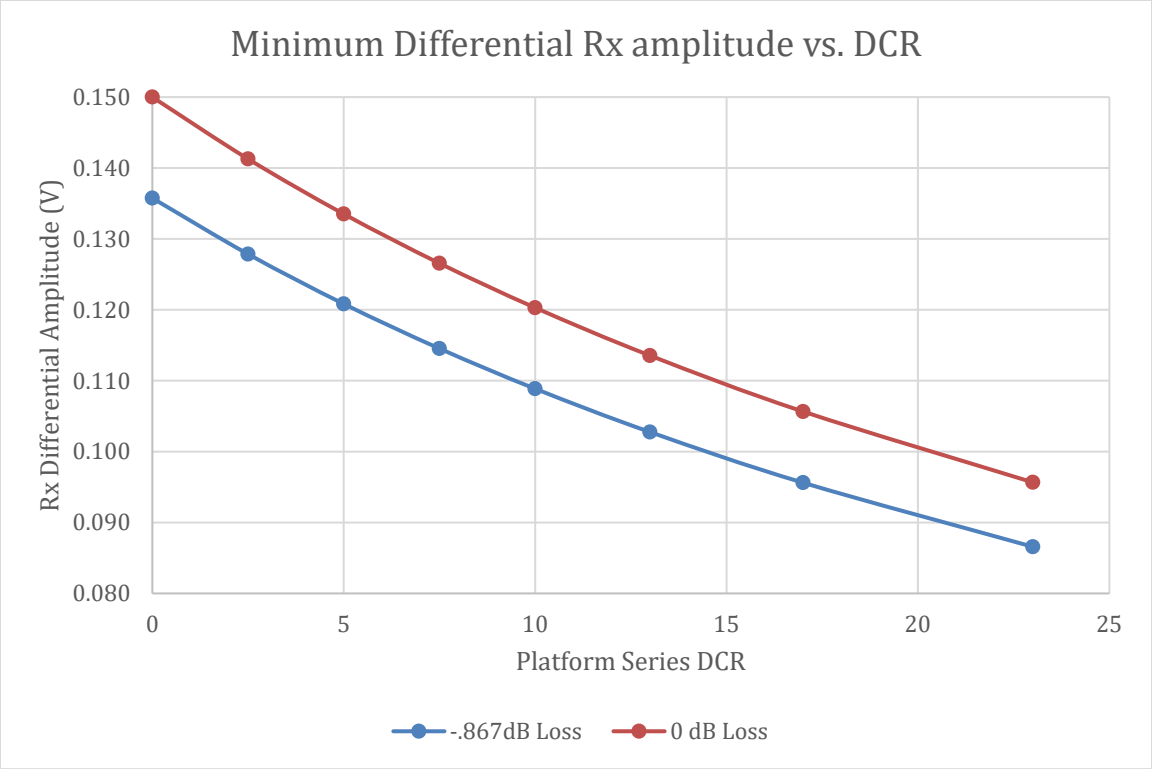

Figure 7-New2. Silicon Design Guide for minimum Rx Amplitude

Notes: Series DCR up to 13 Ω is applicable for a Host, Dual Role Data or Device with Type-C connector.
Series DCR up to 17Ω is only applicable for a Device (ie not Host or Dual Role Data) with Type-C connector..
Series DCR up to 23Ω is only applicable for a Device with a captive cable.

(i). Section 7.1.4.2

From Text:

Reception of data is qualified by the output of the transmission envelope detector. The receiver must disable data recovery when the signal falls below the high-speed squelch level (V_{HSSQ}) defined in Table 7-3. (Detector must indicate squelch when the magnitude of the differential voltage envelope is ≤ 100 mV, and must not indicate squelch if the amplitude of differential voltage envelope is ≥ 150 mV.) Squelch detection must be done with a differential envelope detector, such as the one shown in Figure 7-1. The envelope detector used to detect the squelch state must incorporate a filtering mechanism that prevents indication of squelch during differential data crossovers.

To Text:

Reception of data is qualified by the output of the transmission envelope detector. A receiver must not disable data recovery when the signal is above the minimum amplitude that may appear at its pins/balls. Figure 7-New3 provides a guideline for setting the high-speed squelch level (V_{HSSQ}) level for a host/hub/device based on the local DCR and assuming 150mV amplitude at TP3 for a device or TP2 for a host/hub. Note that the DCR referred to is only for the portion of the system in which the host/hub/device resides. The rest of the system (cable, far end device and its platform) is considered at max DCR range. It is recommended that V_{HSSQ} not fall below 50mV. Squelch detection must be done with a differential envelope detector, such as the one shown in Figure 7-1. The envelope detector used to detect the squelch state must incorporate a filtering mechanism that prevents indication of squelch during differential data crossovers.

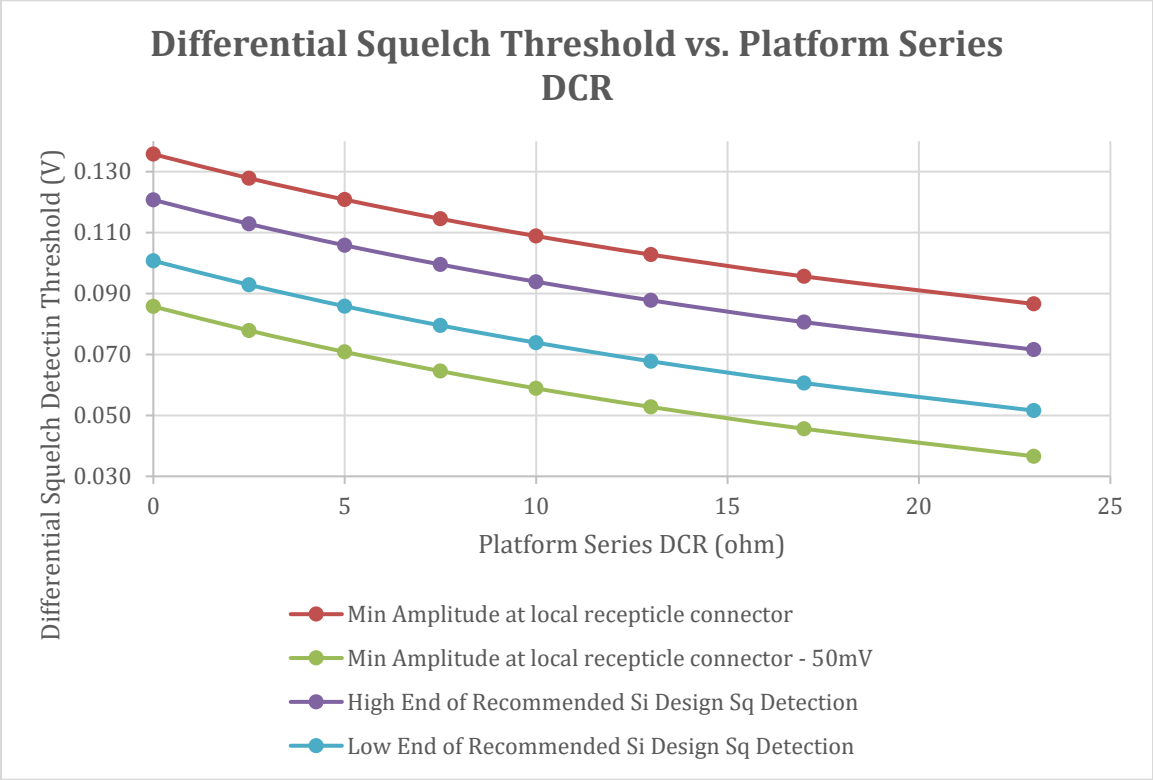

Figure 7-New3. Silicon Design Guide for Squelch Threshold Voltage (V_{HSSQ}) Implementation
Notes: Series DCR up to 13 Ω is applicable for a Host, Dual Role Data or Device with Type-C connector.
Series DCR up to 17Ω is only applicable for a Device (ie not Host or Dual Role Data) with Type-C connector..
Series DCR up to 23Ω is only applicable for a Device with a captive cable.

From Text:

In the case of a downstream facing port, a high-speed capable transceiver must include a differential envelope detector that indicates when the signal on the data exceeds the high-speed Disconnect level (VHSDSC) as defined in Table 7-3. (The detector must not indicate that the disconnection threshold has been exceeded if the differential signal amplitude is ≤525 mV, and must indicate that the threshold has been exceeded if the differential signal amplitude is ≥625 mV.)

To Text:

In the case of a downstream facing port, a high-speed capable transceiver must include a differential envelope detector that indicates when the signal on the data exceeds the high-speed Disconnect level (VHSDSC) as defined in Table 7-3. A downstream facing port operating in high-speed mode must implement a proper disconnect threshold voltage (V_{HSDSC}) level to ensure the interoperability in the USB2 eco-systems with the maximum DCR channel defined in the specification. Silicon design guide for Disconnect Threshold Voltage (V_{HSDSC}) implementation is shown in Figure 7-new.

(j). Section 7.1.7.2, Table 7-3

From Table:

High-speed Squelch State	NA	V_{HSSQ} - Receiver must indicate squelch when magnitude of differential voltage is ≤100 mV; receiver must not indicate squelch if magnitude of differential voltage is ≥150 mV. See Note 3.
High-speed Disconnect State (at downstream facing port)	**NA**	**VHSDSC - Downstream facing port must not indicate device disconnection if differential voltage is ≤ 525 mV, and must indicate device disconnection when magnitude of differential voltage is ≥ 625 mV, at the sample time discussed in Section 7.1.7.3.**

To Table:

High-speed Squelch State	NA	V_{HSSQ} – A receiver must detect valid signaling with the minimum voltage applied at TP2/TP3 as shown in Template 4. Designers may use the Silicon Design Guide for Squelch Detection (Figure 7-New3) to accommodate for their signal amplitude based on their supported local platform DCR. It is recommended that the Squelch Detection threshold be no lower than 50mV at TP1/TP4. See Note 3.
High-speed Disconnect State (at downstream facing port)	**NA**	**VHSDSC - A downstream facing port operating in high-speed mode must implement a proper disconnect threshold**

		voltage (V_{HSDSC}) level to ensure the interoperability in the USB2 eco-systems with the maximum DCR channel defined in the specification. Silicon design guide for Disconnect Threshold Voltage (V_{HSDSC}) implementation is shown in Figure 7-new.

(k). Section 7.1.7.3 Connect and Disconnect Signaling

From Text:

A downstream facing transceiver operating in high-speed mode detects disconnection of a high-speed device by sensing the doubling in differential signal amplitude across the D+ and D- lines that can occur when the device terminations are removed. The Disconnection Envelope Detector output goes high when the downstream facing transceiver transmits and positive reflections from the open line return with a phase which is additive with the transceiver driver signal. Signals with differential amplitudes ≥ 625 mV must reliably activate the Disconnection Envelope Detector. Signals with differential amplitudes ≤ 525 mV must never activate the Disconnection Envelope Detector.

To Text:

A downstream facing transceiver operating in high-speed mode detects disconnection of a high-speed device by sensing the doubling in differential signal amplitude across the D+ and D- lines that can occur when the device terminations are removed. The Disconnection Envelope Detector output goes high when the downstream facing transceiver transmits and positive reflections from the open line return with a phase which is additive with the transceiver driver signal. A downstream facing transceiver operating in high-speed mode must implement a proper disconnect threshold voltage (V_{HSDSC}) level to ensure the interoperability in the USB2 eco-systems with the maximum DCR channel defined in the specification. Silicon design guide for Disconnect Threshold Voltage (V_{HSDSC}) implementation is shown in Figure 7-new.

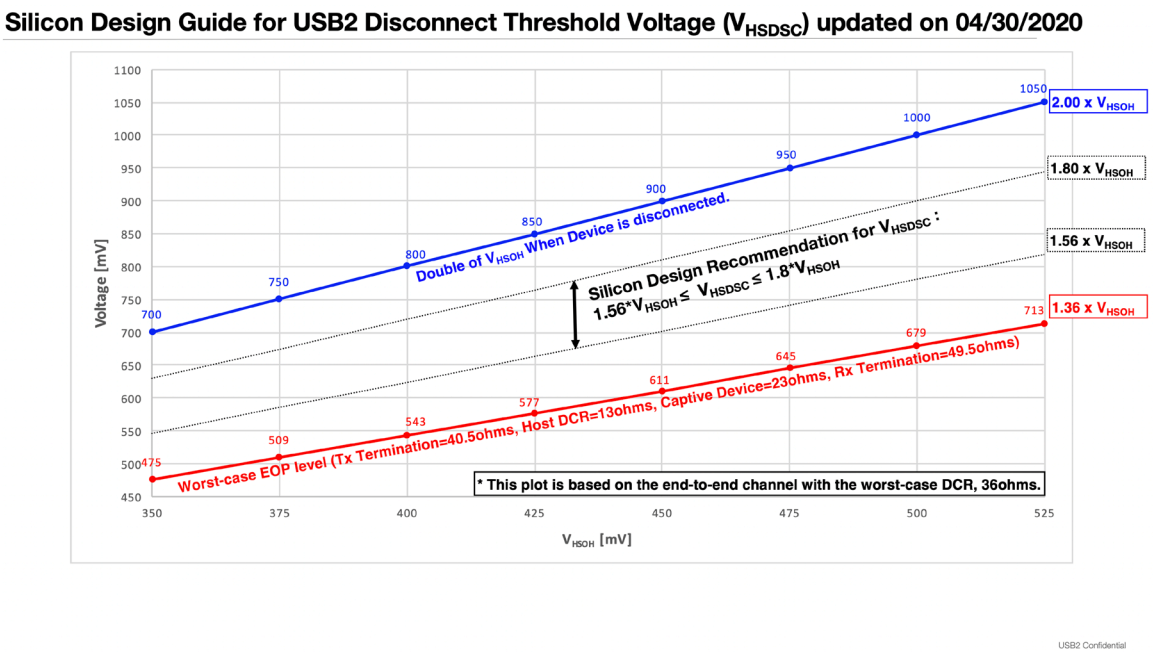

Figure 7-new. Silicon Design Guide for Disconnect Threshold Voltage (V_{HSDSC}) Implementation

(I). Section 7.1.17 Cable Attenuation

From Text:

USB cables must not exceed the loss figures shown in Table 7-6. Between the frequencies called out in the table, the cable loss should be no more than is shown in the accompanying graph.

To Text:

The series DC resistance of D+ or D- in a USB cable must not exceed 3.5 Ω. USB cables must not exceed the loss figures shown in Table 7-6. Between the frequencies called out in the table, the cable loss should be no more than is shown in the accompanying graph.

(m). Section 7.3.2, Table 7-7

From Table:

Table 7-7. DC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Max.	Units
High-speed squelch detection threshold (differential signal amplitude)	V_{HSSQ}	Section 7.1.7.2 (specification refers to differential signal amplitude)	100	150	mV

Parameter	Symbol	Conditions	Min.	Max.	Units
High speed disconnect detection threshold (differential signal amplitude)	**VHSDSC**	**Section 7.1.7.2 (specification refers to differential signal amplitude)**	**525**	**625**	**mV**

High-speed data signaling high	V_{HSOH}	Section 7.1.7.2	360	440	mV

To Table:

Table 7-7. DC Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Max.	Units
High-speed squelch detection threshold (differential signal amplitude)	V_{HSSQ}	Section 7.1.7.2 (specification refers to differential signal amplitude)	Refer Silicon Design Guide for Squelch Detection Implementation in Figure 7-New3. 50mV is the minimum recommended value over all conditions.	Refer Silicon Design Guide for Squelch Detection Implementation in Figure 7-New3. Valid signaling must be received with the minimum voltage applied at TP2/TP3 as shown in Templates 3 and 4.	mV

High speed disconnect detection threshold (differential signal amplitude)	**VHSDSC**	**Section 7.1.7.2 (specification refers to differential signal amplitude)**	**525**	**Refer Silicon Design Guide for Disconnect Threshold Voltage (VHSDSC) Implementation in Figure 7-new**	**mV**
High-speed data signaling high	V_{HSOH}	Section 7.1.7.2	360	625	mV

(n). Section 7.3.2, Table 7-12

New row:

Table 7-12. Cable Characteristics (Note 14)

Parameter	Symbol	Conditions	Min	Max	Units
Cable DCR (D+, D-)				**3.5**	**Ω**