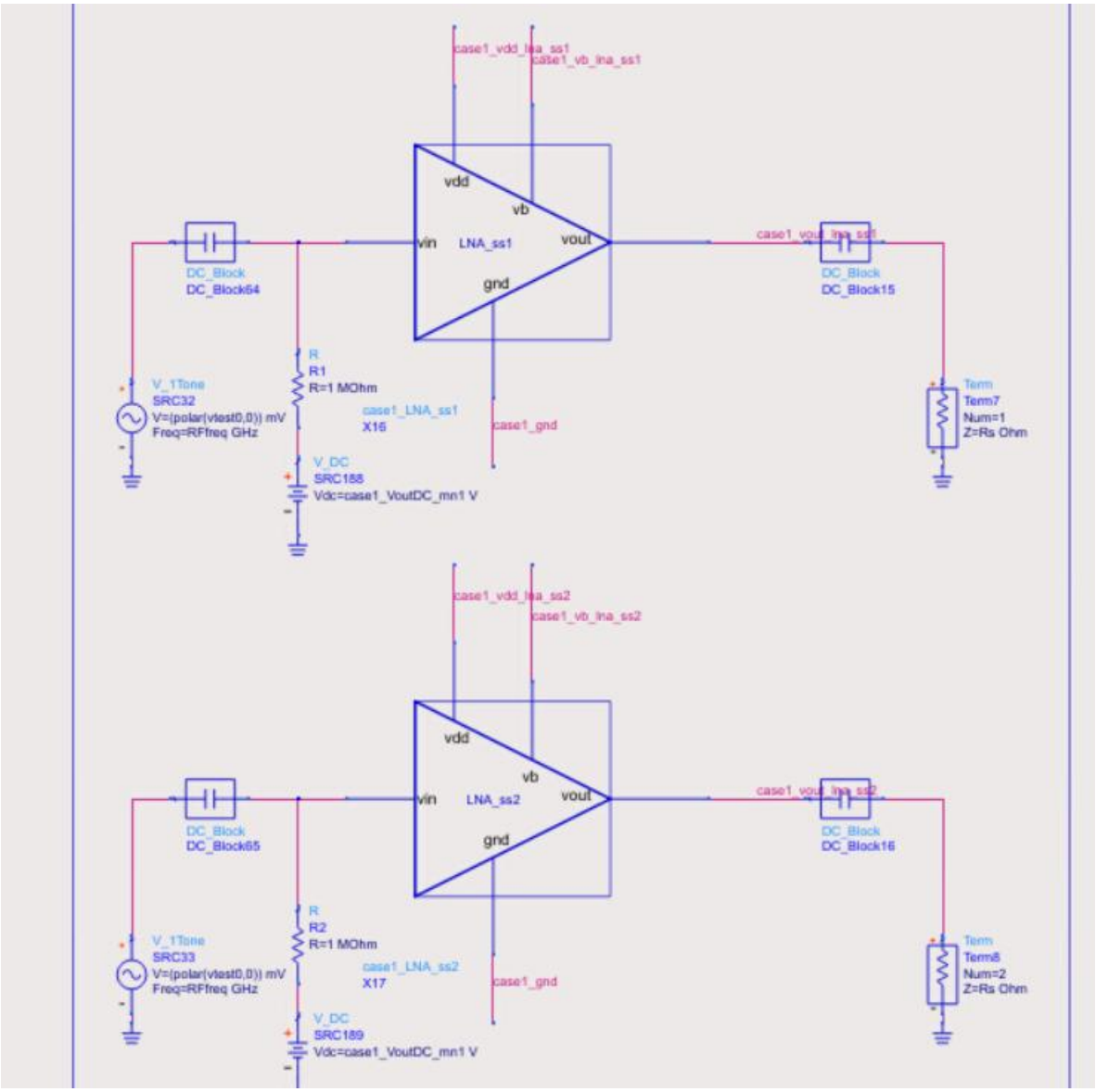
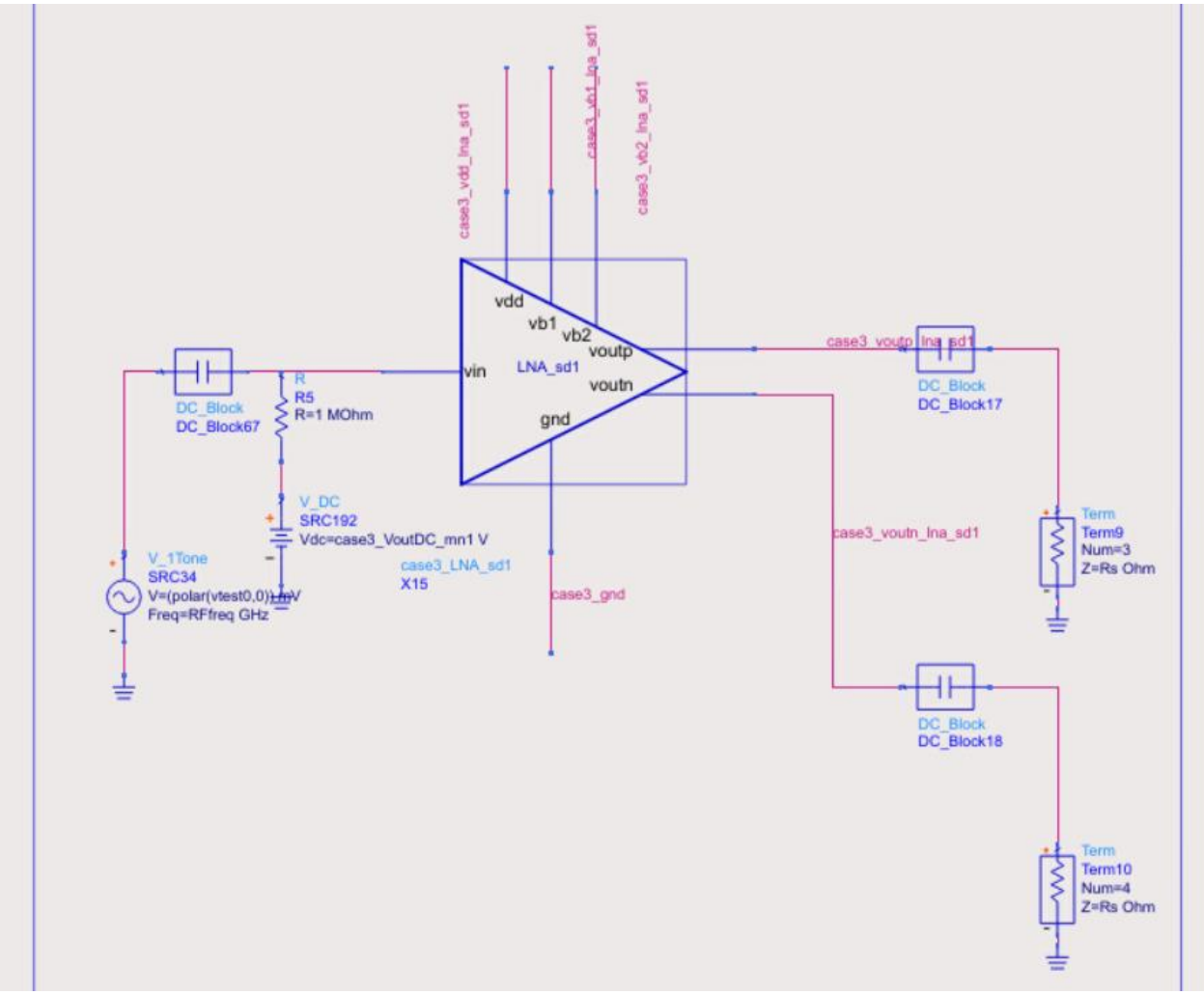
1. Sequential, Loading-aware Flow

1) DC simulation to extract DC bias voltages in the output

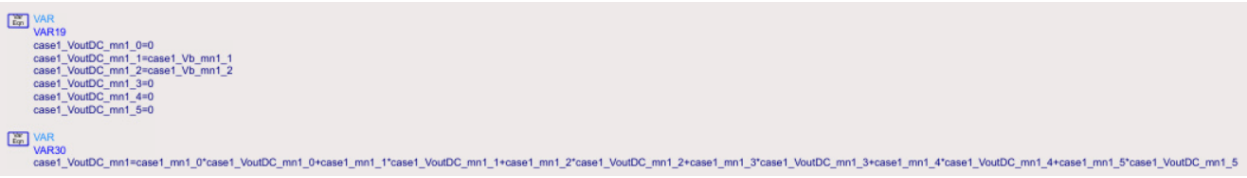
(1) DC_VDC1 (DC output from MN1, LNA, MN2)

Only the active components (LNA, ADD, MX) need simulations.

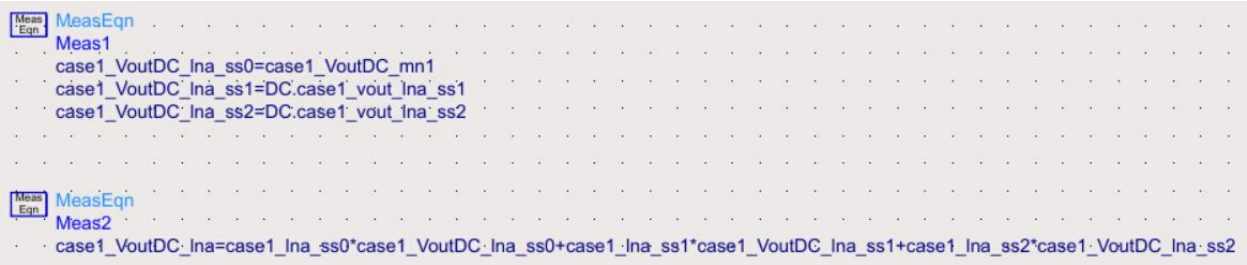




- VoutDC_mn1



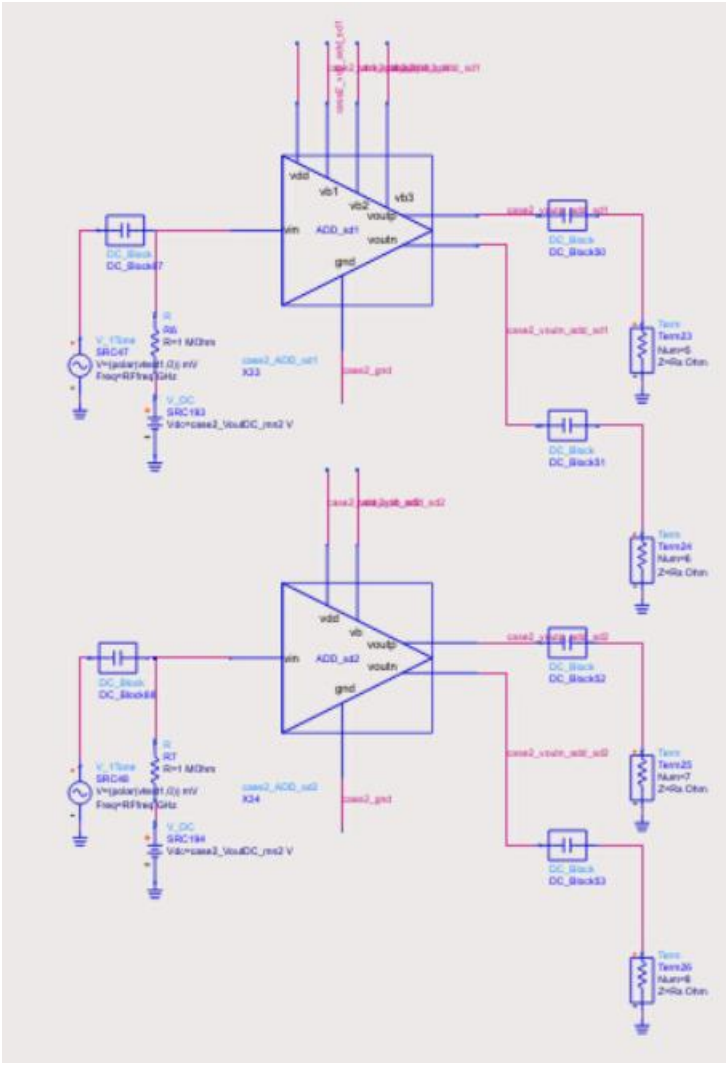
- VoutDC_lna

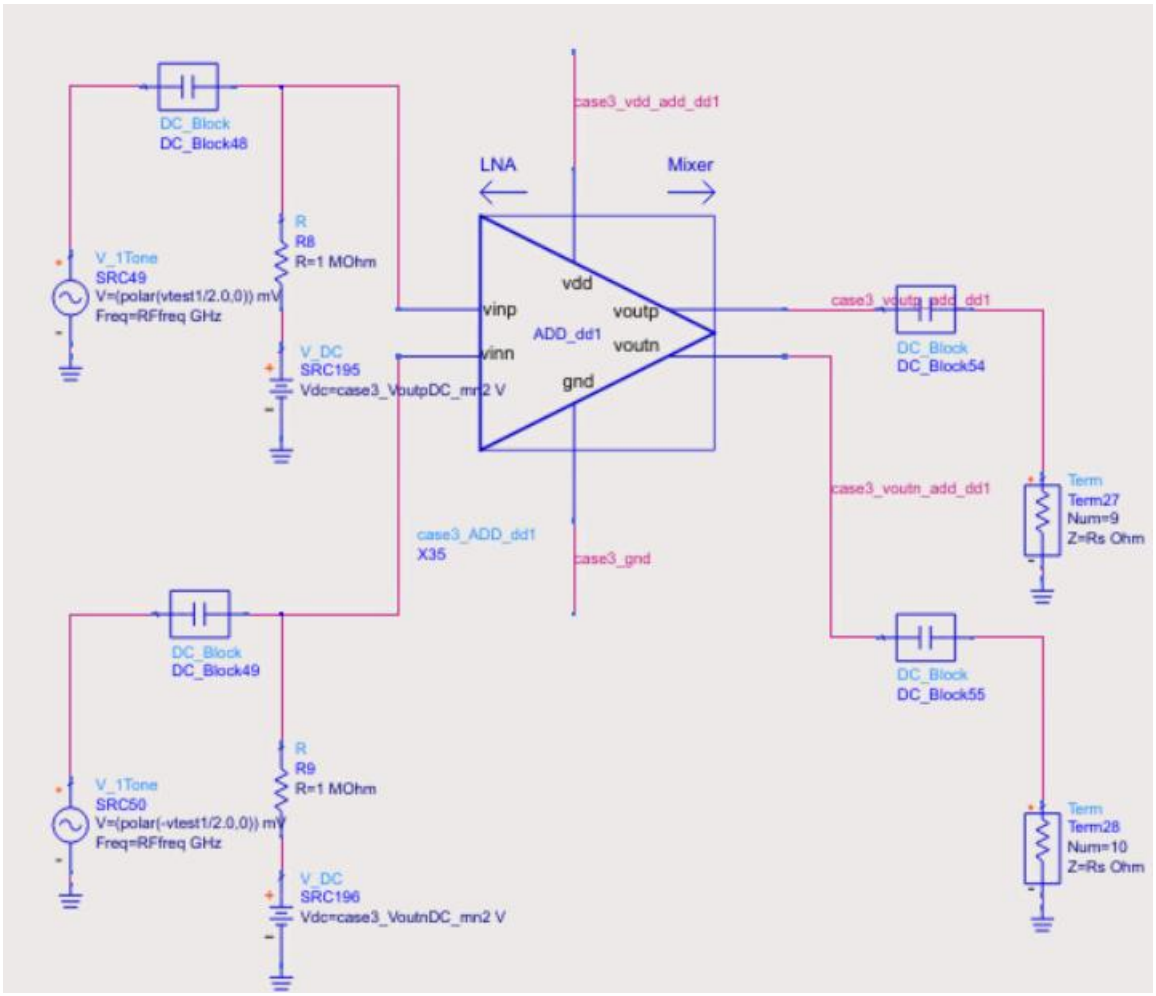


- VoutDC_mn2

```
MeasEqn
Meas4
case1_VoutDC_mn2_0=case1_VoutDC_lna
case1_VoutDC_mn2_1=case1_Vb_mn2_1
case1_VoutDC_mn2_2=case1_Vb_mn2_2
case1_VoutDC_mn2_3=case1_VoutDC_lna
case1_VoutDC_mn2_4=0
case1_VoutDC_mn2_5=case1_VoutDC_lna

MeasEqn
Meas6
case1_VoutDC_mn2=case1_mn2_0*case1_VoutDC_mn2_0+case1_mn2_1*case1_VoutDC_mn2_1+case1_mn2_2*case1_VoutDC_mn2_2+case1_mn2_3*case1_VoutDC_mn2_3+case1_mn2_4*case1_VoutDC_mn2_4+case1_mn2_5*case1_VoutDC_mn2_5
```

(2) DC_VDC2 (ADD, MN3)





- VoutpDC_add, VoutnDC_add, VoutDC_add

```
MeasEqn
Meas8
case2_VoutpDC_add_sd1=DC.case2_voutp_add_sd1
case2_VoutnDC_add_sd1=DC.case2_voutn_add_sd1
case2_VoutpDC_add_sd2=DC.case2_voutp_add_sd2
case2_VoutnDC_add_sd2=DC.case2_voutn_add_sd2

MeasEqn
Meas9
case2_VoutpDC_add=case2_add_sd1*case2_VoutpDC_add_sd1+case2_add_sd2*case2_VoutpDC_add_sd2
case2_VoutnDC_add=case2_add_sd1*case2_VoutnDC_add_sd1+case2_add_sd2*case2_VoutnDC_add_sd2
```

```
MeasEqn
Meas10
case3_VoutpDC_add_dd0=case3_VoutpDC_mn2
case3_VoutnDC_add_dd0=case3_VoutnDC_mn2
case3_VoutpDC_add_dd1=DC.case3_voutp_add_dd1
case3_VoutnDC_add_dd1=DC.case3_voutn_add_dd1

MeasEqn
Meas11
case3_VoutpDC_add=case3_add_dd0*case3_VoutpDC_add_dd0+case3_add_dd1*case3_VoutpDC_add_dd1
case3_VoutnDC_add=case3_add_dd0*case3_VoutnDC_add_dd0+case3_add_dd1*case3_VoutnDC_add_dd1
```

- VoutDC_mn3, VoutpDC_mn3, VoutnDC_mn3

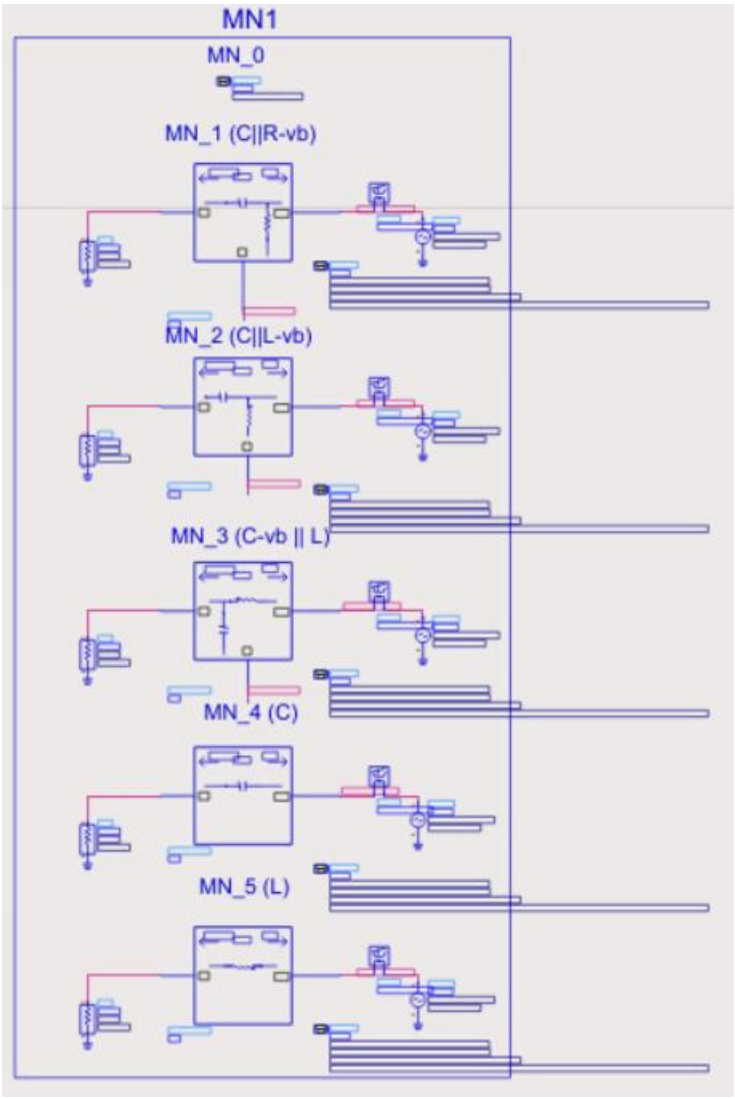
```
MeasEqn
Meas4
case1_VoutDC_mn3_0=case1_VoutDC_add
case1_VoutDC_mn3_1=case1_Vb_mn3_1
case1_VoutDC_mn3_2=case1_Vb_mn3_2
case1_VoutDC_mn3_4=0

MeasEqn
Meas6
case1_VoutDC_mn3=case1_mn3_0*case1_VoutDC_mn3_0+case1_mn3_1*case1_VoutDC_mn3_1+case1_mn3_2*case1_VoutDC_mn3_2+case1_mn3_4*case1_VoutDC_mn3_4
```

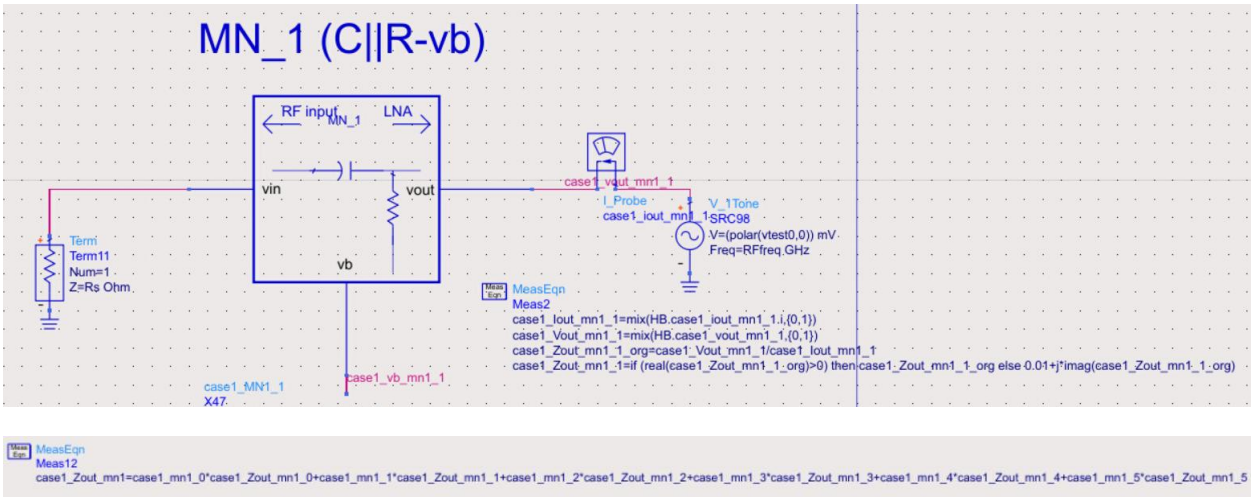
```
VAR
VAR78
case2_VoutpDC_mn3_1=case2_Vb_mn3_1_p
case2_VoutnDC_mn3_1=case2_Vb_mn3_1_n
case2_VoutpDC_mn3_2=case2_Vb_mn3_2_p
case2_VoutnDC_mn3_2=case2_Vb_mn3_2_n
case2_VoutpDC_mn3_4=0
case2_VoutnDC_mn3_4=0

VAR
VAR79
case2_VoutpDC_mn3=case2_mn3_1_p*case2_VoutpDC_mn3_1+case2_mn3_2_p*case2_VoutpDC_mn3_2+case2_mn3_4_p*case2_VoutpDC_mn3_4
case2_VoutnDC_mn3=case2_mn3_1_n*case2_VoutnDC_mn3_1+case2_mn3_2_n*case2_VoutnDC_mn3_2+case2_mn3_4_n*case2_VoutnDC_mn3_4
```

2) HB simulation to extract Zin/Zout per topology

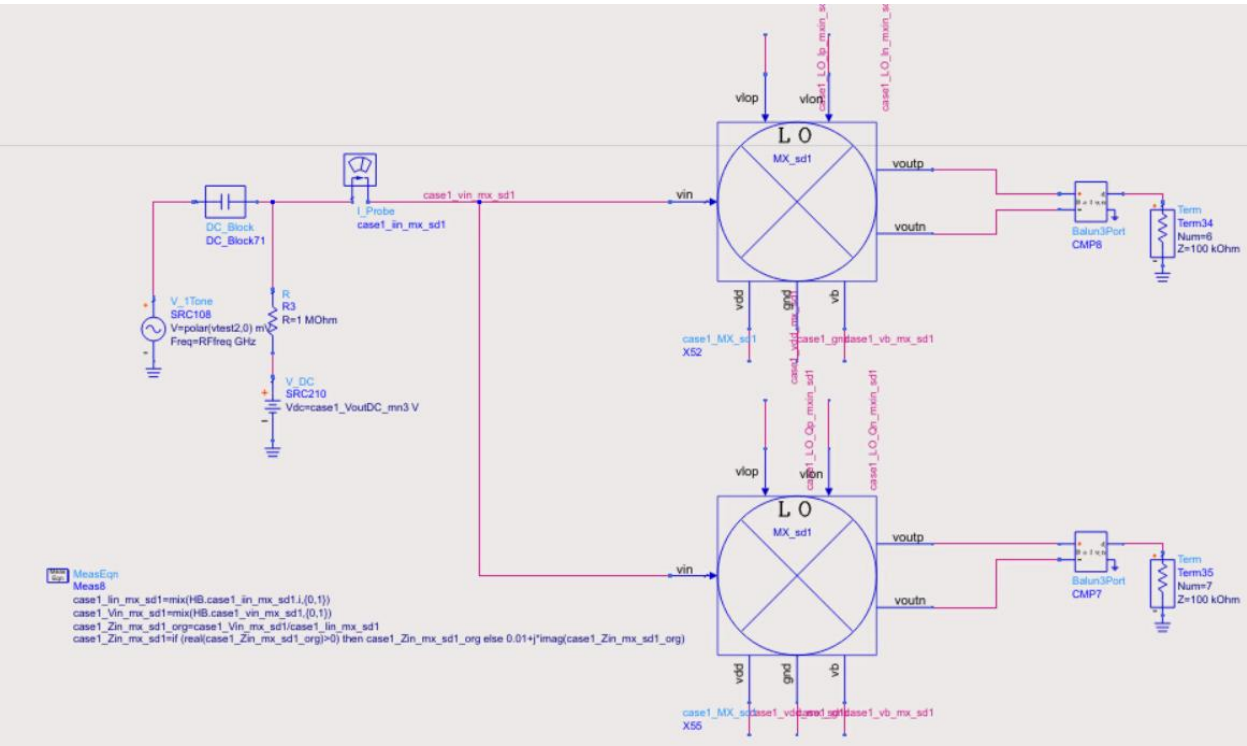
(1) HB_Z1 (Zout_mn1, Zin_mx, Zinp_mx, Zinn_mx)

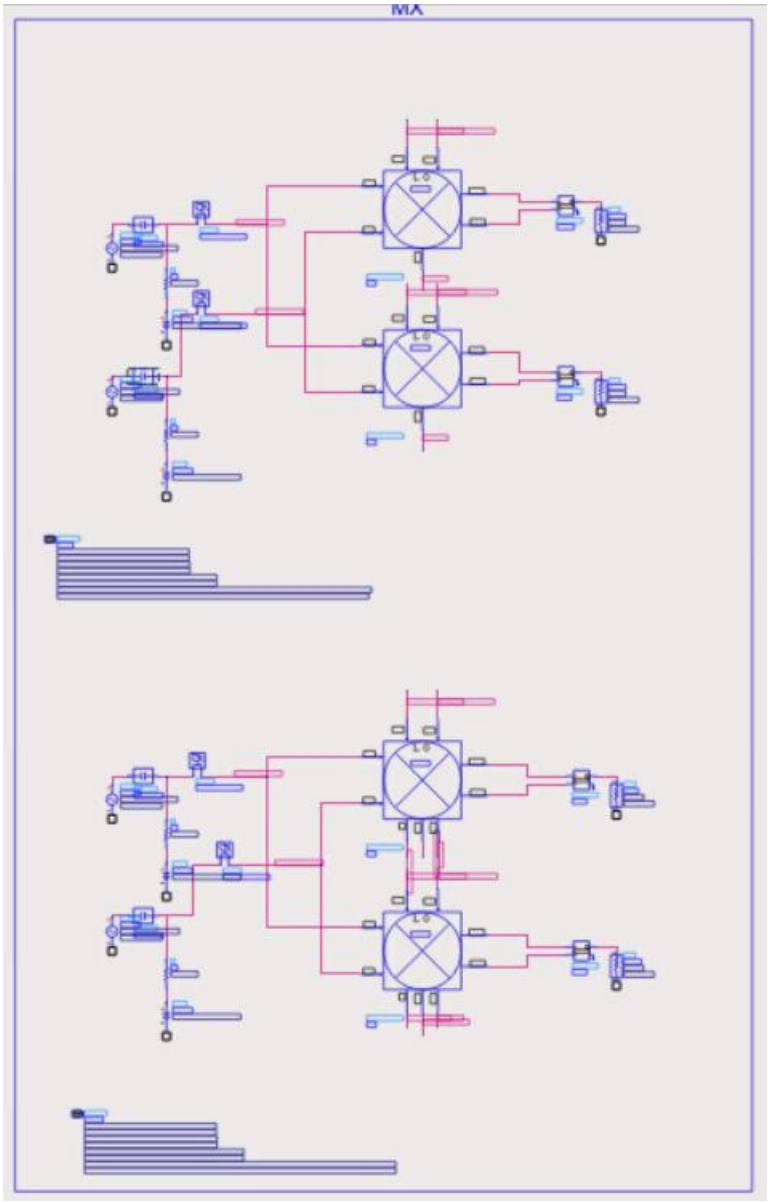
- MN1 → Zout_mn1





- MX → Zin_mx, Zinp_mx, Zinn_mx


vlop
vlon
L O
MX_sd1
voutp
voutn
vin
DC_Block
DC_Block71
I_Probe
case1_iin_mx_sd1
case1_vin_mx_sd1
V_1Tone
SRC108
V=polar(vtest2,0) mV
Freq=RFfreq GHz
R
R3
R=1 MOhm
V_DC
SRC210
Vdc=case1_VoutDC_mn3 V
vdd
gnd
vb
case1_MX_sd1
X52
Balun3Port
CMP8
Term
Term34
Num=6
Z=100 kOhm
Term35
Num=7
Z=100 kOhm
MeasEqn
Meas8
case1_Iin_mx_sd1=mix(HB.case1_iin_mx_sd1.i,{0,1})
case1_Vin_mx_sd1=mix(HB.case1_vin_mx_sd1,{0,1})
case1_Zin_mx_sd1_org=case1_Vin_mx_sd1/case1_Iin_mx_sd1
case1_Zin_mx_sd1=if (real(case1_Zin_mx_sd1_org)>0) then case1_Zin_mx_sd1_org else 0.01+j*imag(case1_Zin_mx_sd1_org)

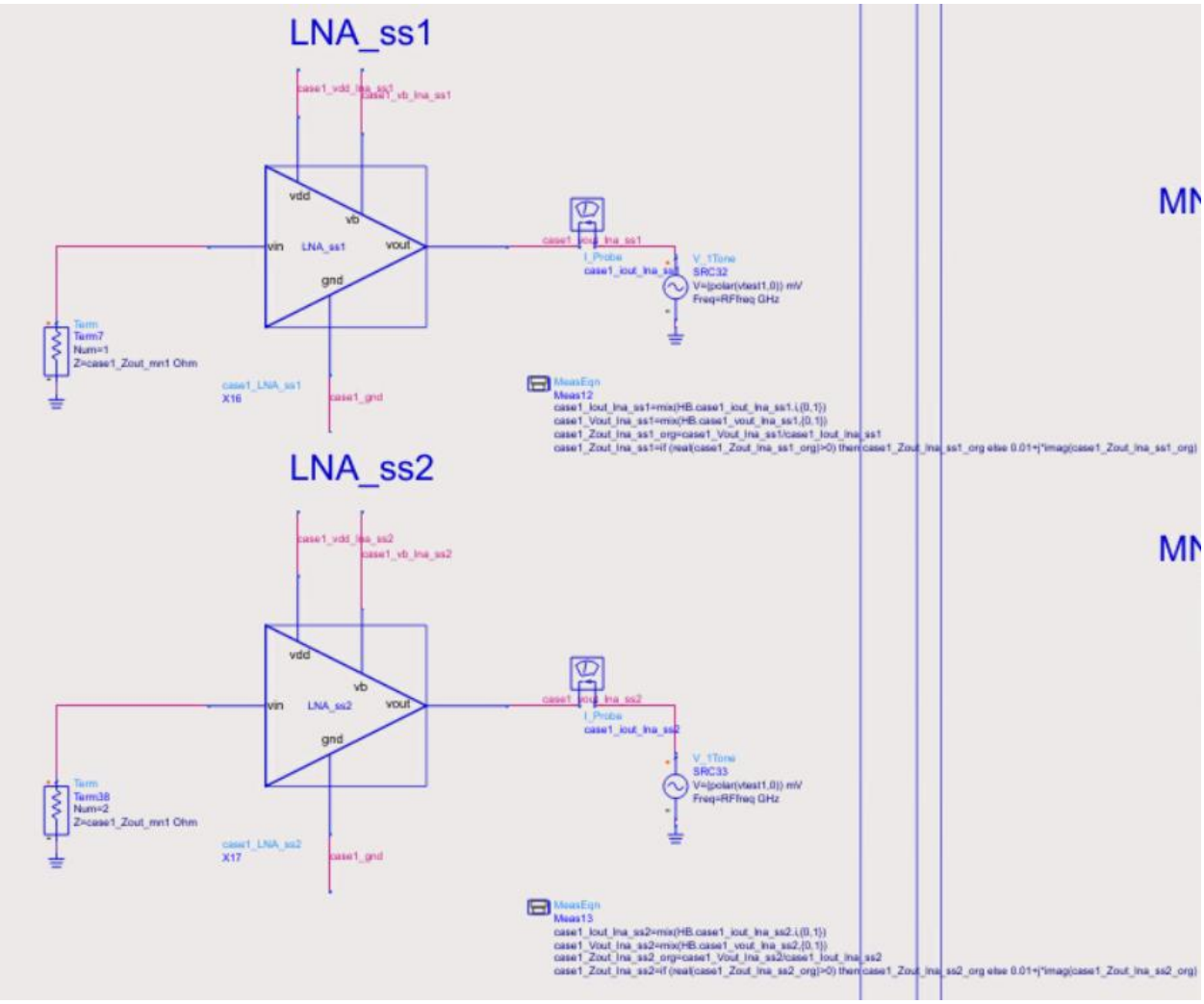


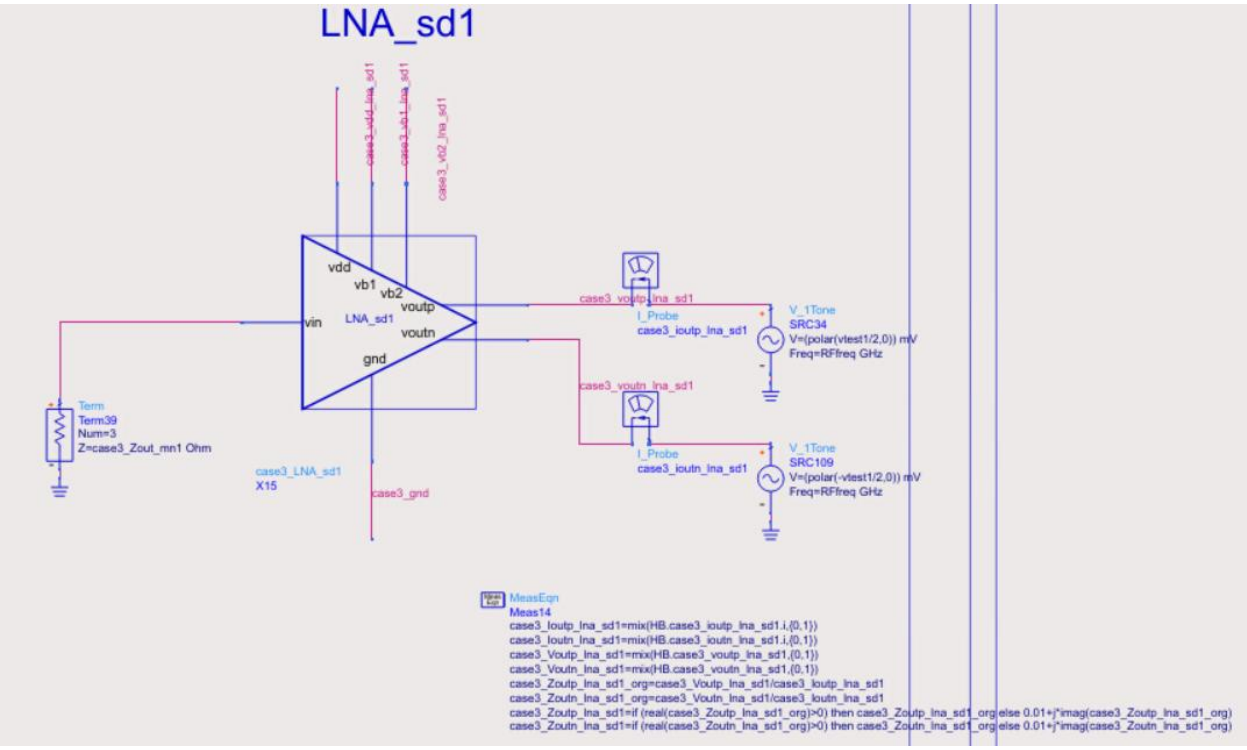

```
MeasEqn
Meas13
case1_Zin_mx=case1_mx_sd1*case1_Zin_mx_sd1
```

```
MeasEqn
Meas31
case3_Zinp_mx=case3_mx_dd1*case3_Zinp_mx_dd1+case3_mx_dd2*case3_Zinp_mx_dd2
case3_Zinn_mx=case3_mx_dd1*case3_Zinn_mx_dd1+case3_mx_dd2*case3_Zinn_mx_dd2
```

(2) HB_Z2 (Zout_lna, Zoutp_lna, Zoutn_lna, Zin_mn3, Zinp_mn3, Zinn_mn3**)**

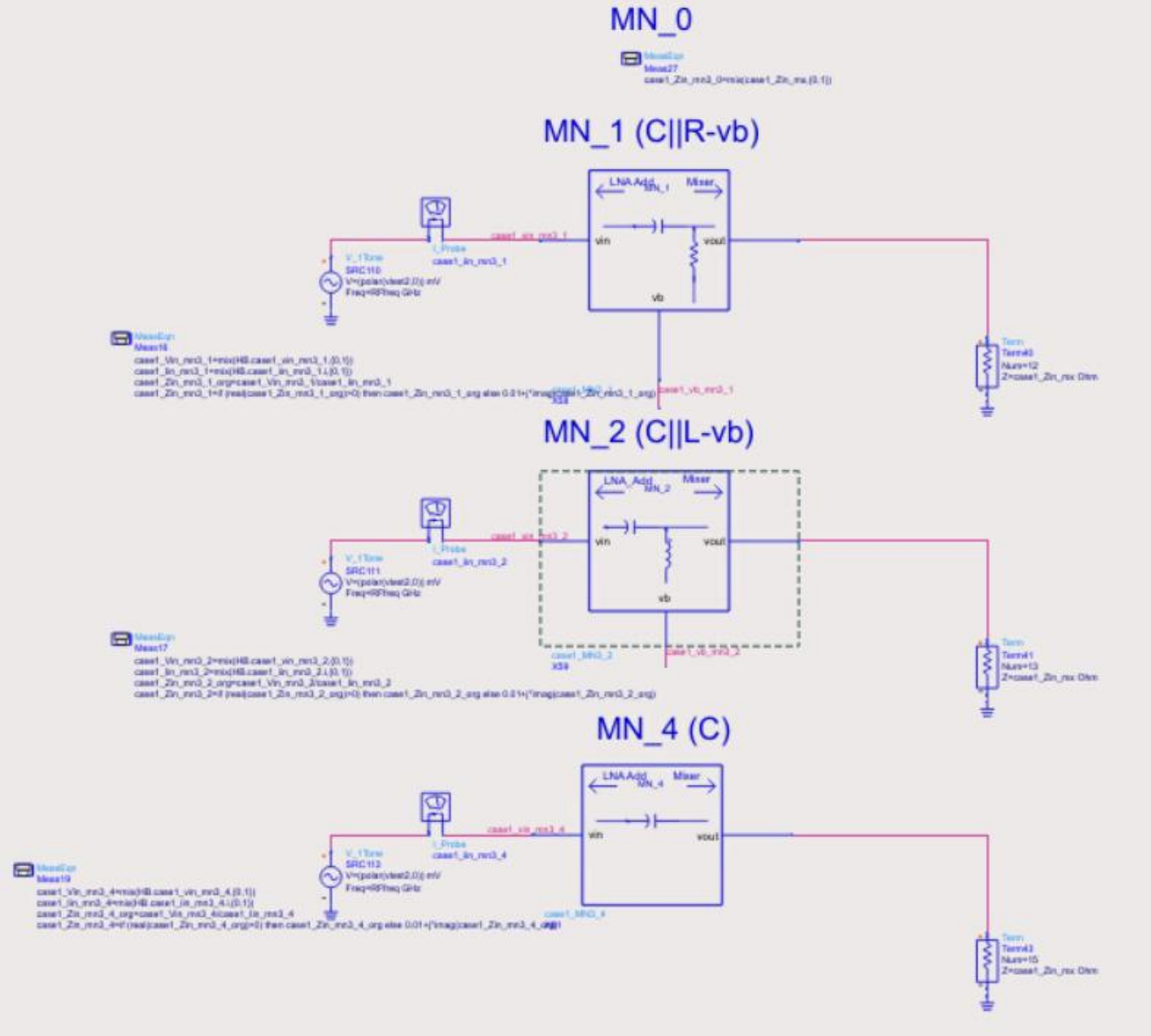
- LNA → Zout_lna, Zoutp_lna, Zoutn_lna

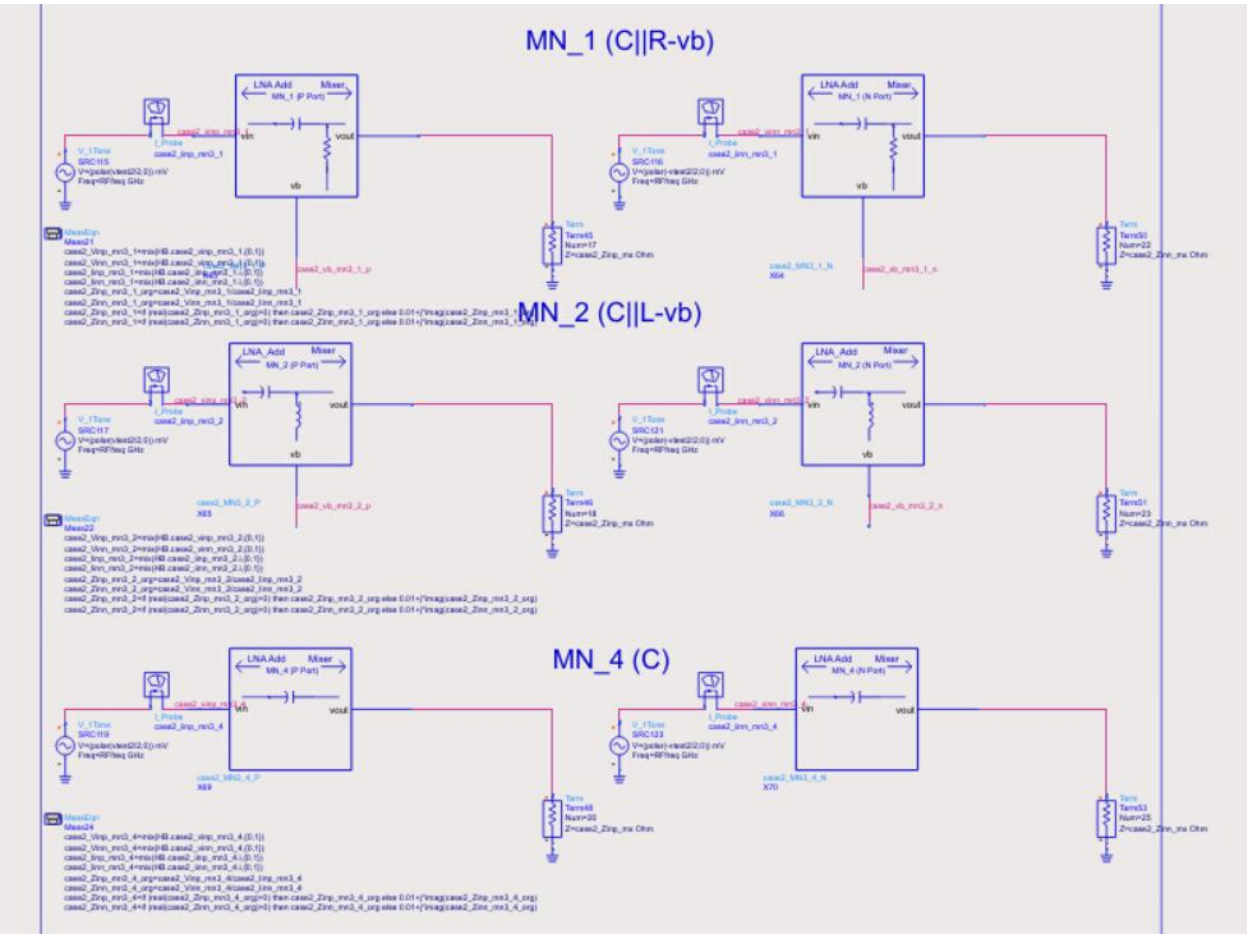




MeasEqn
Meas29
case1_Zout_lna=case1_lna_ss0*case1_Zout_lna_ss0+case1_lna_ss1*case1_Zout_lna_ss1+case1_lna_ss2*case1_Zout_lna_ss2

- MN3 → Zin_mn3, Zinp_mn3, Zinn_mn3


MN_0
MN_1 (C||R-vb)
LNA_Add
Mixer
vin
vout
vb
MN_2 (C||L-vb)
MN_4 (C)




```
MeasEqn
Meas30
case1_Zin_mn3=case1_mn3_0*case1_Zin_mn3_0+case1_mn3_1*case1_Zin_mn3_1+case1_mn3_2*case1_Zin_mn3_2+case1_mn3_4*case1_Zin_mn3_4
```

```
MeasEqn
Meas42
case2_Zinp_mn3=case2_mn3_1_p*case2_Zinp_mn3_1+case2_mn3_2_p*case2_Zinp_mn3_2+case2_mn3_4_p*case2_Zinp_mn3_4
case2_Zinn_mn3=+case2_mn3_1_n*case2_Zinn_mn3_1+case2_mn3_2_n*case2_Zinn_mn3_2+case2_mn3_4_n*case2_Zinn_mn3_4
```

(3) HB_Z3

Zout_mn2, Zoutp_mn2, Zoutn_mn2, Zin_add, Zinp_add, Zinn_add

(4) HB_Z4

Zout_add, Zoutp_add, Zoutn_add, Zin_mn2, Zinp_mn2, Zinn_mn2

(5) HB_Z5

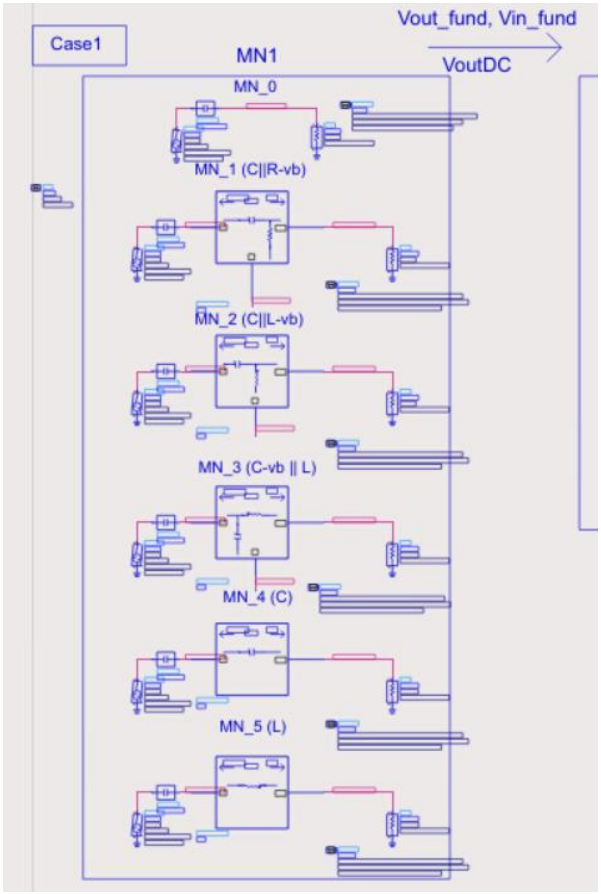
Zin_lna, Zout_mn3, Zoutp_mn3, Zoutn_mn3

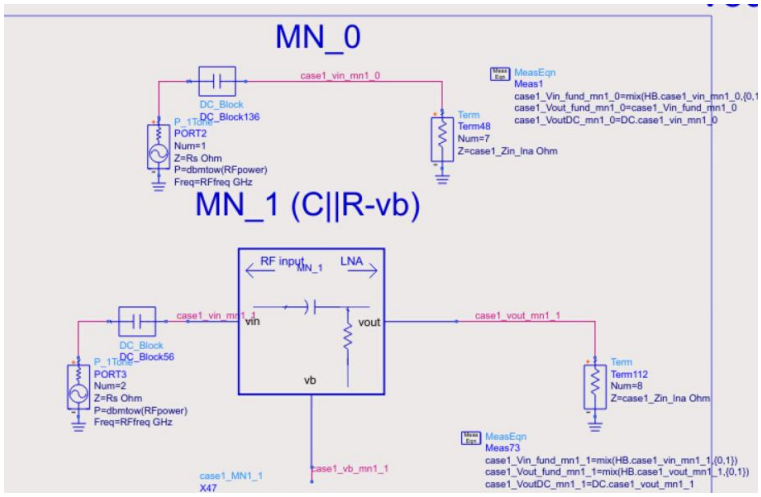
2. HB simulation to evaluate

(1) HB_MN1

Import: Zin_lna

Output (to export to the next stage): Vout_fund (Vout_mn1), Vin_fund, VoutDC (VoutDC_mn1)



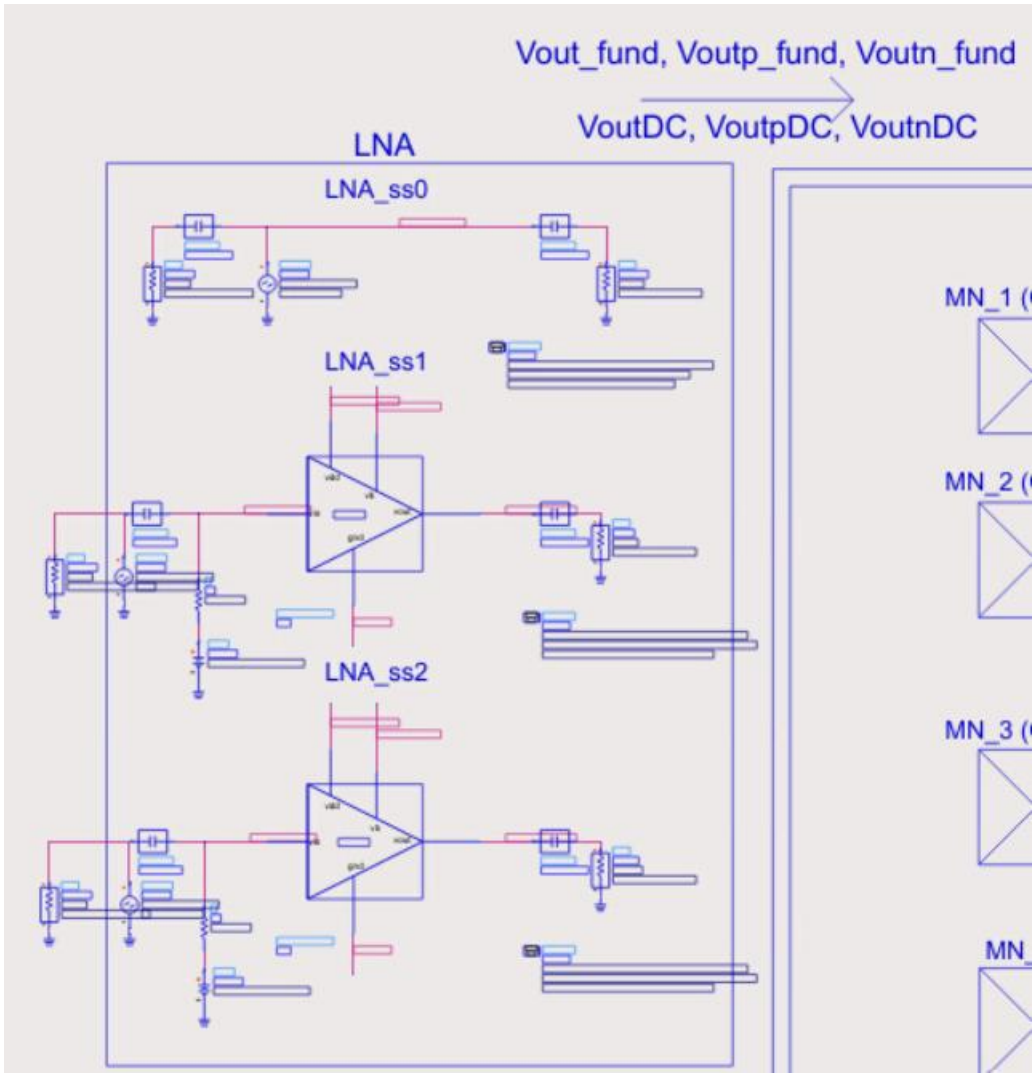


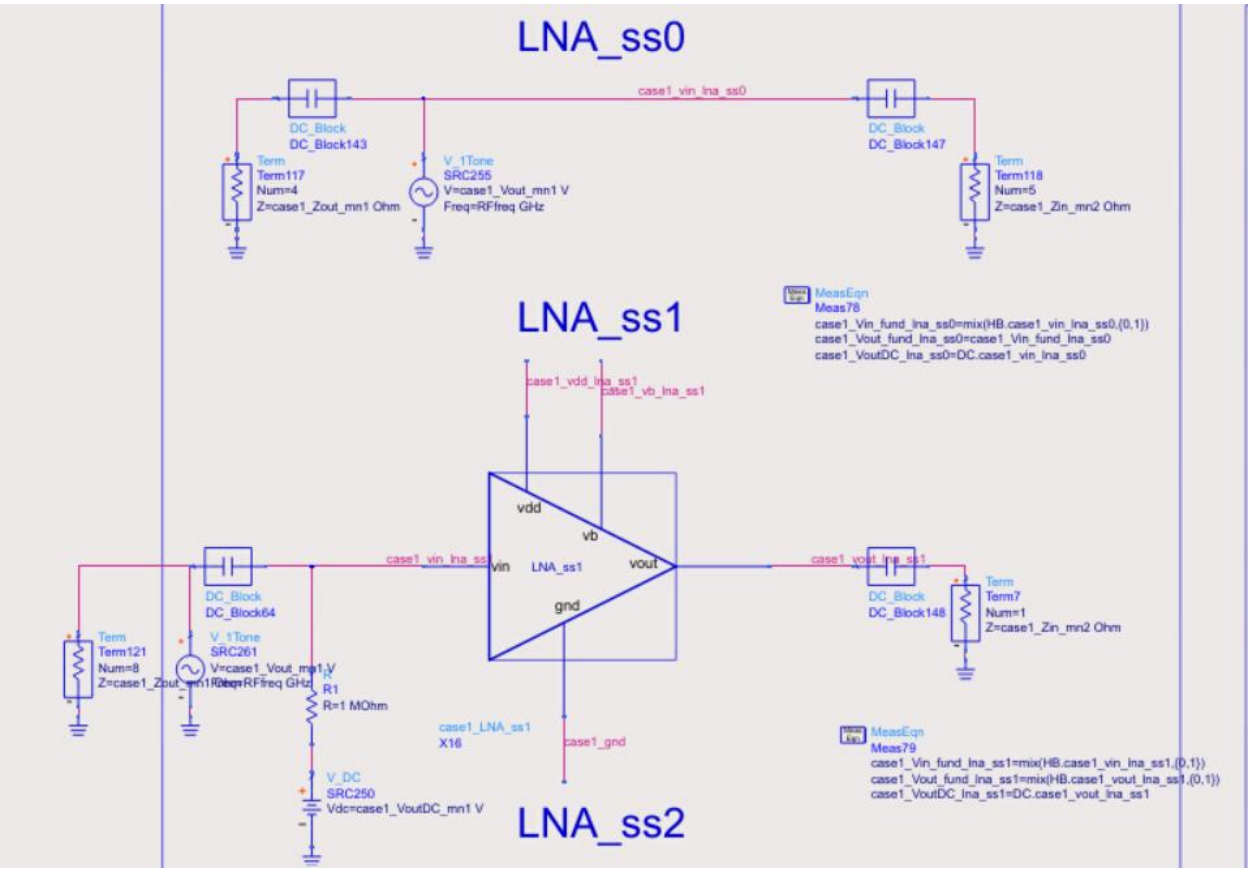
MeasEqn
Meas51
case1_Vin_fund=case1_mn1_0*case1_Vin_fund_mn1_0+case1_mn1_1*case1_Vin_fund_mn1_1+case1_mn1_2*case1_Vin_fund_mn1_2+case1_mn1_3*case1_Vin_fund_mn1_3+case1_mn1_4*case1_Vin_fund_mn1_4+case1_mn1_5*case1_Vin_fund_mn1_5
case1_Vout_fund=case1_mn1_0*case1_Vout_fund_mn1_0+case1_mn1_1*case1_Vout_fund_mn1_1+case1_mn1_2*case1_Vout_fund_mn1_2+case1_mn1_3*case1_Vout_fund_mn1_3+case1_mn1_4*case1_Vout_fund_mn1_4+case1_mn1_5*case1_Vout_fund_mn1_5
case1_VoutDC=case1_mn1_0*case1_VoutDC_mn1_0+case1_mn1_1*case1_VoutDC_mn1_1+case1_mn1_2*case1_VoutDC_mn1_2+case1_mn1_3*case1_VoutDC_mn1_3+case1_mn1_4*case1_VoutDC_mn1_4+case1_mn1_5*case1_VoutDC_mn1_5

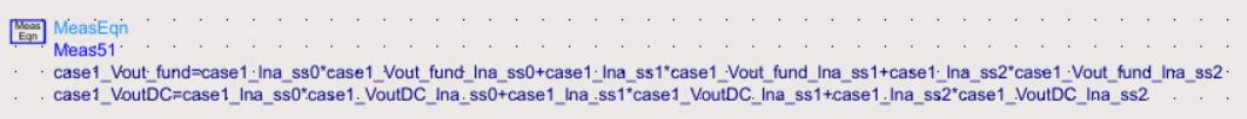
(2) HB_LNA

Import: Zout_mn1, Zin_mn2, Vout_mn1, VoutDC_mn1

Output (to export to the next stage): Vout_fund, Voutp_fund, Voutn_fund, VoutDC, VoutpDC, VoutnDC







(3) HB_MN2

Import: Zout_lna, Zin_add, Vout_lna, VoutDC_lna, Zoutp_lna, Zoutn_lna, Zinp_add, Zinn_add, Voutp_lna, Voutn_lna, VoutpDC_lna, VoutnDC_lna

Output (to export to the next stage): Vout_fund, Voutp_fund, Voutn_fund, VoutDC, Voutp_DC, Voutn_DC

(4) HB_ADD

Import: Zout_mn2, Zin_mn3, Vout_mn2, VoutDC_mn2, Zoutp_mn2, Zoutn_mn2, Zinp_mn3, Zinn_mn3, Voutp_mn2, Voutn_mn2, VoutpDC_mn2, VoutnDC_mn2

Output (to export to the next stage): Vout_fund, Voutp_fund, Voutn_fund, VoutDC, VoutpDC, VoutnDC

(5) HB_MN3

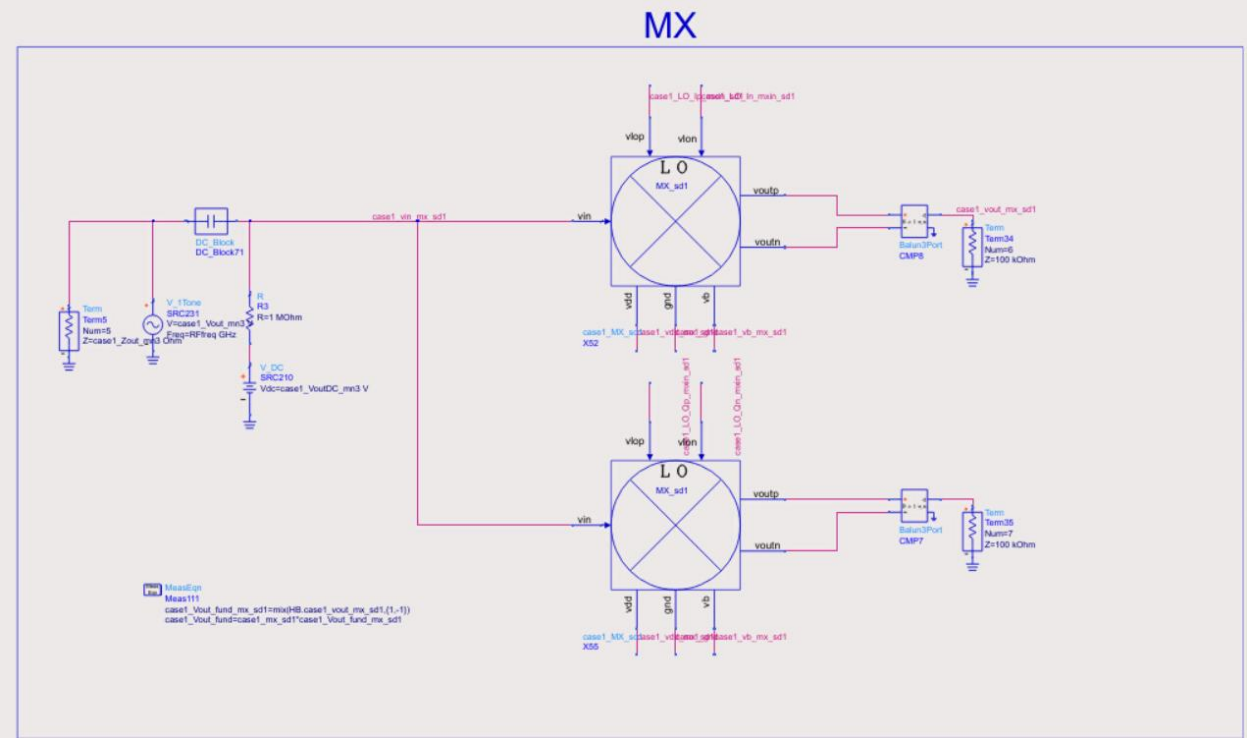
Import: Zout_add, Zin_mx, Vout_add, VoutDC_add, Zoutp_add, Zoutn_add, Zinp_mx, Zinn_mx, Voutp_add, Voutn_add, VoutpDC_add, VoutnDC_add

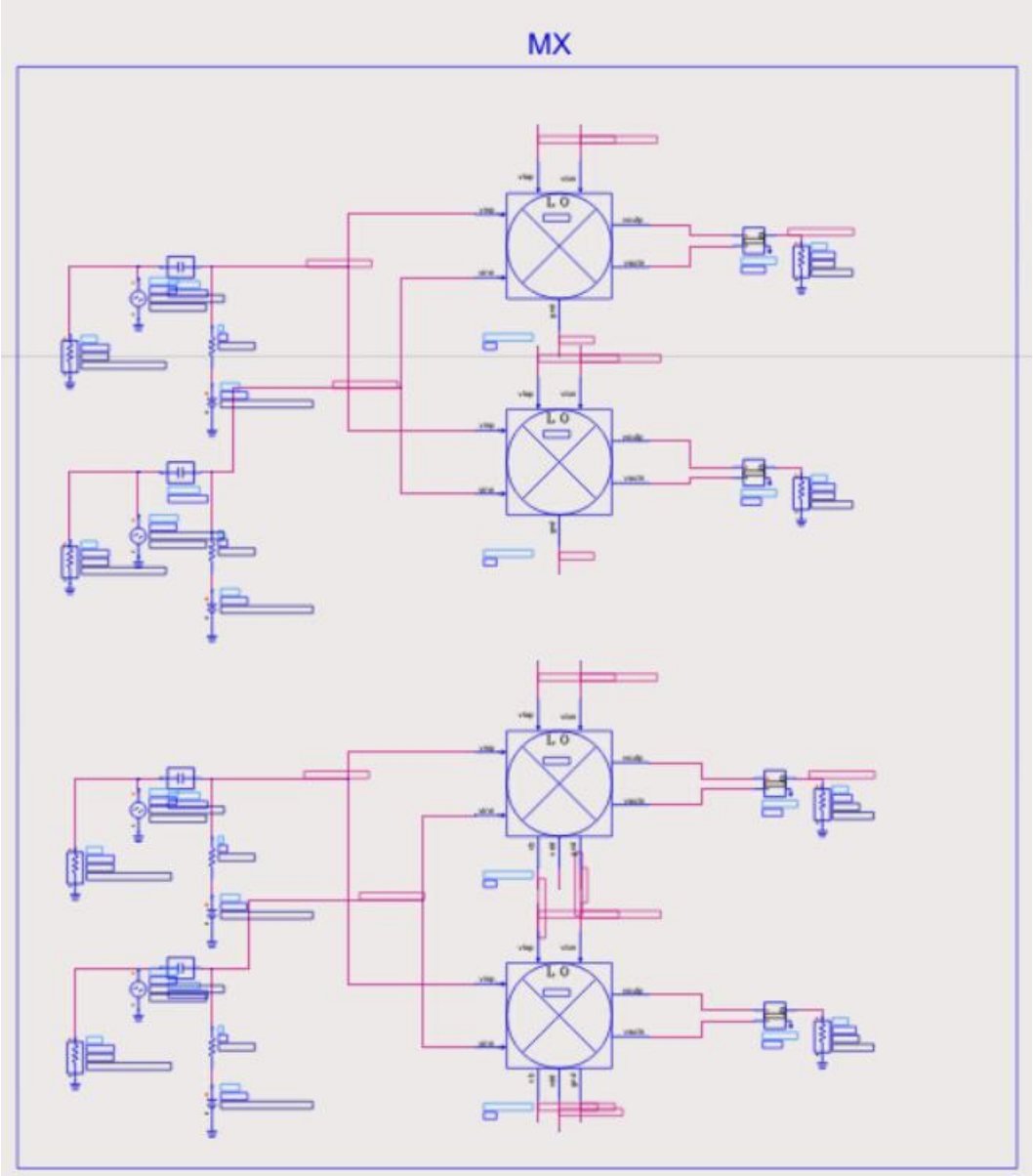
Output (to export to the next stage): Vout_fund, Voutp_fund, Voutn_fund, VoutDC, VoutpDC, VoutnDC

(6) HB_MX

Import: Vin_fund, Zout_mn3, Vout_mn3, VoutDC_mn3, Zoutp_mn3, Zoutn_mn3, Voutp_mn3, Voutn_mn3, VoutpDC_mn3, VoutnDC_mn3

Output: Vout_fund





Meas Eqn MeasEqn

```
Meas114
case2_Vout_fund_mx_dd1=mix(HB.case2_vout_mx_dd1,{1,-1})
case2_Vout_fund_mx_dd2=mix(HB.case2_vout_mx_dd2,{1,-1})
case2_Vout_fund=case2_mx_dd1*case2_Vout_fund_mx_dd1+case2_mx_dd2*case2_Vout_fund_mx_dd2
```