



# Operating systems INT2206-6 Summer 2018-2019

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Bài kiểm tra chương 5-6

**Started on** Sunday, 5 May 2019, 8:03 PM

**State** Finished

**Completed on** Sunday, 5 May 2019, 8:24 PM

**Time taken** 21 mins 22 secs

**Marks** 16.00/20.00

**Grade** 8.00 out of 10.00 (80%)

## Question 1

Incorrect

Mark 0.00 out of 1.00

Flag question

A system with 2-level page table in the form of (p1, p2, offset), and the content of page table No 2 of level 2 is: {(27, v), (213, i), (87, v), (826, v), (92, i)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10. Given a reference =8392136, calculate its physical address, e.g., 12764 or Page fault?

Answer: Page fault



## Question 2

Incorrect

Mark 0.00 out of 1.00

Flag question

Which is INCORRECT about priority (memory) allocation?

Select one:

- ☒ It can prevent thrashing from occurring
- ☐ Frames are globally allocated
- ☐ It cannot prevent thrashing from occurring
- ☐ High priority processes are allocated first

## Question 3

Correct

Mark 1.00 out of 1.00

Flag question

Suppose in a paging on demand system has the page fault rate = 0.2%; the memory access time=300 nano seconds; and the page fault handling time is 7 milli seconds. How many times the performance are slowdown? (e.g. 87)


Answer: 48



**Question 4**

Correct

Mark 1.00 out of 1.00

 Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 8 milliseconds; page-fault rate is  $3/1000$ . Which is the Effective Access Time (EAT) of the system?


Select one:

- ☐ 27.2 micro seconds
- ☐ 26.2 micro seconds
- ☐ 25.2 micro seconds
- ☒ 24.2 micro seconds ✓

**Question 5**

Correct

Mark 1.00 out of 1.00

 Flag question

Which is INCORRECT about dynamic allocation algorithms?


Select one:

- ☒ They are only used in MFT systems ✓
- ☐ They are called whenever a new process arrives
- ☐ One of the algorithms does not need to search the whole free memory list to find a suitable memory region
- ☐ Their task is to find a suitable memory region to load the process into

**Question 6**

Correct

Mark 1.00 out of 1.00

 Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 7 milliseconds; page-fault rate is  $1/1000$ . Which is the Effective Access Time (EAT) of the system?


Select one:

- ☐ 9.2 micro seconds
- ☐ 6.2 micro seconds
- ☐ 8.2 micro seconds
- ☒ 7.2 micro seconds ✓

**Question 7**

Correct

Mark 1.00 out of 1.00

 Flag question

Suppose a paging system has the page fault rate= $0.048\%$ ; the memory access time is: 320 nano seconds; and the page fault handling time is: 9 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  ✓**Question 8**

Correct

Which is INCORRECT about Multiprogramming with a Fixed number of Tasks (MFT) memory allocation algorithm?

Mark 1.00 out of

1.00

Flag question

Select one:

- ☐ Operating system manages the allocated and available partitions
- ☐ When a new process arrives, it finds a suitable partition to allocate to the process
- ☐ Memory is split into fixed partitions
- ☒ Memory is split into partitions of which the size can vary ✓

### Question 9

Correct

Mark 1.00 out of

1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	97	1
1	12	0
2	5	1
3	23	1
4	132	0

Calculate the physical address of the logical address 4278? (e.g. 18932 or error)

Answer: error



### Question 10

Incorrect

Mark 0.00 out of

1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	97	1

1	98	0
---	----	---

2	3	1
---	---	---

3	56	1
---	----	---

4	61	0
---	----	---

Calculate the physical address of the logical address 3784? (e.g. 18932 or error)

Answer: 24264



### Question 11

Correct

Mark 1.00 out of 1.00

Flag question

Given the reference string: 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1. Suppose the system uses Least Recently Used (LRU) page replacement algorithm with 3 frames. Which is the ORDER of the pages that are selected as victims to be swapped out?

Select one:

- ☐ 7 1 2 3 1 4 1 3 2
- ☐ 7 2 1 3 0 4 2 3 2
- ☐ 7 1 2 3 0 4 1 2 3
- ☒ 7 1 2 3 0 4 0 3 2 ✓

### Question 12

Correct

Mark 1.00 out of 1.00

Flag question

A system uses Translation Look-aside Buffer (TLB) for address translation in paging (1 level page table). Suppose the access time of TLB is 20ms; the access time of the memory is 250ms; and the hit rate of TLB is 95%. Which is the Effective Access Time (EAT) of the system?


Select one:

- ☐ 284.5 ms
- ☐ 281.5 ms
- ☒ 282.5 ms ✓
- ☐ 283.5 ms

**Question 13**

Correct

Mark 1.00 out of 1.00

 Flag question

Which is incorrect about 1-level paging?


Select one:

- ☐ Page-table base register (PTBR) is the register pointing to the page table of the process
- ☒ The logical address must be in the form of (page, offset) ✓
- ☐ Page-table length register (PRLR) indicates the size of the page table
- ☐ PRLR can be used to detect whether a page number is out of range

**Question 14**

Correct

Mark 1.00 out of 1.00


 Flag question

Suppose a paging system has the page fault rate=0.08%; the memory access time is: 320 nano seconds; and the page fault handling time is: 9 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  ✓**Question 15**

Incorrect

Mark 0.00 out of 1.00

 Flag question

Which is the reason why a process can run when only a part of it is loaded into memory?


Select one:

- ☐ Because instructions of a process are independent
- ☐ Because only one instruction is executed at a time
- ☐ Because related instructions are always in the same group
- ☒ Because we can indicate which instructions to run ✗

**Question 16**

Correct

Mark 1.00 out of 1.00

 Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

FRAME    VALID		
0	4	1
1	12	0
2	5	1
3	23	0

4      51      1

Calculate the physical address of the logical address 826? (e.g. 18932 or error)

Answer: 4922



### Question 17

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses segmentation memory allocation. The content of the segment table (limit, base) of a process is [(1000, 1400), (400, 6300), (400, 4300), (1100, 3200), (1000, 4700)]. Calculate the physical address of the reference (2, 402) (e.g. a number or invalid)?

Answer: invalid



### Question 18

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 9 milliseconds; page-fault rate is 1/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☐ 7.2 micro seconds
- ☐ 6.2 micro seconds
- ☒ 9.2 micro seconds ✓
- ☐ 8.2 micro seconds

### Question 19

Correct

Mark 1.00 out of 1.00

Flag question


Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 7 milliseconds; page-fault rate is 3/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☐ 23.2 micro seconds
- ☐ 24.2 micro seconds
- ☒ 21.2 micro seconds ✓
- ☐ 22.2 micro seconds

**Question 20**

Correct

Mark 1.00 out of  
1.00 Flag question

A system does NOT use Translation Look-aside Buffer (TLB) for address translation in paging (1 level page table). Suppose the access time of the memory is 200ms; Which is the Effective Access Time (EAT) of the system?

Select one:

- ☐ 160 ms
- ☒ 400 ms ✓
- ☐ 200 ms
- ☐ 180 ms

Finish review

**QUIZ NAVIGATION**

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
---	---	---	---	---	---	---	---	---	----	----	----	----	----	----	----	----	----	----	----

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Finish review

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# Operating systems INT2206-6 Summer 2018-2019

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**Started on** Sunday, 5 May 2019, 8:00 PM

**State** Finished

**Completed on** Sunday, 5 May 2019, 8:18 PM

**Time taken** 17 mins 51 secs

**Marks** 17.00/20.00

**Grade** 8.50 out of 10.00 (85%)

## Question 1

Correct

Mark 1.00 out of 1.00

Flag question

Suppose in a paging on demand system has the page fault rate = 0.2%; the memory access time=200 nano seconds; and the page fault handling time is 7 milli seconds. How many times the performance are slowdown? (e.g. 87)

Answer:  ✓

## Question 2

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses second chance page replacement algorithm with 6 frames. The values of the reference bits of the frames are 1 1 0 1 1 0. The current position of the pointer is at 2nd frame. When the page replacement is called, show the values of the reference bits (e.g. 1 1 0 1 1 0)?

Answer:  ✓

## Question 3

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging (1-level page table) with the frame size of 4KB; the page table of a process is [56, 120, 3]. Which is the physical address of the reference (1, 496)?

Select one:

- ☒ 120\*4096+496 ✓
- ☐ 560\*4096+496
- ☐ 120\*1024+496
- ☐ 3\*4096+496

## Question 4

Incorrect

Which is incorrect about hashed page table?



5/5/2019 1.00 out of 1.00

Flag question

Select one:

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- ☐ Multi processes can have references with the same page number, so the hash table must handle collisions
- ☐ A linked list is added to the hash table when there are multiple references with the same page number
- ☐ This can be used only with 1-level paging
- ☒ The page tables are stored in a hash table ✗

### Question 5

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 7 milliseconds; page-fault rate is 1/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☐ 8.2 micro seconds
- ☒ 7.2 micro seconds ✓
- ☐ 9.2 micro seconds
- ☐ 6.2 micro seconds

### Question 6

Correct

Mark 1.00 out of 1.00

Flag question

Which is INCORRECT about fragmentation?

Select one:

- ☐ There are two types: internal and external fragmentation
- ☒ There is no fragmentation on disks ✓
- ☐ It can lead to a situation where a process cannot run though the total free memory is greater than the process size
- ☐ It leads to less effective memory utilization

### Question 7

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a paging system has the page fault rate=0.048%; the memory access time is: 320 nano seconds; and the page fault handling time is: 9 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  ✓

### Question 8

Correct

Mark 1.00 out of 1.00

Flag question


Suppose a system uses proportional allocation based on the size of the processes. There are two processes A and B with the size of 10 and 127 frames, correspondingly. The memory size is 64 frames, calculate the number of frames allocated for A and B (e.g. 23:17)?

Answer:  ✓

**Question 9**

Incorrect

Mark 0.00 out of 1.00

 Flag question


A system uses working set model with  $\Delta=10$ . Given a reference string: 2 6 1 5 7 7 7 5 1 6 2 3 4 4 4 3 4 4 4 1 3 2 3 4 4 4 3 4 4 4; Show the working set at 20th reference (e.g. 2 6 1 5 7)?

Answer: 6 2 3 4

**Question 10**


Correct

Mark 1.00 out of 1.00

 Flag question

A system uses Translation Look-aside Buffer (TLB) for address translation in paging (1 level page table). Suppose the access time of TLB is 20ms; the access time of the memory is 200ms; and the hit rate of TLB is 90%. Which is the Effective Access Time (EAT) of the system?


Select one:

- ☐ 253 ms
- ☐ 260 ms
- ☐ 250 ms
- ☒ 240 ms 

**Question 11**

Correct

Mark 1.00 out of 1.00

 Flag question


Suppose a system uses segmentation memory allocation. The content of the segment table (limit, base) of a process is [(1000, 1400), (400, 6300), (400, 4300), (1100, 3200), (1000, 4700)]. Calculate the physical address of the reference (4, 106) (e.g. a number or invalid)?

Answer: 4806

**Question 12**


Correct

Mark 1.00 out of 1.00

 Flag question

Suppose a system uses Translation Look-aside Buffer (TLB) for address translation in paging (1 level page table). Which statement is INCORRECT?


Select one:

- ☐ In the worst case, we need to access both TLB and the page table during the address translation process
- ☒ In all cases, during the address translation process, we only need to access TLB 
- ☐ TLB helps to speed up the address translation process
- ☐ The size of TLB is usually small (typically from 64 to 1024 entries)

**Question 13**

Correct

Mark 1.00 out of 1.00

 Flag question

Given the reference string: 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1. Optimal (page replacement) algorithm) is used (with 3 frames), calculate the total page faults?

Answer: 9



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Bài kiểm tra chương 5-6

**Question 14**

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a segment table with the following rows of (base, limit, valid): {(1432823, 1236, v), (876530, 8364, v), (3898764, 2894, i), (14987378, 45288, v), (2876906, 9862, i)}. Given a reference (s, offset)=(0, 8976), identify its physical address?

Select one:

- ☐ 3907740
- ☒ Invalid reference ✓
- ☐ 2885882
- ☐ 885506

**Question 15**

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	97	1
1	12	0
2	5	1
3	23	1
4	132	0

Calculate the physical address of the logical address 4278? (e.g. 18932 or error)

Answer: error ✓

**Question 16**

Incorrect

Mark 0.00 out of 1.00

Flag question


Suppose a system uses FIFO page replacement algorithm with 3 frames. Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5, show the pages (in appearing order, e.g. 1, 2, 3, 4, 5) that are selected as victims to be swapped out?

Answer: 1, 2, 3, 4, 2, 1 ✗

**Question 17**

Correct

Mark 1.00 out of 1.00


 Flag question

Suppose a paging system has the page fault rate=0.3%; the memory access time is: 200 nano seconds; and the page fault handling time is: 7 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  **Question 18**

Correct

Mark 1.00 out of 1.00

 Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.


	FRAME	VALID
0	97	1
1	12	0
2	5	1
3	23	1
4	132	0

Calculate the physical address of the logical address 3782? (e.g. 18932 or error)

Answer:  **Question 19**

Correct

Mark 1.00 out of 1.00

 Flag question

Suppose a paging system has the page fault rate=0.18%; the memory access time is: 320 nano seconds; and the page fault handling time is: 9 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  **Question 20**

Correct

Mark 1.00 out of 1.00

Suppose a system uses paging (1-level page table) with the frame size of 4KB; the page table of a process is [56, 120, 3]. Which is the physical address of the reference (0, 496)?

Flag question

Select one:

- ☐  $120 \cdot 1024 + 496$
- ☐  $3 \cdot 4096 + 496$
- ☒  $56 \cdot 4096 + 496$  ✓
- ☐  $120 \cdot 4096 + 496$

Finish review

### QUIZ NAVIGATION

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

Show one page at a time

Finish review

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# Operating systems INT2206-6 Summer 2018-2019

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**Started on** Sunday, 5 May 2019, 8:01 PM

**State** Finished

**Completed on** Sunday, 5 May 2019, 8:35 PM

**Time taken** 33 mins 57 secs

**Marks** 16.00/20.00

**Grade** 8.00 out of 10.00 (80%)

## Question 1

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging with 2-level page table without Translation Look-aside Buffer (TLB). Which is INCORRECT?

Select one:

- ☐ A reference has the form of (p,d)
- ☒ The physical address of a reference is  $f1*2^m + f2*2^n + d$ , where f1 and f2 are the values from outer and inner page tables, correspondingly ✓
- ☐ The address register is split as follows: p1, p2, d, where p1 spans m bits, p2 spans n bits, d spans k bits
- ☐ It takes 3 memory accesses for a reference

## Question 2

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	4	1
1	12	0
2	5	1

3

23

1

Calculate the physical address of the logical address 826? (e.g. 18932 or error)

Answer: 4922

**Question 3**

Correct

Mark 1.00 out of 1.00

Flag question

Which is incorrect about inverted page table?

Select one:

- ☐ This page table maps frame numbers to page numbers of running processes
- ☐ Multi-level page table is not needed in this scheme
- ☒ The process identifier needs not to be included in the table ✓
- ☐ In order to look up frame number for a reference, the operating system must construct the triple (process-id, page-number, offset)

**Question 4**

Correct

Mark 1.00 out of 1.00

Flag question

Given the reference string: 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1. Suppose the system uses Least Recently Used (LRU) page replacement algorithm with 3 frames. Which is the ORDER of the pages that are selected as victims to be swapped out?

Select one:

- ☐ 7 1 2 3 1 4 1 3 2
- ☐ 7 2 1 3 0 4 2 3 2
- ☐ 7 1 2 3 0 4 1 2 3
- ☒ 7 1 2 3 0 4 0 3 2 ✓

**Question 5**

Correct

Mark 1.00 out of 1.00

Flag question

A system with 2-level page table in the form of (p1, p2, offset), and the content of page table No 0 of level 2 is: {(27, v), (213, i), (87, v), (826, v), (92, v)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10. Given a reference = 13556, its physical address is?

Select one:


- ☐ Page fault

- ☐ 873716
- ☐ 378100

**Question 6**

Incorrect

Mark 0.00 out of 1.00

 Flag question


A system uses working set model with  $\Delta=10$ . Given a reference string: 2 6 1 5 7 7 7 7 5 1 6 2 3 4 4 4 3 4 4 4 1 3 2 3 4 4 4 3 4 4 4; Show the working set at 20th reference (e.g. 2 6 1 5 7)?

Answer: 6 2 3 4 4

**Question 7**

Correct

Mark 1.00 out of 1.00

 Flag question


Suppose a paging system has the page fault rate=0.08%; the memory access time is: 320 nano seconds; and the page fault handling time is: 7 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer: 18

**Question 8**


Incorrect

Mark 0.00 out of 1.00

 Flag question

A system with 2-level page table, the frame size is 4KB; the address register is 32 bits, the row size of the page table is 4 bytes; the address register is divided into (p1, p2, offset) for fast address translation (no need to use multiplication and addition for calculating the physical address). Given a reference =4200746, the corresponding (p1, p2, offset) is?


Select one:

- ☐ (2, 3, 256)
- ☐ (1, 2, 256)
- ☒ (0, 1026, 256) 
- ☐ (1, 3, 256)

**Question 9**


Correct

Mark 1.00 out of 1.00

 Flag question

Which is INCORRECT about page fault?

Select one:

- ☐ it occurs when a reference to a page that is not in memory
- ☐ a page fault handler is called whenever it occurs
- ☐ it occurs in paging on demand
- ☒ when a page fault occurs the corresponding process will be terminated 

**Question 10**

Correct

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 8 milliseconds; page-fault rate is 1/1000. Calculate the Effective Access Time (EAT) (in micro second) of



the system (e.g. 7.8)?


Bài kiểm tra chương 5-6

Answer: 8.2

**Question 11**

Correct

Mark 1.00 out of 1.00

 Flag question


Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5. Suppose the system uses Least Recently Used (LRU) page replacement algorithm with 4 frames, calculate the total page faults?

Answer: 8

**Question 12**

Correct

Mark 1.00 out of 1.00

 Flag question

Which is INCORRECT about dynamic allocation algorithms?


Select one:

- ☐ They are called whenever a new process arrives
- ☒ They are only used in MFT systems ✓
- ☐ Their task is to find a suitable memory region to load the process into
- ☐ One of the algorithms does not need to search the whole free memory list to find a suitable memory region

**Question 13**

Correct

Mark 1.00 out of 1.00

 Flag question


Suppose a system uses contiguous memory allocation with the following information: the base address is 1640; the limit register is 2400; and a reference is 164. Calculate the physical address of the above reference?

Answer: 1804

**Question 14**

Correct

Mark 1.00 out of 1.00

 Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 7 milliseconds; page-fault rate is 1/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☐ 9.2 micro seconds
- ☐ 8.2 micro seconds
- ☒ 7.2 micro seconds ✓
- ☐ 6.2 micro seconds

**Question 15**

Correct

Mark 1.00 out of 1.00

Flag question

A system with 2-level page table in the form of (p1, p2, offset), and the content of page table No 2 of level 2 is: {(27, v), (213, i), (87, v), (826, v), (92, i)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10. Given a reference =8389986, its physical address is?

Select one:

- ☐ 3384674
- ☐ 378210
- ☐ 357730
- ☒ 111970 ✓

**Question 16**

Correct

Mark 1.00 out of 1.00

Flag question

Given the reference string: 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1. Suppose the system uses Least Recently Used (LRU) page replacement algorithm with 3 frames. Calculate the total page faults?

Answer: 12 ✓

**Question 17**

Incorrect

Mark 0.00 out of 1.00

Flag question

Suppose a paging system has the page fault rate=0.3%; the memory access time is: 200 nano seconds; and the page fault handling time is: 7 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer: 105 ✗

**Question 18**

Incorrect

Mark 0.00 out of 1.00

Flag question

Suppose a paging system has the page fault rate=0.18%; the memory access time is: 320 nano seconds; and the page fault handling time is: 9 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer: 21 ✗

**Question 19**

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

FRAME      VALID		
0	4	1
1	12	0

2      5      1

3      23      0

4      51      1

Calculate the physical address of the logical address 3874? (e.g. 18932 or error)

Answer: error



### Question 20

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging (1-level page table) with the frame size of 4KB; the page table of a process is [56, 120, 3]. Which is the physical address of the reference (1, 196)?

Select one:

- ☒  $120 \times 4096 + 196$  ✓
- ☐  $560 \times 4096 + 196$
- ☐  $3 \times 4096 + 196$
- ☐  $120 \times 1024 + 196$

Finish review

### QUIZ NAVIGATION

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

Show one page at a time

Finish review



# Operating systems INT2206-6 Summer 2018-2019

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**Started on** Sunday, 5 May 2019, 8:01 PM

**State** Finished

**Completed on** Sunday, 5 May 2019, 8:36 PM

**Time taken** 34 mins 47 secs

**Marks** 19.00/20.00

**Grade** 9.50 out of 10.00 (95%)

## Question 1

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses segmentation memory allocation. The content of the segment table (limit, base) of a process is [(1000, 1400), (400, 6300), (400, 4300), (1100, 3200), (1000, 4700)]. Which is the physical address of the reference (3, 208)?

Select one:

- ☐ 3208
- ☒ 3408 ✓
- ☐ 2008
- ☐ 4408

## Question 2

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

FRAME      VALID		
0	75	1
1	12	0
2	5	1

3          23          1

4          132          0

Calculate the physical address of the logical address 264? (e.g. 18932 or error)

Answer: 77064

### Question 3

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses Translation Look-aside Buffer (TLB) for address translation in paging (1 level page table). Which statement is INCORRECT?

Select one:

- ☐ In the worst case, we need to access both TLB and the page table during the address translation process
- ☒ In all cases, during the address translation process, we only need to access TLB ✓
- ☐ The size of TLB is usually small (typically from 64 to 1024 entries)
- ☐ TLB helps to speed up the address translation process

### Question 4

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 8 milliseconds; page-fault rate is 3/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☐ 27.2 micro seconds
- ☐ 26.2 micro seconds
- ☐ 25.2 micro seconds
- ☒ 24.2 micro seconds ✓

### Question 5

Incorrect

Mark 0.00 out of 1.00

Flag question

Which is the reason why a process can run when only a part of it is loaded into memory?

Select one:

- ☐ Because only one instruction is executed at a time
- ☐ Because we can indicate which instructions to run
- ☒ Because instructions of a process are independent ✗

- ☐ Because related instructions are always in the same group

### Question 6

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging (1-level page table) with the frame size of 4KB; the page table of a process is [56, 120, 3]. Which is the physical address of the reference (2, 496)?

Select one:

- ☒  $3 \times 4096 + 496$  ✓
- ☐  $120 \times 4096 + 496$
- ☐  $120 \times 1024 + 496$
- ☐  $56 \times 4096 + 496$

### Question 7

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 7 milliseconds; page-fault rate is 1/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☐ 6.2 micro seconds
- ☐ 8.2 micro seconds
- ☒ 7.2 micro seconds ✓
- ☐ 9.2 micro seconds

### Question 8

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging (1 level page table), and the access time of memory is 250 ms. Calculate the time to access the memory from a reference (p,d)?

Answer:  ✓

### Question 9

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a paging system has the page fault rate=0.18%; the memory access time is: 320 nano seconds; and the page fault handling time is: 9 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  ✓

### Question 10

Correct

Mark 1.00 out of 1.00

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 8 milliseconds; page-fault rate is 1/1000. Which is the Effective Access Time (EAT) (in micro second) of the system?

Flag question

Select one:

- ☐ 8.4 micro seconds
- ☒ 8.2 micro seconds ✓
- ☐ 8.5 micro seconds
- ☐ 8.3 micro seconds

### Question 11

Correct

Mark 1.00 out of 1.00

Flag question

Which is CORRECT about the task Memory Map Unit (MMU)?

Select one:

- ☐ MMU loads a program into memory
- ☐ MM allocates memory for processes
- ☒ MMU maps a logic address into a physical address ✓
- ☐ MMU maps a physical address into a logic address

### Question 12

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system with 2-level page table; the address register is 52 bits; the frame size is 4KB; the row size of page table is 4 bytes; Which is the correct register division (in number of bits) for fast address translation in the form of (p1, p2, offset)?

Select one:

- ☐ (29, 11, 12)
- ☐ (30, 11, 11)
- ☐ (28, 12, 12)
- ☒ (30, 10, 12) ✓

### Question 13

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a paging system has the page fault rate=0.18%; the memory access time is: 320 nano seconds; and the page fault handling time is: 6 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  ✓

### Question 14

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

FRAME    VALID		
0	4	1

1	12	0
---	----	---

2	5	1
---	---	---

3	23	0
---	----	---

4	51	1
---	----	---

Calculate the physical address of the logical address 1058? (e.g. 18932 or error)

Answer: error



### Question 15

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 8 milliseconds; page-fault rate is 1/1000. Which is the Effective Access Time (EAT) (in micro second) of the system?

Select one:

- ☒ 8.2 micro seconds ✓
- ☐ 8.3 micro seconds
- ☐ 8.5 micro seconds
- ☐ 8.4 micro seconds

### Question 16

Correct

Mark 1.00 out of 1.00

Flag question

Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5. Suppose a system uses FIFO page replacement algorithm with 3 frames. Calculate the total page faults?

Answer: 9



### Question 17

Correct

Mark 1.00 out of 1.00

Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5. Suppose the Optimal (page replacement) algorithm is used (with 4 frames), calculate the total page faults?



Flag question

Answer:

6



### Question 18

Correct

Mark 1.00 out of 1.00

Flag question

Suppose in a paging on demand system has the page fault rate = 0.2%; the memory access time=200 nano seconds; and the page fault handling time is 7 milli seconds. How many times the performance are slowdown? (e.g. 87)

Answer:

71



### Question 19

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	1291	1
1	12	0
2	5	1
3	23	1
4	132	0

Calculate the physical address of the logical address 986? (e.g. 18932 or error)

Answer:

1322970



### Question 20

Correct

Mark 1.00 out of 1.00

Which is correct about inverted page table?

Select one:

- ☐ This does not reduce the memory space for storing page tables

Flag question

- ☒ This page table maps frame numbers to page numbers of running processes ✓
- ☐ This scheme can't detect page fault
- ☐ This scheme can have multiple level versions

Finish review

### QUIZ NAVIGATION

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

Show one page at a time

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---

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# Operating systems INT2206-6 Summer 2018-2019

Home ► My courses ► Operating Systems ► INT2206-6 Summer 2018-2019 ► 2 May - 8 May ► Bài kiểm tra chương 5-6

**Started on** Sunday, 5 May 2019, 8:00 PM

**State** Finished

**Completed on** Sunday, 5 May 2019, 8:33 PM

**Time taken** 33 mins 25 secs

**Marks** 19.00/20.00

**Grade** 9.50 out of 10.00 (95%)

## Question 1

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 8 milliseconds; page-fault rate is 1/1000. Which is the Effective Access Time (EAT) (in micro second) of the system?

Select one:

- ☐ 8.3 micro seconds
- ☒ 8.2 micro seconds ✓
- ☐ 8.5 micro seconds
- ☐ 8.4 micro seconds

## Question 2

Correct

Mark 1.00 out of 1.00

Flag question

Which is correct about inverted page table?

Select one:

- ☐ This scheme can't detect page fault
- ☐ This scheme can have multiple level versions
- ☒ This page table maps frame numbers to page numbers of running processes ✓
- ☐ This does not reduce the memory space for storing page tables

## Question 3

Correct

Mark 1.00 out of 1.00

Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5. Suppose the system uses Least Recently Used (LRU) page replacement algorithm with 4 frames, calculate the total page faults?

Flag question

Answer:

8



#### Question 4

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses contiguous memory allocation with the following information: the base address is 1980; the limit register is 1400; and a reference is 1344. Calculate the physical address of the above reference?

Answer:

3324



#### Question 5

Correct

Mark 1.00 out of 1.00

Flag question

Which is incorrect about inverted page table?

Select one:

- ☐ This page table maps frame numbers to page numbers of running processes
- ☐ The number of entries in this page table equals the number of frames
- ☐ The process identifier must be also included in the table
- ☒ We can not detect page fault in this scheme ✓

#### Question 6

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	4	1
1	12	0
2	5	1
3	23	0
4	51	1

Calculate the physical address of the logical address 1058? (e.g. 18932 or error)

Answer: error



### Question 7

Incorrect

Mark 0.00 out of 1.00

Flag question

A system uses working set model with  $\Delta=10$ . Given a reference string: 2 6 1 5 7 7 7 5 1 6 2 3 4 4 4 3 4 4 4 1 3 2 3 4 4 4 3 4 4 4; Show the working set at 20th reference (e.g. 2 6 1 5 7)?

Answer: 2 6 1 5 7 3 4



### Question 8

Correct

Mark 1.00 out of 1.00

Flag question

Which is INCOREECT about memory protection in paging?

Select one:

- ☐ This ensures a process always accesses to locations within its memory space
- ☐ This ensures the page corresponding to a reference is loaded into the memory before accessing
- ☒ This ensures a reference always points to a location in memory ✓
- ☐ This ensures a process never refers to an invalid memory location

### Question 9

Correct

Mark 1.00 out of 1.00

Flag question

Which is incorrect about segmentation?

Select one:

- ☐ The logical address is in the form of (segment, offset)
- ☒ The segment number  $s$  is legal if  $s \leq \text{STLR}$  ✓
- ☐ Segment-table base register (STBR) is the pointer to the segment table's location in memory
- ☐ STLR stores the number of segments in the segment table

### Question 10

Correct

Mark 1.00 out of 1.00

Flag question

Given the reference string: 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1. Suppose the system uses FIFO page replacement with 3 frames, calculate the total page faults?

Answer: 15



### Question 11

Correct

A system with 2-level page table in the form of (p1, p2, offset), and the content of page table No 1 of level 2 is: {(612, v), (14, i), (123, v), (5, v), (756, i)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10.

Mark 1.00 out of 1.00

Flag question

Given a reference =4196656, calculate its physical address, e.g., 12764?

Answer:  ✓

### Question 12

Correct

Mark 1.00 out of 1.00

Flag question

Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5. Suppose a system uses FIFO page replacement algorithm with 3 frames. Calculate the total page faults?

Answer:  ✓

### Question 13

Correct

Mark 1.00 out of 1.00

Flag question

Which is INCORRECT about page fault?

Select one:

- ☐ it occurs when a reference to a page that is not in memory
- ☐ it occurs in paging on demand
- ☒ when a page fault occurs the corresponding process will be terminated ✓
- ☐ a page fault handler is called whenever it occurs

### Question 14

Correct

Mark 1.00 out of 1.00

Flag question

Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5. Suppose the Optimal (page replacement) algorithm) is used (with 4 frames), calculate the total page faults?

Answer:  ✓

### Question 15

Correct

Mark 1.00 out of 1.00

Flag question

Which is correct about MFT?

Select one:

- ☒ This is a memory allocation method ✓
- ☐ This a process scheduling algorithm
- ☐ This the name of page replacement algorithm

### Question 16

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

FRAME    VALID		
0	1291	1

1	12	0
---	----	---

2	5	1
---	---	---

3	23	1
---	----	---

4	132	0
---	-----	---

Calculate the physical address of the logical address 1982? (e.g. 18932 or error)

Answer: error



### Question 17

Correct

Mark 1.00 out of 1.00

Flag question

Given the reference string: 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1. Suppose the system uses FIFO page replacement with 3 frames. Show the order of pages that are selected as victims to be swapped out (e.g. 7 0 1 2 0 3 0)?

Answer: 7 0 1 2 3 0 4 2 3 0 1 2



### Question 18

Correct

Mark 1.00 out of 1.00

Flag question

Which is incorrect about inverted page table?

Select one:

- ☐ The number of entries in this page table equals the number of frames
- ☐ We can detect the page fault if the lookup in the table is not found
- ☐ This page table maps frame numbers to page numbers of running processes
- ☒ The process identifier needs not to be included in the table ✓

### Question 19

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 8 milliseconds; page-fault rate is 3/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☐ 27.2 micro seconds

- ☐ 26.2 micro seconds
- ☒ 24.2 micro seconds ✓
- ☐ 25.2 micro seconds

### Question 20

Correct

Mark 1.00 out of  
1.00

Flag question

Suppose a paging system has the page fault rate=0.3%; the memory access time is: 250 nano seconds; and the page fault handling time is: 7 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  ✓

Finish review

### QUIZ NAVIGATION

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# Operating systems INT2206-6 Summer 2018-2019

Home ► My courses ► Operating Systems ► INT2206-6 Summer 2018-2019 ► 2 May - 8 May ► Bài kiểm tra chương 5-6

Started on	Sunday, 5 May 2019, 8:00 PM
State	Finished
Completed on	Sunday, 5 May 2019, 8:35 PM
Time taken	35 mins
Marks	16.00/20.00
Grade	8.00 out of 10.00 (80%)

Question 1

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging (1-level page table) with the frame size of 4KB; the page table of a process is [56, 120, 3]. Which is the physical address of the reference (1, 196)?

- Select one:
- ☐ 120\*1024+196
  - ☐ 3\*4096+196
  - ☐ 560\*4096+196
  - ☒ 120\*4096+196 ✓

Question 2

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	4	1
1	12	0
2	5	1
3	23	1

4

132

0

Calculate the physical address of the logical address 264? (e.g. 18932 or error)

Answer: 4360



### Question 3

Correct

Mark 1.00 out of 1.00

Flag question

A system with 2-level page table in the form of (p1, p2, offset), and the content of page table No 1 of level 2 is: {(612, v),(14, i),(123, v),(5, v),(756, i)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10. Given a reference =4233524, its physical address is?

Select one:

- ☒ 534836 ✓
- ☐ 51508
- ☐ 2537780
- ☐ 3127604

### Question 4

Correct

Mark 1.00 out of 1.00

Flag question

A system with 2-level page table in the form of (p1, p2, offset), and the content of page table No 1 of level 2 is: {(27, v),(213, i),(87, v),(826, v),(92, i)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10. Given a reference =4196872, calculate its physical address, e.g., 12764 or Page fault?

Answer: 113160



### Question 5

Correct

Mark 1.00 out of 1.00

Flag question

Suppose in a paging on demand system has the page fault rate = 0.2%; the memory access time=200 nano seconds; and the page fault handling time is 7 milli seconds. How many times the performance are slowdown? (e.g. 87)

Answer: 71



### Question 6

Incorrect

Mark 0.00 out of 1.00

Flag question

Suppose a paging system has the page fault rate=0.18%; the memory access time is: 320 nano seconds; and the page fault handling time is: 9 milli seconds. How many times the performance is slowdown? (eg. 87).


Answer: 51



**Question 7**

Not answered

Marked out of 1.00

 Flag question


A system with 2-level page table in the form of (p1, p2, offset), and the content of page table No 1 of level 2 is: {(27, v),(213, i),(87, v),(826, v),(92, i)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10. Given a reference =4200968, calculate its physical address, e.g., 12764 or Page fault?

Answer:

**Question 8**

Correct

Mark 1.00 out of 1.00

 Flag question


Suppose a paging system has the page fault rate=0.08%; the memory access time is: 320 nano seconds; and the page fault handling time is: 7 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer: 18

**Question 9**


Correct

Mark 1.00 out of 1.00

 Flag question

Suppose a system uses paging (1-level page table) with the frame size of 4KB; the page table of a process is [56, 120, 3]. Which is the physical address of the reference (1, 496)?


Select one:

- ☐ 3\*4096+496
- ☐ 120\*1024+496
- ☐ 56\*4096+496
- ☒ 120\*4096+496 

**Question 10**


Correct

Mark 1.00 out of 1.00

 Flag question

A system with 2-level page table in the form of (p1, p2, offset), and the content of page table No 2 of level 2 is: {(612, v),(14, i),(123, v),(5, v),(756, i)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10. Given a reference =8395272, its physical address is?

Select one:

- ☐ 3101144
- ☒ Page fault 
- ☐ 61912
- ☐ 508376

**Question 11**

Correct

Mark 1.00 out of 1.00

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 9 milliseconds; page-fault rate is 3/1000. Which is the Effective Access Time (EAT) of the system?

Flag question

Select one:

- ☐ 28.2 micro seconds
- ☒ 27.2 micro seconds ✓
- ☐ 29.2 micro seconds
- ☐ 26.2 micro seconds

### Question 12

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a paging system has the page fault rate=0.08%; the memory access time is: 250 nano seconds; and the page fault handling time is: 7 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  ✓

### Question 13

Correct

Mark 1.00 out of 1.00

Flag question

Given the reference string: 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1. Optimal (page replacement algorithm) is used (with 3 frames), calculate the total page faults?

Answer:  ✓

### Question 14

Incorrect

Mark 0.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 6 milliseconds; page-fault rate is 3/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☒ 19.2 micro seconds ✗
- ☐ 17.2 micro seconds
- ☐ 20.2 micro seconds
- ☐ 18.2 micro seconds

### Question 15

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a paging system has the page fault rate=0.18%; the memory access time is: 320 nano seconds; and the page fault handling time is: 7 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  ✓

### Question 16

Correct

Given the 1-level page table of a process as bellow, with the frame size=1KB.

FRAME	VALID
-------	-------

Mark 1.00 out of 1.00

Flag question

0 4 1

1 12 0

2 5 1

3 23 0

4 51 1

Calculate the physical address of the logical address 3874? (e.g. 18932 or error)

Answer: error



### Question 17

Correct

Mark 1.00 out of 1.00

Flag question

Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5. Suppose the system uses Least Recently Used (LRU) page replacement algorithm with 4 frames, calculate the total page faults?

Answer: 8



### Question 18

Incorrect

Mark 0.00 out of 1.00

Flag question

Suppose a system uses FIFO page replacement algorithm with 3 frames. Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5, show the pages (in appearing order, e.g. 1, 2, 3, 4, 5 ...) causing a page fault.

Answer: 1, 2, 3, 4, 5, 1, 2, 3, 4, 5



### Question 19

Correct

Mark 1.00 out of 1.00

Flag question

Which is incorrect about 1-level paging?

Select one:

- ☐ Page-table length register (PRLR) indicates the size of the page table
- ☐ Page-table base register (PTBR) is the register pointing to the page table of the process

- ☐ PRLR can be used to detect whether a page number is out of range
- ☒ The logical address must be in the form of (page, offset) ✓

### Question 20

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses Translation Look-aside Buffer (TLB) for address translation in paging (1 level page table). Which statement is INCORRECT?

Select one:

- ☐ TLB helps to speed up the address translation process
- ☐ In the worst case, we need to access both TLB and the page table during the address translation process
- ☐ The size of TLB is usually small (typically from 64 to 1024 entries)
- ☒ In all cases, during the address translation process, we only need to access TLB ✓

Finish review

### QUIZ NAVIGATION

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

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**Started on** Sunday, 5 May 2019, 8:00 PM

**State** Finished

**Completed on** Sunday, 5 May 2019, 8:35 PM

**Time taken** 35 mins 1 sec

**Marks** 13.00/20.00

**Grade** 6.50 out of 10.00 (65%)

## Question 1

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	4	1
1	12	0
2	5	1
3	23	0
4	51	1

Calculate the physical address of the logical address 4982? (e.g. 18932 or error)


Answer: 53110



**Question 2**

Correct

Mark 1.00 out of 1.00

 Flag question

Which is incorrect about hashed page table?


Select one:

- ☐ The page tables are stored in a hash table
- ☐ A linked list is added to the hash table when there are multiple references with the same page number
- ☒ Each process has a distinct page table ✓
- ☐ Multi processes can have references with the same page number, so the hash table must handle collisions

**Question 3**

Correct

Mark 1.00 out of 1.00

 Flag question


Suppose a system uses segmentation memory allocation. The content of the segment table (limit, base) of a process is [(1000, 1400), (400, 6300), (400, 4300), (1100, 3200), (1000, 4700)]. Calculate the physical address of the reference (4, 106) (e.g. a number or invalid)?

Answer:  ✓

**Question 4**

Incorrect

Mark 0.00 out of 1.00

 Flag question

Which is the reason why a process can run when only a part of it is loaded into memory?


Select one:

- ☐ Because instructions of a process are independent
- ☐ Because related instructions are always in the same group
- ☒ Because we can indicate which instructions to run ✗
- ☐ Because only one instruction is executed at a time

**Question 5**

Incorrect

Mark 0.00 out of 1.00

 Flag question

A system with 2-level page table in the form of (p1, p2, offset), and the content of page table No 1 of level 2 is: {(612, v), (14, i), (123, v), (5, v), (756, i)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10. Given a reference =4233524, its physical address is?

Select one:


- ☐ 534836
- ☐ 51508
- ☒ 3127604 ✗
- ☐ 2537780



**Question 6**

Correct

Mark 1.00 out of 1.00


 Flag question

Given the reference string: 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1. Suppose the system uses Least Recently Used (LRU) page replacement algorithm with 3 frames. Calculate the total page faults?

Answer:  **Question 7**

Correct

Mark 1.00 out of 1.00


 Flag question

Given the reference string: 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1. Suppose the system uses FIFO page replacement with 3 frames, calculate the total page faults?

Answer:  **Question 8**


Correct

Mark 1.00 out of 1.00

 Flag question

Which is CORRECT about the task Memory Map Unit (MMU)?


Select one:

- ☐ MM allocates memory for processes
- ☐ MMU maps a physical address into a logic address
- ☐ MMU loads a program into memory
- ☒ MMU maps a logic address into a physical address 

**Question 9**

Incorrect

Mark 0.00 out of 1.00


 Flag question

A system with 2-level page table in the form of (p1, p2, offset), and the content of page table No 2 of level 2 is: {(27, v), (213, i), (87, v), (826, v), (92, i)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10. Given a reference = 8389986, calculate its physical address, e.g., 12764 or Page fault?

Answer:  **Question 10**

Correct

Mark 1.00 out of 1.00

 Flag question

Suppose a paging system has the page fault rate=0.08%; the memory access time is: 320 nano seconds; and the page fault handling time is: 9 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  **Question 11**

Correct

Mark 1.00 out of 1.00

Suppose a paging system has the page fault rate=0.3%; the memory access time is: 250 nano seconds; and the page fault handling time is: 7 milli seconds. How many times the performance is slowdown? (eg. 87).

Flag question

Answer: 85 ✓

### Question 12

Incorrect

Mark 0.00 out of 1.00

Flag question

A system with 2-level page table in the form of (p1, p2, offset), and the content of page table No 0 of level 2 is: {(27, v), (213, i), (87, v), (826, v), (92, v)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10. Given a reference = 13556, calculate its physical address, e.g., 12764 or Page fault?

Answer: Page fault ✗

### Question 13

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 6 milliseconds; page-fault rate is 2/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☐ 15.2 micro seconds
- ☐ 13.2 micro seconds
- ☒ 12.2 micro seconds ✓
- ☐ 14.2 micro seconds

### Question 14

Correct

Mark 1.00 out of 1.00

Flag question

Which is INCORRECT about Multiprogramming with a Fixed number of Tasks (MFT) memory allocation algorithm?

Select one:

- ☒ Memory is split into partitions of which the size can vary ✓
- ☐ Operating system manages the allocated and available partitions
- ☐ When a new process arrives, it finds a suitable partition to allocate to the process
- ☐ Memory is split into fixed partitions

### Question 15

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses FIFO page replacement algorithm with 3 frames. Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5, show the pages (in appearing order, e.g. 1, 2, 3, 4, 5) that are selected as victims to be swapped out?

Answer: 1, 2, 3, 4, 1, 2 ✓

### Question 16

Correct

Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5. Suppose a system uses FIFO page replacement algorithm with 3 frames. Calculate the total page faults?

Mark 1.00 out of 1.00

Flag question

Answer:

9



### Question 17

Incorrect

Mark 0.00 out of 1.00

Flag question

Which is INCORRECT about priority (memory) allocation?

Select one:

- ☒ It can prevent thrashing from occurring
- ☐ Frames are globally allocated
- ☐ High priority processes are allocated first
- ☐ It cannot prevent thrashing from occurring

### Question 18

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a paging system has the page fault rate=0.18%; the memory access time is: 320 nano seconds; and the page fault handling time is: 9 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:

52



### Question 19

Not answered

Marked out of 1.00

Flag question

A system with 2-level page table in the form of (p1, p2, offset), and the content of page table No 1 of level 2 is: {(612, v),(14, i),(123, v),(5, v),(756, i)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10. Given a reference =4196656, calculate its physical address, e.g., 12764?

Answer:



### Question 20

Incorrect

Mark 0.00 out of 1.00

Flag question

A system with 2-level page table, the frame size is 4KB; the address register is 32 bits, the row size of the page table is 4 bytes; the address register is divided into (p1, p2, offset) for fast address translation (no need to use multiplication and addition for calculating the physical address). Given a reference =4200746, the corresponding (p1, p2, offset) is?

Select one:

- ☐ (0, 1, 256)
- ☐ (1, 0, 256)
- ☒ (2, 0, 256)
- ☐ (0, 2, 256)

Finish review

### QUIZ NAVIGATION



Show one page at a time

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---

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INT2206-6 Summer 2018-2019

# Operating systems INT2206-6 Summer 2018-2019

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Started on	Sunday, 5 May 2019, 8:02 PM
State	Finished
Completed on	Sunday, 5 May 2019, 8:36 PM
Time taken	34 mins 49 secs
Marks	18.00/20.00
Grade	9.00 out of 10.00 (90%)

Question 1

Correct

Mark 1.00 out of 1.00

Flag question

Which is incorrect about MFT?

Select one:

☐

This memory allocation method causes internal fragmentation

☐

The memory for applications is divided into a number of partitions when the system boots up

☒

This is a memory allocation method which is widely used in current operating systems

☐

The size of the memory partitions may be different when the system boots up

Question 2

Correct

Mark 1.00 out of 1.00

Flag question

Which is the reason why a process can run when only a part of it is loaded into memory?

Select one:

☒

Because only one instruction is executed at a time

☐

Because related instructions are always in the same group

☐

Because we can indicate which instructions to run

☐

Because instructions of a process are independent

Question 3

Correct

Mark 1.00 out of 1.00

Flag question

Which is INCORRECT about paging (1-level page table)?

Select one:

☐

Pages are of equal size

☐

Virtual space is also divided into pages

☐

Page size is equal frame size

☒

It is a contiguous memory allocation method

Question 4

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 9 milliseconds; page-fault rate is 1/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

☒

9.2 micro seconds

☐

8.2 micro seconds

☐

6.2 micro seconds

☐ 7.2 micro seconds

### Question 5

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a paging system has the page fault rate=0.3%; the memory access time is: 250 nano seconds; and the page fault handling time is: 7 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  ✓

### Question 6

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a paging system has the page fault rate=0.08%; the memory access time is: 150 nano seconds; and the page fault handling time is: 7 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  ✓

### Question 7

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a segment table with the following rows of (base, limit, valid): {(1432823, 1236, v), (876530, 8364, v), (3898764, 2894, i), (14987378, 45288, v), (2876906, 9862, i)}. Given a reference (s, offset)=(0, 894), identify its physical address?

Select one:

- ☒ 1433717 ✓
- ☐ 3899658
- ☐ 14988272
- ☐ 2877800

### Question 8

Incorrect

Mark 0.00 out of 1.00

Flag question

A system uses proportional memory allocation method. There are 3 processes in the system: P1, P2, P3 with the size of 138KB, 96KB, and 164KB, correspondingly. Suppose the memory size is 180KB, and the frame size is 2KB, calculate the number of frames allocated for processes P1, P2, P3 (e.g. 23:34:12)?

Answer:  ✗

### Question 9

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 8 milliseconds; page-fault rate is 3/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☐ 25.2 micro seconds
- ☐ 26.2 micro seconds
- ☐ 27.2 micro seconds
- ☒ 24.2 micro seconds ✓

### Question 10

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 6 milliseconds; page-fault rate is 2/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☐ 13.2 micro seconds
- ☐ 14.2 micro seconds
- ☐ 15.2 micro seconds

☒ 12.2 micro seconds ✓

Question 11

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	4	1
1	12	0
2	5	1
3	23	0
4	51	1

Calculate the physical address of the logical address 4982? (e.g. 18932 or error)

Answer: 53110 ✓

Question 12

Incorrect

Mark 0.00 out of 1.00

Flag question

A system with 2-level page table, the frame size is 4KB; the address register is 32 bits, the row size of the page table is 4 bytes; the address register is divided into (p1, p2, offset) for fast address translation (no need to use multiplication and addition for calculating the physical address). Given a reference =8398178, the corresponding (p1, p2, offset) is, e.g., (12, 12, 12)?

Select one:

- ☐ (1, 2, 256)
- ☐ (1, 3, 256)
- ☐ (1, 0, 256)
- ☒ (2, 2, 256) ✗

Question 13

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses segmentation memory allocation. The content of the segment table (limit, base) of a process is [(1000, 1400), (400, 6300), (400, 4300), (1100, 3200), (1000, 4700)]. Calculate the physical address of the reference (4, 402) (e.g. a number or invalid)?

Answer: 5102 ✓

Question 14

Correct

Mark 1.00 out of 1.00

Given the reference string: 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1. Suppose the system uses Least Recently Used (LRU) page replacement algorithm with 3 frames. Calculate the total page faults?

Flag question

Answer: 12 ✓

Question 15  
Correct  
Mark 1.00 out of 1.00  
Flag question

Suppose a system uses paging (1-level page table) with the frame size of 4KB; the page table of a process is [56, 120, 3]. Which is the physical address of the reference (1, 196)?

Select one:

- ☐ 120\*1024+196
- ☐ 3\*4096+196
- ☐ 560\*4096+196
- ☒ 120\*4096+196 ✓

Question 16  
Correct  
Mark 1.00 out of 1.00  
Flag question

Suppose a system uses contiguous memory allocation with the following information: the base address is 13400; the limit register is 1200; and a reference is 1246. Which is the result of the Memory Management Unit (MMU)?

Select one:

- ☐ 1446
- ☐ 14646
- ☒ An error ✓
- ☐ 14154

Question 17  
Correct  
Mark 1.00 out of 1.00  
Flag question

Suppose a system uses proportional allocation based on the size of the processes. There are two processes A and B with the size of 10 and 127 frames, correspondingly. The memory size is 64 frames, calculate the number of frames allocated for A and B (e.g. 23:17)?

Answer: 5:59 ✓

Question 18  
Correct  
Mark 1.00 out of 1.00  
Flag question

A system with 2-level page table in the form of (p1, p2, offset), and the content of page table No 2 of level 2 is: {(612, v),(14, i),(123, v),(5, v),(756, i)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10. Given a reference =8407560, its physical address is?

Select one:

- ☐ 14996354
- ☐ 885506
- ☒ Page fault ✓
- ☐ 3907740

Question 19  
Correct  
Mark 1.00 out of 1.00  
Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

FRAME    VALID		
0	4	1
1	12	0



2                      5                      1

3                      23                      1

4                      51                      1

Calculate the physical address of the logical address 7289? (e.g. 18932 or error)

Answer:  ✓

Question 20

Correct

Mark 1.00 out of 1.00

Flag question

Given the reference string: 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1. Optimal (page replacement) algorithm) is used (with 3 frames), show the pages (in appearing order) that are selected as victims to be swapped out?

Select one:

- ☐ 7 1 0 3 4 2
- ☐ 7 0 1 4 3 2
- ☐ 7 1 4 1 3 2
- ☒ 7 1 0 4 3 2 ✓

Finish review

QUIZ NAVIGATION

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

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# Operating systems INT2206-6 Summer 2018-2019

Home ► My courses ► Operating Systems ► INT2206-6 Summer 2018-2019 ► 2 May - 8 May ► Bài kiểm tra chương 5-6

**Started on** Sunday, 5 May 2019, 8:00 PM

**State** Finished

**Completed on** Sunday, 5 May 2019, 8:34 PM

**Time taken** 34 mins 24 secs

**Marks** 16.00/20.00

**Grade** 8.00 out of 10.00 (80%)

## Question 1

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a paging system has the page fault rate=0.18%; the memory access time is: 320 nano seconds; and the page fault handling time is: 9 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer: 52



## Question 2

Not answered

Marked out of 1.00

Flag question

A system with 2-level page table in the form of (p1, p2, offset), and the content of page table No 0 of level 2 is: {(27, v), (213, i), (87, v), (826, v), (92, v)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10. Given a reference =13134, calculate its physical address, e.g., 12764 or Page fault?

Answer:



## Question 3

Correct

Mark 1.00 out of 1.00

Flag question

A system uses Translation Look-aside Buffer (TLB) for address translation in paging (1 level page table). Suppose the access time of TLB is 20ms; the access time of the memory is 200ms; and the hit rate of TLB is 84%. Which is the Effective Access Time (EAT) of the system?


Select one:

- ☐ 250 ms
- ☐ 253 ms
- ☒ 252 ms ✓
- ☐ 251 ms

**Question 4**

Correct

Mark 1.00 out of 1.00

 Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	75	1
1	12	0
2	5	1
3	23	1
4	132	0


Calculate the physical address of the logical address 264? (e.g. 18932 or error)

Answer: 77064

**Question 5**

Correct

Mark 1.00 out of 1.00

 Flag question

Suppose a system with 2-level page table; the address register is 52 bits; the frame size is 4KB; the row size of page table is 4 bytes; Which is the correct register division (in number of bits) for fast address translation in the form of (p1, p2, offset)?

Select one:

- ☐ (28, 12, 12)
- ☐ (30, 11, 11)
- ☒ (30, 10, 12) ✓
- ☐ (29, 11, 12)

**Question 6**

Correct

Mark 1.00 out of 1.00

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 8 milliseconds; page-fault rate is 1/1000. Which is the Effective Access Time (EAT) (in micro second) of the system?

Flag question

Select one:

- ☒ 8.2 micro seconds ✓
- ☐ 8.4 micro seconds
- ☐ 8.5 micro seconds
- ☐ 8.3 micro seconds

### Question 7

Correct

Mark 1.00 out of 1.00

Flag question

Suppose in a paging on demand system has the page fault rate = 0.2%; the memory access time=200 nano seconds; and the page fault handling time is 7 milli seconds. How many times the performance are slowdown? (e.g. 87)

Answer:  ✓

### Question 8

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 6 milliseconds; page-fault rate is 2/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☐ 13.2 micro seconds
- ☒ 12.2 micro seconds ✓
- ☐ 15.2 micro seconds
- ☐ 14.2 micro seconds

### Question 9

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	1291	1
1	12	0
2	5	1
3	23	1

4	132	0
---	-----	---

Calculate the physical address of the logical address 3782? (e.g. 18932 or error)

Answer: 24262



### Question 10

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses proportional allocation based on the size of the processes. There are two processes A and B with the size of 10 and 127 frames, correspondingly. The memory size is 64 frames, calculate the number of frames allocated for A and B (e.g. 23:17)?

Answer: 5:59



### Question 11

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 8 milliseconds; page-fault rate is 1/1000. Which is the Effective Access Time (EAT) (in micro second) of the system?

Select one:

- ☐ 8.4 micro seconds
- ☒ 8.2 micro seconds ✓
- ☐ 8.5 micro seconds
- ☐ 8.3 micro seconds

### Question 12

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as below, with the frame size=1KB.

	Frame	Valid
--	-------	-------

0	4	1
---	---	---

1	12	0
---	----	---

2	5	1
---	---	---

3	23	0
---	----	---

4	51	1
---	----	---

Which is the correct physical address of the reference 3678?

Select one:

- ☐ 12894
- ☐ 4702
- ☐ 52830
- ☒ error ✓

### Question 13

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a paging system has the page fault rate=0.08%; the memory access time is: 320 nano seconds; and the page fault handling time is: 7 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  ✓

### Question 14

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a paging system has the page fault rate=0.08%; the memory access time is: 250 nano seconds; and the page fault handling time is: 7 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  ✓

### Question 15

Not answered

Marked out of 1.00

Flag question


A system with 2-level page table, the frame size is 4KB; the address register is 32 bits, the row size of the page table is 4 bytes; the address register is divided into (p1, p2, offset) for fast address translation (no need to use multiplication and addition for calculating the physical address). Given a reference =13556, calculate the corresponding (p1, p2, offset), e.g., (2, 0, 46)?

Answer:  ✗

**Question 16**


Incorrect

Mark 0.00 out of 1.00

 Flag question

Suppose a system uses contiguous memory allocation with the following information: the base address is 13400; the limit register is 1200; and a reference is 1246. Which is the result of the Memory Management Unit (MMU)?


Select one:

- ☐ 1446
- ☒ 14646 
- ☐ 14154
- ☐ An error

**Question 17**

Correct

Mark 1.00 out of 1.00

 Flag question


Suppose a system uses segmentation memory allocation. The content of the segment table (limit, base) of a process is [(1000, 1400), (400, 6300), (400, 4300), (1100, 3200), (1000, 4700)]. Calculate the physical address of the reference (4, 138) (e.g. a number or invalid)?

Answer: 4838

**Question 18**


Correct

Mark 1.00 out of 1.00

 Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 9 milliseconds; page-fault rate is 3/1000. Which is the Effective Access Time (EAT) of the system?


Select one:

- ☐ 29.2 micro seconds
- ☐ 28.2 micro seconds
- ☒ 27.2 micro seconds 
- ☐ 26.2 micro seconds

**Question 19**


Correct

Mark 1.00 out of 1.00

 Flag question

Which is the reason why a process can run when only a part of it is loaded into memory?

Select one:

- ☐ Because instructions of a process are independent
- ☒ Because only one instruction is executed at a time 
- ☐ Because we can indicate which instructions to run
- ☐ Because related instructions are always in the same group

**Question 20**

Not answered

Marked out of 1.00

A system with 2-level page table in the form of (p1, p2, offset), and the content of page table No 1 of level 2 is: {(32, v), (45, i), (12, v), (5, v), (34, i)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10. Given a reference = 4225332, calculate its physical address, e.g., 12764?

Flag question

Answer:



Finish review

### QUIZ NAVIGATION

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

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2 May - 8 May ► Bài kiểm tra chương 5-6

## QUIZ NAVIGATION



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Finish review

**Started on** Sunday, 5 May 2019, 8:00 PM

**State** Finished

**Completed on** Sunday, 5 May 2019, 8:33 PM

**Time taken** 33 mins 29 secs

**Marks** 18.00/20.00

**Grade** 9.00 out of 10.00 (90%)

### Question 1

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 7 milliseconds; page-fault rate is 3/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☐ 24.2 micro seconds
- ☒ 21.2 micro seconds ✓
- ☐ 22.2 micro seconds
- ☐ 23.2 micro seconds

### Question 2

Incorrect

Mark 0.00 out of 1.00

Flag question

Which is incorrect about 1-level paging?

Select one:

- ☒ A reference is not valid with  $p \geq \text{PRLR}$ , where  $p$  is the page number of a reference ✗
- ☐ Page-table length register (PRLR) indicates the size of the page table
- ☐ Page-table base register (PTBR) is the register


pointing to the page table of the process

- ☐ The logical address must be in the form of (page, offset)

### Question 3

Correct

Mark 1.00 out of 1.00

 Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 6 milliseconds; page-fault rate is 1/1000. Which is the Effective Access Time (EAT) of the system?


Select one:

- ☐ 7.2 micro seconds
- ☐ 9.2 micro seconds
- ☒ 6.2 micro seconds ✓
- ☐ 8.2 micro seconds

### Question 4

Incorrect

Mark 0.00 out of 1.00

 Flag question


Suppose a paging system has the page fault rate=0.048%; the memory access time is: 320 nano seconds; and the page fault handling time is: 9 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  ✗

### Question 5

Correct

Mark 1.00 out of 1.00

 Flag question

A system with 2-level page table, and a process has only 5 pages, the content of page table No 2 of level 2 (p1, p2, offset) is: {(27, v),(213, i),(87, v), (826, v),(92, i)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bit for level 2 of the address register is 10. Given a reference =8398178, calculate its physical address, eg., 1929 or Page fault?

Answer:

✓

### Question 6

Correct

Mark 1.00 out of 1.00

Flag question

Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5. Suppose the system uses Least Recently Used (LRU) page replacement algorithm with 3 frames, calculate the total page faults?

Answer: 10



### Question 7

Correct

Mark 1.00 out of 1.00

Flag question

A system with 2-level page table, the frame size is 4KB; the address register is 32 bits, the row size of the page table is 4 bytes; the address register is divided into (p1, p2, offset) for fast address translation (no need to use multiplication and addition for calculating the physical address). Given a reference =13556, the corresponding (p1, p2, offset) is?

Select one:

- ☐ (2, 0, 312)
- ☐ (2, 2, 312)
- ☒ (3, 2, 312) ✓
- ☐ (3, 0, 312)

### Question 8

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging (1 level page table), and the access time of memory is 150 ms. Calculate the time to access the memory from a reference (p,d)?

Answer: 300



### Question 9

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

FRAME		VALID
0	4	1

1	12	0
---	----	---

2	5	1
---	---	---

3	23	0
---	----	---

4	51	1
---	----	---

Calculate the physical address of the logical address 2078? (e.g. 18932 or error)

Answer:

5150



### Question 10

Correct

Mark 1.00 out of 1.00

Flag question

A system with 2-level page table, the frame size is 4KB; the address register is 32 bits, the row size of the page table is 4 bytes; the address register is divided into (p1, p2, offset) for fast address translation (no need to use multiplication and addition for calculating the physical address). Given a reference =8398178, the corresponding (p1, p2, offset) is, e.g., (12, 12, 12)?


Select one:

- ☒ (1, 2, 256) ✓
- ☐ (1, 3, 256)
- ☐ (2, 2, 256)
- ☐ (1, 0, 256)

### Question 11

Correct

Mark 1.00 out of 1.00

 Flag question

Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5. Suppose the system uses Least Recently Used (LRU) page replacement algorithm with 4 frames, calculate the total page faults?

Answer:


8



### Question 12

Correct

Mark 1.00 out of 1.00

 Flag question

Which is INCORRECT about thrashing?


Select one:

- ☐ It is the situation where page fault rate is high, the time for serving page faults is high
- ☒ LRU page replacement algorithm can prevent thrashing from occurring ✓
- ☐ Working set model can prevent thrashing from occurring
- ☐ CPU utilization is low when thrashing occurs

### Question 13

Correct

Mark 1.00 out of 1.00

 Flag question

Suppose a system uses Multiprogramming with a Fixed number of Tasks (MFT) memory allocation algorithm with  $n$  partitions and  $m$  processes ( $m > n$ ). Which is INCORRECT?

Select one:

- ☒ A process can span over some partitions ✓
- ☐ The maximum number of allocated processes is  $n$
- ☐ There may be cases, the number of allocated processes is less than  $n$ .
- ☐ The whole process resides in a partition

### Question 14


Correct

Mark 1.00 out of 1.00

Which is correct about 2-level page table?

Select one:

- ☒ In order to apply fast physical address translation, the address register is divided into

 Flag question

(k, n, m) bits, where the page size is  $2^m$ ; and the number of page table row per page is  $2^n$




- ☐ The address register can be divided into (k, n, m) bits with any number of (k, n, m)
- ☐ 2-level is only used for large processes. For small processes, 1-level page table is activated
- ☐ A reference takes 2 memory accesses

### Question 15


Correct

Mark 1.00 out of 1.00

 Flag question

Which is CORRECT about associative memory?


Select one:

- ☐ It is system cache
- ☒ It is a cache used in address translation process 
- ☐ It is RAM
- ☐ It is a part of RAM

### Question 16

Correct


Mark 1.00 out of 1.00

 Flag question

A system uses working set model with  $\Delta=10$ .

Given a reference string: 2 6 1 5 7 7 7 5 1 6 2 3 4 4 4 3 4 4 1 3 2 3 4 4 4 3 4 4 4; Show the working set at 20th reference (e.g. 2 6 1 5 7)?


Answer:

2 3 4 6 

### Question 17


Correct

Mark 1.00 out of 1.00

 Flag question

Given the reference string: 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1. Optimal (page replacement algorithm) is used (with 3 frames), show the pages (in appearing order) that are selected as victims to be swapped out?

Select one:

- ☐ 7 1 4 1 3 2
- ☒ 7 1 0 4 3 2 


☐ 7 1 0 3 4 2

☐ 7 0 1 4 3 2

### Question 18

Correct

Mark 1.00 out of 1.00

 Flag question


Suppose in a paging on demand system has the page fault rate = 0.2%; the memory access time=200 nano seconds; and the page fault handling time is 7 milli seconds. How many times the performance are slowdown? (e.g. 87)

Answer:  

### Question 19

Correct

Mark 1.00 out of 1.00

 Flag question


Suppose a paging system has the page fault rate=0.3%; the memory access time is: 200 nano seconds; and the page fault handling time is: 7 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer:  


### Question 20

Correct

Mark 1.00 out of 1.00

 Flag question

Suppose a system uses paging (1 level page table), and the access time of memory is 200 ms. Calculate the time to access the memory from a reference (p,d)?

Answer:  

Finish review

You are logged in as Vũ Tùng Dương (Log out)  
INT2206-6 Summer 2018-2019



# Operating systems INT2206-6 Summer 2018-2019

Home ► My courses ► Operating Systems ► INT2206-6 Summer 2018-2019 ► 2 May - 8 May ► Bài kiểm tra chương 5-6

**Started on** Sunday, 5 May 2019, 8:00 PM

**State** Finished

**Completed on** Sunday, 5 May 2019, 8:35 PM

**Time taken** 34 mins 59 secs

**Marks** 17.00/20.00

**Grade** 8.50 out of 10.00 (85%)

## Question 1

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 8 milliseconds; page-fault rate is 1/1000. Calculate the Effective Access Time (EAT) (in micro second) of the system (e.g. 7.8)?

Answer: 8.2

## Question 2

Correct

Mark 1.00 out of 1.00

Flag question

Which is incorrect about MFT?

Select one:

- ☐ This memory allocation method causes internal fragmentation
- ☐ The memory for applications is divided into a number of partitions when the system boots up
- ☐ The size of the memory partitions may be different when the system boots up
- ☒ This is a memory allocation method which is widely used in current operating systems

## Question 3

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses segmentation memory allocation. The content of the segment table (limit, base) of a process is [(1000, 1400), (400, 6300), (400, 4300), (1100, 3200), (1000, 4700)]. Calculate the physical address of the reference (3, 106) (e.g. a number or invalid)?


Answer: 3306



**Question 4**


Incorrect

Mark 0.00 out of 1.00

 Flag question

A system with 2-level page table, and the content of page table No 1 of level 2 (p1, p2, offset) is: {(32, v),(45, i),(12, v),(5, v),(34, i)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10. Given a reference =4225332, its physical address is?


Select one:

- ☒ 170292 
- ☐ 215348
- ☐ 80180
- ☐ 162100

**Question 5**

Incorrect

Mark 0.00 out of 1.00


 Flag question

Suppose a paging system has the page fault rate=0.048%; the memory access time is: 320 nano seconds; and the page fault handling time is: 9 milli seconds. How many times the performance is slowdown? (eg. 87).


Answer:  **Question 6**

Correct

Mark 1.00 out of 1.00


 Flag question

Suppose a paging system has the page fault rate=0.08%; the memory access time is: 250 nano seconds; and the page fault handling time is: 7 milli seconds. How many times the performance is slowdown? (eg. 87).


Answer:  **Question 7**

Correct

Mark 1.00 out of 1.00


 Flag question

Suppose a system uses contiguous memory allocation with the following information: the base address is 1640; the limit register is 2400; and a reference is 164. Calculate the physical address of the above reference?

Answer:  **Question 8**

Correct

Mark 1.00 out of 1.00

 Flag question


Suppose a system uses FIFO page replacement algorithm with 3 frames. Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5, show the pages (in appearing order, e.g. 1, 2, 3, 4, 5 ...) causing a page fault.

Answer:  

**Question 9**

Incorrect

Mark 0.00 out of 1.00


 Flag question

Suppose a paging system has the page fault rate=0.08%; the memory access time is: 320 nano seconds; and the page fault handling time is: 7 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer: 19 **Question 10**

Correct

Mark 1.00 out of 1.00


 Flag question

Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5. Suppose the Optimal (page replacement) algorithm) is used (with 4 frames), show the pages (in appearing order, e.g. 1, 2, 3, 4, 1, 2) that cause a page fault?

Answer: 1, 2, 3, 4, 5, 4 **Question 11**

Correct

Mark 1.00 out of 1.00


 Flag question

Suppose a paging system has the page fault rate=0.18%; the memory access time is: 320 nano seconds; and the page fault handling time is: 9 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer: 52 **Question 12**


Correct

Mark 1.00 out of 1.00

 Flag question

Suppose a system has 4GB RAM with paging, and the frame size is 1KB, frame number field is 4 bytes. Which is the maximum size of a page table?


Select one:

- ☐ 2 MB
- ☐ 4 MB
- ☐ 8 MB
- ☒ 16 MB 

**Question 13**


Correct

Mark 1.00 out of 1.00

 Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 7 milliseconds; page-fault rate is 1/1000. Which is the Effective Access Time (EAT) of the system?


Select one:

- ☐ 6.2 micro seconds
- ☐ 9.2 micro seconds
- ☐ 8.2 micro seconds
- ☒ 7.2 micro seconds 

**Question 14**

Correct

Mark 1.00 out of 1.00

 Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	75	1
1	12	0
2	5	1
3	23	1
4	132	0


Calculate the physical address of the logical address 264? (e.g. 18932 or error)

Answer: 77064

**Question 15**

Correct

Mark 1.00 out of 1.00

 Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	4	1
1	12	0
2	5	1
3	23	0

4	51	1
---	----	---

Calculate the physical address of the logical address 3874? (e.g. 18932 or error)

Answer: error



### Question 16

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 8 milliseconds; page-fault rate is 1/1000. Which is the Effective Access Time (EAT) (in micro second) of the system?

Select one:

- ☐ 8.3 micro seconds
- ☐ 8.4 micro seconds
- ☒ 8.2 micro seconds ✓
- ☐ 8.5 micro seconds

### Question 17

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
--	-------	-------

0	4	1
---	---	---

1	12	0
---	----	---

2	5	1
---	---	---

3	23	0
---	----	---

4	51	1
---	----	---

Calculate the physical address of the logical address 1058? (e.g. 18932 or error)

Answer: error



### Question 18

Correct

Mark 1.00 out of 1.00

Flag question

Given the reference string: 7 0 1 2 0 3 0 4 2 3 0 3 2 1 2 0 1 7 0 1. Suppose the system uses FIFO page replacement with 3 frames. Show the order of pages that are selected as victims to be swapped out (e.g. 7 0 1 2 0 3 0)?

Answer: 7 0 1 2 3 0 4 2 3 0 1 2



### Question 19

Correct

Mark 1.00 out of 1.00

Flag question

Which is NOT a dynamic allocation algorithm used in MVT and MFT systems?

Select one:

- ☒ Well fit ✓
- ☐ Best fit
- ☐ Worst fit
- ☐ First fit

### Question 20

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system has 6GB RAM with paging, and the frame size is 1KB, frame number field is 4 bytes. Which is the maximum size of a page table?

Select one:

- ☐ 32 MB
- ☐ 8 MB
- ☒ 24 MB ✓
- ☐ 16 MB

Finish review

### QUIZ NAVIGATION

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

Show one page at a time

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INT2206-6 Summer 2018-2019



# Operating systems INT2206-6 Summer 2018-2019

Home ► My courses ► Operating Systems ► INT2206-6 Summer 2018-2019 ► 2 May - 8 May ► Bài kiểm tra chương 5-6

**Started on** Sunday, 5 May 2019, 8:03 PM

**State** Finished

**Completed on** Sunday, 5 May 2019, 8:38 PM

**Time taken** 34 mins 56 secs

**Marks** 19.00/20.00

**Grade** 9.50 out of 10.00 (95%)

## Question 1

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	Frame	Valid
0	4	1
1	12	0
2	5	1
3	23	0
4	51	1

Which is the correct physical address of the reference 3678?

Select one:

- ☐ 52830
- ☒ error ✓
- ☐ 4702

**Question 2**

Correct

Mark 1.00 out of 1.00

Flag question

Suppose in a paging on demand system has the page fault rate = 0.2%; the memory access time=200 nano seconds; and the page fault handling time is 7 milli seconds. How many times the performance are slowdown? (e.g. 87)

Answer: 71

**Question 3**

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 9 milliseconds; page-fault rate is 1/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☐ 6.2 micro seconds
- ☒ 9.2 micro seconds
- ☐ 7.2 micro seconds
- ☐ 8.2 micro seconds

**Question 4**

Correct

Mark 1.00 out of 1.00

Flag question

A system with 2-level page table in the form of (p1, p2, offset), and the content of page table No 1 of level 2 is: {(27, v),(213, i),(87, v),(826, v),(92, i)}. Suppose the frame size is 4KB; the address register is 32 bit, the number of bits for level 2 (p2) of the address register is 10. Given a reference =4200968, calculate its physical address, e.g., 12764 or Page fault?

Answer: Page fault

**Question 5**

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	4	1
1	12	0
2	5	1



3

23

0

4

51

1

Calculate the physical address of the logical address 4982? (e.g. 18932 or error)

Answer: 53110

**Question 6**

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 9 milliseconds; page-fault rate is 3/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☐ 29.2 micro seconds
- ☐ 28.2 micro seconds
- ☐ 26.2 micro seconds
- ☒ 27.2 micro seconds ✓

**Question 7**

Correct

Mark 1.00 out of 1.00

Flag question

Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5. Suppose the system uses Least Recently Used (LRU) page replacement algorithm with 3 frames, calculate the total page faults?

Answer: 10

**Question 8**

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses proportional allocation based on the size of the processes. There are two processes A and B with the size of 10 and 127 frames, correspondingly. The memory size is 64 frames, calculate the number of frames allocated for A and B (e.g. 23:17)?

Answer: 5:59

**Question 9**

Correct

Suppose a paging system has the page fault rate=0.008%; the memory access time is: 320 nano seconds; and the page fault handling time is: 9 milli seconds. How many times the performance is slowdown? (eg. 87).

5/5/2019 1.00 out of 1.00

Flag question

Answer: 3 Bài kiểm tra chương 5-6

### Question 10

Correct

Mark 1.00 out of 1.00

Flag question

A system uses Translation Look-aside Buffer (TLB) for address translation in paging (1 level page table). Suppose the access time of TLB is 20ms; the access time of the memory is 200ms; and the hit rate of TLB is 90%. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☐ 253 ms
- ☐ 260 ms
- ☐ 250 ms
- ☒ 240 ms ✓

### Question 11

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a paging system has the page fault rate=0.08%; the memory access time is: 320 nano seconds; and the page fault handling time is: 9 milli seconds. How many times the performance is slowdown? (eg. 87).

Answer: 23 ✓

### Question 12

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	4	1
1	12	0
2	5	1
3	23	0
4	132	1

Calculate the physical address of the logical address 4982? (e.g. 18932 or error)

Answer: 136054



### Question 13

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging (1-level page table) with the frame size of 4KB; the page table of a process is [56, 120, 3]. Which is the physical address of the reference (1, 1296)?

Select one:

- ☐  $120 \times 1024 + 1296$
- ☐  $560 \times 4096 + 1296$
- ☐  $3 \times 4096 + 1296$
- ☒  $120 \times 4096 + 1296$  ✓

### Question 14

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	97	1
1	12	0
2	5	1
3	23	1
4	132	0

Calculate the physical address of the logical address 3782? (e.g. 18932 or error)

**Question 15**

Correct

Mark 1.00 out of 1.00

Flag question

Which is INCORRECT about page replacement?

Select one:

- ☒ The swapped out page is always written into disk
- ☐ A victim will be selected to be swapped out
- ☐ The swapped out page is only written into disk if it is modified
- ☐ The page table of the process having the swapped out page will be updated

**Question 16**

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	97	1
1	98	0
2	3	1
3	56	1
4	61	0

Calculate the physical address of the logical address 1286? (e.g. 18932 or error)

Answer: error

**Question 17**

Incorrect

Which is incorrect about 1-level paging?

Mark 0.00 out of 1.00

Flag question

Select one:

- ☐ PRLR can be used to detect whether a page number is out of range
- ☐ Page-table base register (PTBR) is the register pointing to the page table of the process
- ☐ The logical address must be in the form of (page, offset)
- ☒ Page-table length register (PRLR) indicates the size of the page table ✗

### Question 18

Correct

Mark 1.00 out of 1.00

Flag question

Given the reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, 5. Suppose the Optimal (page replacement) algorithm) is used (with 4 frames), calculate the total page faults?

Answer:

6



### Question 19

Correct

Mark 1.00 out of 1.00

Flag question

Suppose a system uses paging on demand without a Translation Look-aside Table (TLB). The memory access time is 200 nano seconds; page-fault service time is 6 milliseconds; page-fault rate is 1/1000. Which is the Effective Access Time (EAT) of the system?

Select one:

- ☒ 6.2 micro seconds ✓
- ☐ 9.2 micro seconds
- ☐ 8.2 micro seconds
- ☐ 7.2 micro seconds

### Question 20

Correct

Mark 1.00 out of 1.00

Flag question

Given the 1-level page table of a process as bellow, with the frame size=1KB.

	FRAME	VALID
0	645	1
1	12	0
2	5	1
3	23	1

4

132

0

Calculate the physical address of the logical address 264? (e.g. 18932 or error)

Answer: 660744



Finish review

### QUIZ NAVIGATION

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

Show one page at a time

Finish review

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