UNIVERSIDAD DE INGENIERÍA Y TECNOLOGÍA

Curso:

Arquitectura de computadoras'

Laboratorio 02

Estudiante:

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Profesora:

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Question 1:

Waveform:

RTL schematic:

Synthesis:

Table:

/	Analysis	Synthesis
Cells	5	6
Ports	4	4
Nets	8	8

Question 2:

Waveform:

RTL schematic:

Synthesis:

Table:

/	Analysis	Synthesis
Cells	3	7
Ports	4	4
Nets	6	9

Question 3:

Waveform:

RTL schematic:

Synthesis:

Table:

/	Analysis	Synthesis
Cells	2	7
Ports	4	4
Nets	4	11

Question 4:

Behavioral:

Waveform:

RTL schematic:

Synthesis:

Table:

/	Analysis	Synthesis
Cells	4	11
Ports	6	6

Nets	6	15

Structural:

Waveform:

RTL schematic:

Synthesis:

Table:

/	Analysis	Synthesis
Cells	4	22
Ports	6	6
Nets	6	24

Implementación en la Basys3:

DIGILENT
BASYS 3