SAM V71

Atmel | SMART ARM-based Flash MCU

DATASHEET

Introduction

Atmel® | SMART SAM V71 is a high-performance Flash microcontroller (MCU) based on the 32-bit ARM® Cortex®-M7 RISC (5.04 CoreMark/MHz) processor with floating point unit (FPU). Designed for Automotive applications, the SAM V71 has been developed and manufactured according to the most stringent requirements of the international standard ISO-TS-16949. The device operates at a maximum speed of 300 MHz, features up to 2048 Kbytes of Flash, dual 16-Kbyte cache memory, up to 384 Kbytes of SRAM and is available in 64-, 100- and 144-pin packages.

The Atmel | SMART SAM V71 offers an extensive peripheral set, including Ethernet 10/100, dual CAN-FD, High-speed USB Host and Device plus PHY, up to 8 UARTs, I2S, SD/MMC interface, a CMOS camera interface, system control and a 12-bit ADC, as well as high-performance crypto-processors AES, SHA and TRNG.

Features

- Core
  - ARM Cortex-M7 running at up to 300 MHz(1)
  - 16 Kbytes of ICache and 16 Kbytes of DCache with Error Code Correction (ECC)
  - Single- and double-precision HW Floating Point Unit (FPU)
  - Memory Protection Unit (MPU) with 16 zones
  - DSP Instructions, Thumb®-2 Instruction Set
  - Embedded Trace Module (ETM) with instruction trace stream, including Trace Port Interface Unit (TPIU)
- Memories
  - Up to 2048 Kbytes embedded Flash with unique identifier and user signature for user-defined data
  - Up to 384 Kbytes embedded Multi-port SRAM
  - Tightly Coupled Memory (TCM) interface with four configurations (disabled, 2 x 32 Kbytes, 2 x 64 Kbytes, 2 x 128 Kbytes)
  - 16 Kbytes ROM with embedded Bootloader routines (UART0, USB) and IAP routines
  - 16-bit Static Memory Controller (SMC) with support for SRAM, PSRAM, LCD module, NOR and NAND Flash with on-the-fly scrambling

  - 16-bit SDRAM Controller (SDRAMC) interfacing up to 256 MB and with on-the-fly scrambling
- System
  - Embedded voltage regulator for single-supply operation
  - Power-on-Reset (POR), Brown-out Detector (BOD) and Dual Watchdog for safe operation
  - Quartz or ceramic resonator oscillators: 3 to 20 MHz main oscillator with failure detection, 12 MHz or 16 MHz needed for USB operations. Optional low-power 32.768 kHz for RTC or device clock
  - RTC with Gregorian calendar mode, waveform generation in low-power modes
  - RTC counter calibration circuitry compensates for 32.768 kHz crystal frequency variations
  - 32-bit low-power Real-time Timer (RTT)
  - High-precision Main RC oscillator with 12 MHz default frequency for device startup. In-application trimming access for frequency adjustment. 8/12 MHz are factory-trimmed.
  - 32.768 kHz crystal oscillator or Slow RC oscillator as source of low-power mode device clock (SLCK)
  - One 500 MHz PLL for system clock, one 480 MHz PLL for USB high-speed operations
  - Temperature Sensor
  - One dual-port 24-channel central DMA Controller (XDMAC)
- Low-Power Features
  - Low-power Sleep, Wait and Backup modes, with typical power consumption down to 1.1 µA in Backup mode with RTC, RTT and wakeup logic enabled
  - Ultra-low-power RTC and RTT
  - 1 Kbyte of backup RAM (BRAM) with dedicated regulator
- Peripherals
  - One Ethernet MAC (GMAC) 10/100 Mbps in MII mode and RMII with dedicated DMA. IEEE1588 PTP frames and 802.3az Energy-efficiency support. Ethernet AVB support with IEEE802.1AS Timestamping and IEEE802.1Qav credit-based traffic-shaping hardware support.
  - USB 2.0 Device/Mini Host High-speed (USBHS) at 480 Mbps, 4-Kbyte FIFO, up to 10 bidirectional endpoints, dedicated DMA
  - 12-bit ITU-R BT. 601/656 Image Sensor Interface (ISI)
  - Two master Controller Area Networks (MCAN) with Flexible Data Rate (CAN-FD) with SRAM-based mailboxes, time- and event-triggered transmission
  - MediaLB® device with 3-wire mode, up to 1024 x Fs speed, supporting MOST25 and MOST50 networks
  - Three USARTs. USART0/1/2 support LIN mode, ISO7816, IrDA®, RS-485, SPI, Manchester and Modem modes; USART1 supports LON mode.
  - Five 2-wire UARTs with SleepWalking™ support
  - Three Two-Wire Interfaces (TWIHS) (I^2C-compatible) with SleepWalking support
  - Quad I/O Serial Peripheral Interface (QSPI) interfacing up to 256 MB Flash and with eXecute-In-Place and on-the-fly scrambling
  - Two Serial Peripheral Interfaces (SPI)
  - One Serial Synchronous Controller (SSC) with I2S and TDM support
  - Two Inter-IC Sound Controllers (I2SC)
  - One High-speed Multimedia Card Interface (HSMCI) (SDIO/SD Card/e.MMC)
  - Four Three-Channel 16-bit Timer/Counters (TC) with Capture, Waveform, Compare and PWM modes, constant on time. Quadrature decoder logic and 2-bit Gray Up/Down Counter for stepper motor
  - Two 4-channel 16-bit PWMs with complementary outputs, Dead Time Generator and eight fault inputs per PWM for motor control, two external triggers to manage power factor correction (PFC), DC-DC and lighting control.
  - Two Analog Front-End Controllers (AFEC), each supporting up to 12 channels with differential input mode and programmable gain stage, allowing dual sample-and-hold at up to 1.7 Msps. Offset and gain error correction feature.
  - One 2-channel 12-bit 1 Msps-per-channel Digital-to-Analog Controller (DAC) with Differential and Over Sampling modes

  - One Analog Comparator Controller (ACC) with flexible input selection, selectable input hysteresis
- Cryptography
  - True Random Number Generator (TRNG)
  - AES: 256-, 192-, 128-bit Key Algorithm, Compliant with FIPS PUB-197 Specifications
  - Integrity Check Monitor (ICM). Supports Secure Hash Algorithm SHA1, SHA224 and SHA256.
- I/O
  - Up to 114 I/O lines with external interrupt capability (edge- or level-sensitivity), debouncing, glitch filtering and On-die Series Resistor Termination
  - Five Parallel Input/Output Controllers (PIO)
- Voltage
  - Single supply voltage from 3.0V to 3.6V
- Automotive
  - Qualification AEC-Q100 grade 2 ([-40°C : +105°C] ambient temperature)
- Packages
  - LQFP144, 144-lead LQFP, 20 x 20 mm, pitch 0.5 mm
  - TFBGA144, 144-ball TFBGA, 10 x 10 mm, pitch 0.8 mm
  - LQFP100, 100-lead LQFP, 14 x 14 mm, pitch 0.5 mm
  - TFBGA100, 100-ball TFBGA, 9 x 9 mm, pitch 0.8 mm
  - LQFP64, 64-lead LQFP, 10 x 10 mm, pitch 0.5 mm

Notes: 1. 300 MHz is at [-40°C : +105°C], 1.2V or with the internal regulator.

1. Description

The Atmel | SMART SAM V71 devices are members of a family of Automotive Flash microcontrollers based on the high-performance 32-bit ARM Cortex-M7 processor with Floating Point Unit (FPU). These devices operate at up to 300 MHz and feature up to 2048 Kbytes of Flash and up to 384 Kbytes of SRAM.

The on-chip SRAM can be configured as Tightly Coupled Memory (TCM) or system memory. A multi-port access to the SRAM guarantees a minimum access latency.

The peripheral set includes:

- **Connectivity interfaces**
  - Ethernet MAC (GMAC) with specific hardware support for Audio Video Bridging (AVB)
  - High-speed USB Device port and a high-speed USB Host port sharing an embedded transceiver
  - MediaLB (MLB) device interface
- **Memory interfaces**
  - High-speed Multimedia Card Interface (HSMCI) for SDIO/SD/e.MMC
  - External Bus Interface (EBI) featuring an SDRAM Controller
  - Static Memory Controller providing connection to SRAM, PSRAM, NOR Flash, LCD module and NAND Flash
- **Communication interfaces**
  - Controller Area Networks with Flexible Data Rate (CAN-FD)
  - Universal Synchronous Asynchronous Receiver Transmitters (USART)
  - Universal Asynchronous Receiver Transmitters (UART)
  - Two-wire Interfaces (TWI) supporting the I^2C protocol
  - Quad I/O Serial Peripheral Interface (QSPI)
  - Serial Peripheral Interfaces (SPI)
  - Serial Synchronous Controller (SSC) supporting I2S and TDM protocols
  - Inter-IC Sound Controllers (I2SC)
  - Image Sensor Interface (ISI)
- **Control and timing**
  - Enhanced Pulse Width Modulators (PWM)
  - General-purpose 16-bit timers with stepper motor and quadrature decoder logic support
  - Ultra low-power Real-Time Timer (RTT)
  - Ultra low-power Real-Time Clock (RTC)
- **Integrated analog capability**
  - Dual Analog Front-End (AFE) including a 12-bit Analog-to-Digital Converter (ADC), a Programmable Gain Amplifier (PGA), dual Sample-and-Hold and a digital averaging with up to 16-bit resolution
  - Dual-channel 12-bit Digital-to-Analog Converter (DAC)
  - Analog Comparator
- **Cryptography**
  - High-performance crypto-processors Advanced Encryption Standard (AES)
  - Secure Hash Algorithm (SHA)
  - True Random Number Generator (TRNG)
- **Power optimization**
  - Sleep mode
  - SleepWalking™ mode
  - Backup mode

- Clock system optimization
- Sending/reacting to events in Active and Sleep modes

The SAM V71 devices have three software-selectable low-power modes: Sleep, Wait and Backup. In Sleep mode, the processor is stopped while all other functions can be kept running. In Wait mode, all clocks and functions are stopped but some peripherals can be configured to wake up the system based on predefined conditions. This feature, called SleepWalking, performs a partial asynchronous wakeup, thus allowing the processor to wake up only when needed. In Backup mode, RTT, RTC and wakeup logic are running. In addition, in this mode, the device is able to meet the most stringent Key-Off requirements while retaining 1Kbyte of SRAM.

To optimize power consumption, the clock system has been designed to support different clock frequencies for selected peripherals. Moreover, the processor and bus clock frequency can be modified without affecting processing on, for example, the USB, U(S)ART, AFE and Timer Counter.

The SAM V71 devices are also capable of sending and reacting to events in Active and Sleep modes without processor intervention.

2. Configuration Summary

The SAM V71 devices differ in memory size, package and features. Table 2-1 summarizes the different configurations.

Table 2-1. Configuration Summary

Feature	SAMV71Q21	SAMV71Q20	SAMV71Q19	SAMV71N21	SAMV71N20	SAMV71N19	SAMV71J21	SAMV71J20	SAMV71J19
Flash (Kbytes)	2048	1024	512	2048	1024	512	2048	1024	512
Multi-port SRAM (Kbytes)	384		256	384		256	384		256
Cache(I/D) (Kbytes)	16/16								
Package	LQFP144 TFBGA144			LQFP100 TFBGA100			LQFP64		
Number of PIOs	114			75			44		
External Bus Interface	16-bit data, 4 chip selects, 24-bit address			–			–		
SDRAM Interface	Yes			–			–		
Media LB Interface	Yes								
Central DMA	24								
12-bit ADC	24 ch.(1)			10 ch.(1)			5 ch.(1)		
12-bit DAC	2 ch.			2 ch.			1 ch.		
Timer Counter Channels	12								
Timer Counter Channels I/O	36			9			3		
USART/UART	3/5(2)			3/5(2)			2/3(3)		
QSPI	Yes			Yes			SPI mode only		
SPI0	Yes			Yes			No		
SPI1	Yes			No			No		
USART SPI	3			3			0		
TWI	3			3			2		
HSMCI	1 port 4 bits			1 port 4 bits			–		
CAN	2 ports			2 ports			1 port		

Table 2-1. Configuration Summary (Continued)

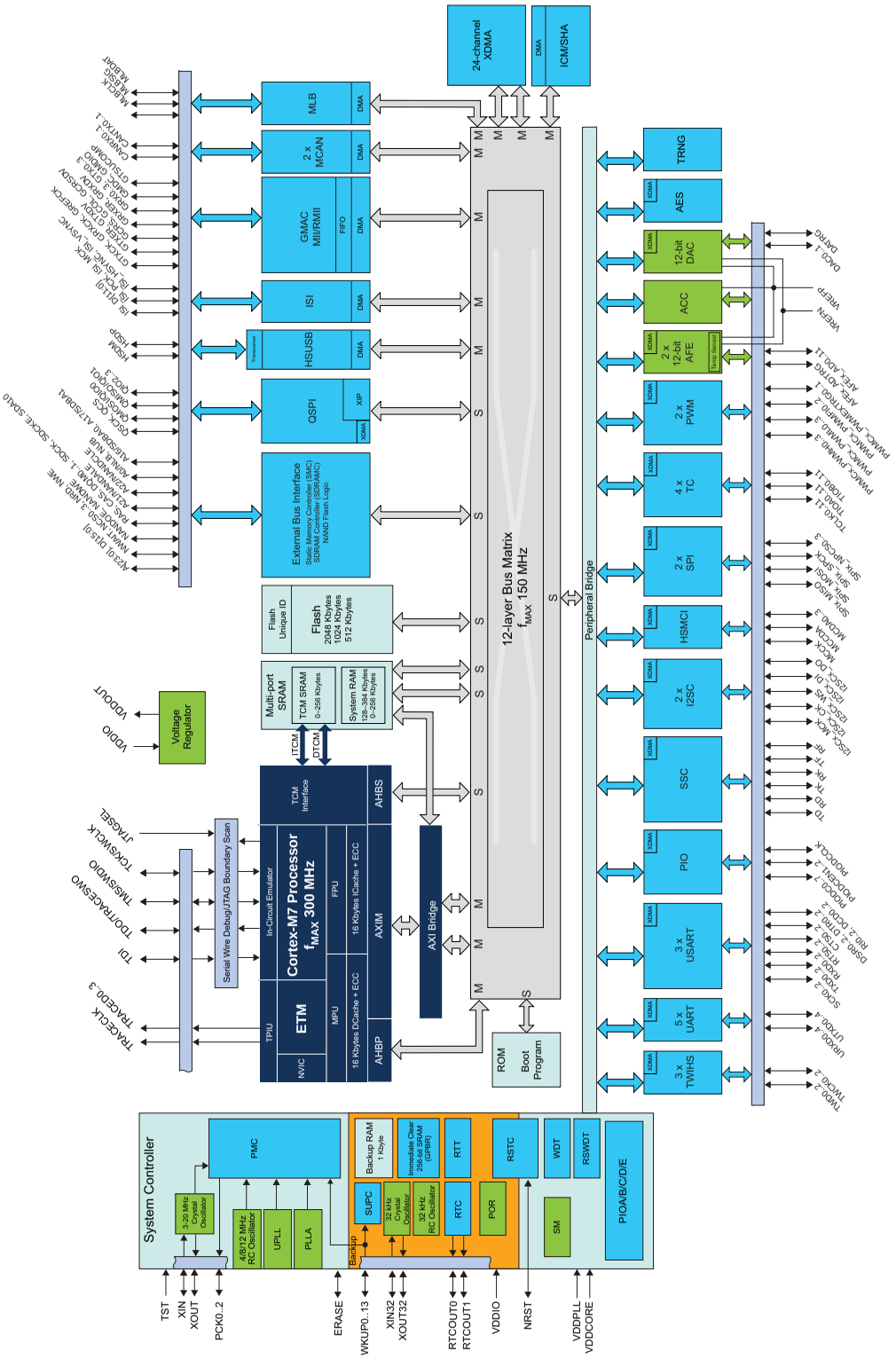
Feature	SAMV71Q21	SAMV71Q20	SAMV71Q19	SAMV71N21	SAMV71N20	SAMV71N19	SAMV71J21	SAMV71J20	SAMV71J19
GMAC	MII, RMII			MII, RMII			RMII		
ISI	12-bit			12-bit			8-bit		
SSC	Yes								
I2SC	2			1			0		
USB	High-speed			High-speed			High-speed		
Analog Comparator	Yes			Yes			Yes		
Embedded Trace Macrocell (ETM)	Yes			Yes			Yes		

Notes:
1. One channel is reserved for internal temperature sensor.
2. LON support on USART1 only.
3. USART functionality is limited to UART.

3. Block Diagram

See Table 2-1 for detailed configurations of memory size, package and features of the SAM V71 devices.

Figure 3-1. SAM V71 144-pin Block Diagram



4. Signal Description

Table 4-1 gives details on signal names classified by peripheral.

Table 4-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Power Supplies					
VDDIO	Peripherals I/O Lines Power Supply	Power	–	–	–
VDDIN	Voltage Regulator Input, AFE, DAC and Analog Comparator Power Supply[1]	Power	–	–	–
VDDOUT	Voltage Regulator Output	Power	–	–	–
VDDPLL	PLLA Power Supply	Power	–	–	–
VDDPLLUSB	USB PLL and Oscillator Power Supply	Power	–	–	–
VDDCORE	Powers the core, the embedded memories and the peripherals	Power	–	–	–
GND, GNDPLL, GNDPLLUSB, GNDANA, GNDUTMI	Ground	Ground	–	–	–
VDDUTMII	USB Transceiver Power Supply	Power	–	–	–
VDDUTMIC	USB Core Power Supply	Power	–	–	–
GNDUTMI	USB Ground	Ground	–	–	–
Clocks, Oscillators and PLLs					
XIN	Main Oscillator Input	Input	–	VDDIO	–
XOUT	Main Oscillator Output	Output	–		–
XIN32	Slow Clock Oscillator Input	Input	–		–
XOUT32	Slow Clock Oscillator Output	Output	–		–
PCK0–PCK2	Programmable Clock Output	Output	–		–
Real Time Clock					
RTCOUT0	Programmable RTC Waveform Output	Output	–	VDDIO	–
RTCOUT1	Programmable RTC Waveform Output	Output	–		–

Table 4-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Serial Wire Debug/JTAG Boundary Scan					
SWCLK/TCK	Serial Wire Clock / Test Clock (Boundary scan mode only)	Input	–	VDDIO	–
TDI	Test Data In (Boundary scan mode only)	Input	–		–
TDO/TRACESWO	Test Data Out (Boundary scan mode only)	Output	–		–
SWDIO/TMS	Serial Wire Input/Output / Test Mode Select (Boundary scan mode only)	I/O / Input	–		–
JTAGSEL	JTAG Selection	Input	High		–
Trace Debug Port					
TRACECLK	Trace Clock	Output	–	VDDIO	PCK3 is used for ETM
TRACED0–TRACED3	Trace Data	Output	–		–
Flash Memory					
ERASE	Flash and NVM Configuration Bits Erase Command	Input	High	VDDIO	–
Reset/Test					
NRST	Synchronous Microcontroller Reset	I/O	Low	VDDIO	–
TST	Test Select	Input	–		–
Universal Asynchronous Receiver Transceiver - UART(x=[0:4])					
URXDx	UART Receive Data	Input	–	–	PCK4 can be used to generate the baud rate
UTXDx	UART Transmit Data	Output	–	–	
PIO Controller - PIOA - PIOB - PIOC - PIOD - PIOE					
PA0–PA31	Parallel IO Controller A	I/O	–	VDDIO	–
PB0–PB9, PB12–PB13	Parallel IO Controller B	I/O	–		–
PC0– PC31	Parallel IO Controller C	I/O	–		–
PD0–PD31	Parallel IO Controller D	I/O	–	–	–
PE0–PE5	Parallel IO Controller E	I/O	–	–	–
PIO Controller - Parallel Capture Mode					
PIODC0–PIODC7	Parallel Capture Mode Data	Input	–	VDDIO	–
PIODCCLK	Parallel Capture Mode Clock	Input	–		–
PIODCEN1–PIODCEN2	Parallel Capture Mode Enable	Input	–		–
External Bus Interface					
D[15:0]	Data Bus	I/O	–	–	–
A[23:0]	Address Bus	Output	–	–	–
NWAIT	External Wait Signal	Input	Low	–	–
Static Memory Controller - SMC					

Table 4-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
NCS0–NCS3	Chip Select Lines	Output	Low	–	–
NRD	Read Signal	Output	Low	–	–
NWE	Write Enable	Output	Low	–	–
NWR0–NWR1	Write Signal	Output	Low	–	–
NBS0–NBS1	Byte Mask Signal	Output	Low	–	Used also for SDRAMC
NAND Flash Logic					
NANDOE	NAND Flash Output Enable	Output	Low	–	–
NANDWE	NAND Flash Write Enable	Output	Low	–	–
SDR-SDRAM Controller Logic					
SDCK	SDRAM Clock	Output	–	–	–
SDCKE	SDRAM Clock Enable	Output	–	–	–
SDCS	SDRAM Controller Chip Select	Output	–	–	–
BA0–BA1	Bank Select	Output	–	–	–
SDWE	SDRAM Write Enable	Output	–	–	–
RAS–CAS	Row and Column Signal	Output	–	–	–
SDA10	SDRAM Address 10 Line	Output	–	–	–
High Speed Multimedia Card Interface - HSMCI					
MCCK	Multimedia Card Clock	I/O	–	–	–
MCCDA	Multimedia Card Slot A Command	I/O	–	–	–
MCDA0–MCDA3	Multimedia Card Slot A Data	I/O	–	–	–
Universal Synchronous Asynchronous Receiver Transmitter USART(x=[0:2])					
SCKx	USARTx Serial Clock	I/O	–	–	PCK4 can be used to generate the baud rate
TXDx	USARTx Transmit Data	I/O	–	–	
RXDx	USARTx Receive Data	Input	–	–	
RTSx	USARTx Request To Send	Output	–	–	
CTSx	USARTx Clear To Send	Input	–	–	
DTRx	USARTx Data Terminal Ready	Output	–	–	
DSRx	USARTx Data Set Ready	Input	–	–	
DCDx	USARTx Data Carrier Detect	Input	–	–	
RIx	USARTx Ring Indicator	Input	–	–	
LONCOL1	LON Collision Detection	Input	–	–	
Synchronous Serial Controller - SSC					
TD	SSC Transmit Data	Output	–	–	–
RD	SSC Receive Data	Input	–	–	–
TK	SSC Transmit Clock	I/O	–	–	–
RK	SSC Receive Clock	I/O	–	–	–

Table 4-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
TF	SSC Transmit Frame Sync	I/O	–	–	–
RF	SSC Receive Frame Sync	I/O	–	–	–
Inter-IC Sound Controller - I2SC[1..0]					
I2SCx_MCK	Master Clock	Output	–	VDDIO	GCLK[PID] can be used to generate the baud rate
I2SCx_CK	Serial Clock	I/O	–	VDDIO	
I2SCx_WS	I2S Word Select	I/O	–	VDDIO	
I2SCx_DI	Serial Data Input	Input	–	VDDIO	
I2SCx_DO	Serial Data Output	Output	–	VDDIO	
Image Sensor Interface - ISI					
ISI_D0–ISI_D11	Image Sensor Data	Input	–	–	–
ISI_MCK	Image sensor Reference clock. No dedicated signal, PCK1 can be used.	Output	–	–	–
ISI_HSYNC	Image Sensor Horizontal Synchro	Input	–	–	–
ISI_VSYNC	Image Sensor Vertical Synchro	Input	–	–	–
ISI_PCK	Image Sensor Data clock	Input	–	–	–
Timer Counter - TC(x=[0:11])					
TCLKx	TC Channel x External Clock Input	Input	–	–	PCK6 can be used as an input clock PCK7 can be used as an input clock for TC0 only
TIOAx	TC Channel x I/O Line A	I/O	–	–	
TIOBx	TC Channel x I/O Line B	I/O	–	–	
Pulse Width Modulation Controller- PWMC(x=[0..1])					
PWMCx_PWMH0– PWMCx_PWMH3	Waveform Output High for Channel 0–3	Output	–	–	–
PWMCx_PWML0– PWMCx_PWML3	Waveform Output Low for Channel 0–3	Output	–	–	Only output in complementary mode when dead time insertion is enabled.
PWMCx_PWMFI0– PWMCx_PWMFI2	Fault Input	Input	–	–	–
PWMCx_PWMEXTRG0– PWMCx_PWMEXTRG1	External Trigger Input	Input	–	–	–
Serial Peripheral Interface - SPI(x=[0..1])					
SPIx_MISO	Master In Slave Out	I/O	–	–	–
SPIx_MOSI	Master Out Slave In	I/O	–	–	–
SPIx_SPCK	SPI Serial Clock	I/O	–	–	–
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	–	–
SPIx_NPCS1– SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low	–	–

Table 4-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
Quad IO SPI - QSPI					
QSCK	QSPI Serial Clock	Output	–	–	–
QCS	QSPI Chip Select	Output	–	–	–
QIO0–QIO3	QSPI I/O QIO0 is QMOSI Master Out Slave In QIO1 is QMISO Master In Slave Out	I/O	–	–	–
Two-Wire Interface - TWIHS(x=0..2)					
TWDx	TWIx Two-wire Serial Data	I/O	–	–	–
TWCKx	TWIx Two-wire Serial Clock	I/O	–	–	–
Analog					
VREFP	ADC, DAC and Analog Comparator Positive Reference	Analog	–	–	–
VREFN	ADC, DAC and Analog Comparator Negative Reference Must be connected to GND or GNDANA.	Analog	–	–	–
12-bit Analog Front End - (x=[0..1])					
AFEx_AD0–AFEx_AD11	Analog Inputs	Analog, Digital	–	–	–
AFEx_ADTRG	ADC Trigger	Input	–	VDDIO	–
12-bit Digital-to-Analog Converter - DAC					
DAC0–DAC1	Analog Output	Analog, Digital	–	–	–
DATRG	DAC Trigger	Input	–	VDDIO	–
Fast Flash Programming Interface - FFPI					
PGMEN0–PGMEN1	Programming Enabling	Input	–	VDDIO	–
PGMM0–PGMM3	Programming Mode	Input	–	VDDIO	–
PGMD0–PGMD15	Programming Data	I/O	–		–
PGMRDY	Programming Ready	Output	High		–
PGMNVALID	Data Direction	Output	Low		–
PGMNOE	Programming Read	Input	Low		–
PGMNCMD	Programming Command	Input	Low		–
USB High Speed - USBHS					
HSDM	USB High Speed Data -	Analog, Digital	–	VDDUTMII	–
HSDP	USB High Speed Data +		–		–
VBG	Bias Voltage Reference for USB	Analog	–	–	–
Ethernet MAC 10/100 - GMAC					

Table 4-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level	Voltage Reference	Comments
GREFCK	Reference Clock	Input	–	–	RMII only
GTXCK	Transmit Clock	Input	–	–	MII only
GRXCK	Receive Clock	Input	–	–	MII only
GTXEN	Transmit Enable	Output	–	–	–
GTX0 - GTX3	Transmit Data	Output	–	–	GTX0–GTX1 only in RMII
GTXER	Transmit Coding Error	Output	–	–	MII only
GRXDV	Receive Data Valid	Input	–	–	MII only
GRX0 - GRX3	Receive Data	Input	–	–	GRX0–GRX1 only in RMII
GRXER	Receive Error	Input	–	–	–
GCRS	Carrier Sense	Input	–	–	MII only
GCOL	Collision Detected	Input	–	–	MII only
GMDC	Management Data Clock	Output	–	–	–
GMDIO	Management Data Input/Output	I/O	–	–	–
GTSUCOMP	TSU timer comparison valid	Output	–	–	–
Controller Area Network - MCAN (x=[0:1])					
CANRXx	CAN Receive	Input	–	–	CANRX1 is available on PD28 for 100-pin only CANRX1 is available on PC12 for 144-pin only
CANTXx	CAN Transmit	Output	–	–	PCK5 can be used for CAN clock PCK6 and PCK7 can be used for CAN timestamping
MediaLB - MLB					
MLBCLK	MLB Clock	input	–	–	–
MLBSIG	MLB Signal	I/O	–	–	–
MLBDAT	MLB Data	I/O	–	–	–

Note: 1. Refer to Section 7.5 “Active Mode” for restrictions on the voltage range of analog cells.

5. Automotive Quality Grade

The SAM V71 has been developed and manufactured according to the most stringent requirements of the international standard ISO-TS-16949. This datasheet contains limit values extracted from the results of extensive characterization (temperature and voltage).

The quality and reliability of the SAM V71 has been verified during regular product qualification as per AEC-Q100 grade 2 (–40°C to +105°C).

Table 5-1. Temperature Grade Identification for Automotive Products

Temperature (°C)	Temperature Identifier	Comments
–40°C to +105°C	B	AEC-Q100 Grade 2

6. Package and Pinout

In the tables that follow, the column “Reset State” indicates the reset state of the line with mnemonics.

- “PIO” “/” signal

Indicates whether the PIO Line resets in I/O mode or in peripheral mode. If “PIO” is mentioned, the PIO line is maintained in a static state as soon as the reset is released. As a result, the bit corresponding to the PIO line in the register PIO_PSR (Peripheral Status Register) resets low.

If a signal name is mentioned in the “Reset State” column, the PIO line is assigned to this function and the corresponding bit in PIO_PSR resets high. This is the case of pins controlling memories, in particular the address lines, which require the pin to be driven as soon as the reset is released.

- “I” / ”O”

Indicates whether the signal is input or output state.

- “PU” / “PD”

Indicates whether pullup, pulldown or nothing is enabled.

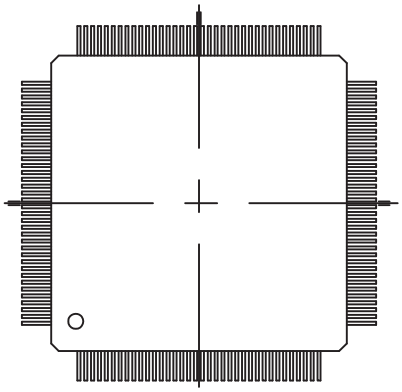
- “ST”

Indicates if Schmitt Trigger is enabled.

6.1 144-lead Packages

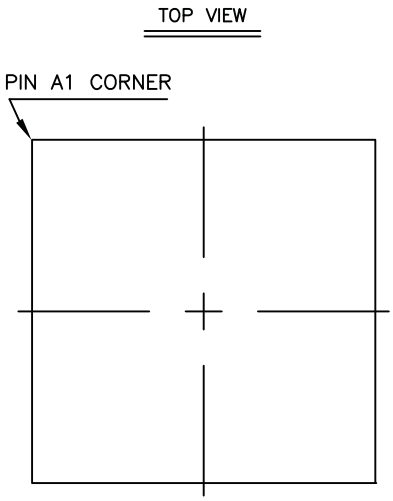
6.1.1 144-pin LQFP Package Outline

Figure 6-1. Orientation of the 144-pin LQFP Package



6.1.2 144-ball TFBGA Package Outline

Figure 6-2. Orientation of the 144-ball TFBGA Package



6.2 144-lead Package Pinout

Table 6-1. 144-lead Package Pinout

LQFP Pin	TFBGA Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		PIO Peripheral D		Reset State
				Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
102	C11	VDDIO	GPIO_AD	PA0	I/O	WKUP0[1]	I	PWMC0_PWMH0	O	TIOA0	I/O	A17/BA1	O	I2SC0_MCK	O	PIO, I, PU, ST
99	D12	VDDIO	GPIO_AD	PA1	I/O	WKUP1[1]	I	PWMC0_PWML0	O	TIOB0	I/O	A18	O	I2SC0_CK	I/O	PIO, I, PU, ST
93	E12	VDDIO	GPIO	PA2	I/O	WKUP2[1]	I	PWMC0_PWMH1	O	–	–	DATRG	I	–	–	PIO, I, PU, ST
91	F12	VDDIO	GPIO_AD	PA3	I/O	PIODC0[2]	I	TWD0	I/O	LONCOL1	I	PCK2	O	–	–	PIO, I, PU, ST
77	K12	VDDIO	GPIO	PA4	I/O	WKUP3/PIODC1[3]	I	TWCK0	O	TCLK0	I	UTXD1	O	–	–	PIO, I, PU, ST
73	M11	VDDIO	GPIO_AD	PA5	I/O	WKUP4/PIODC2[3]	I	PWMC1_PWML3	O	ISI_D4	I	URXD1	I	–	–	PIO, I, PU, ST
114	B9	VDDIO	GPIO_AD	PA6	I/O	–	–	–	–	PCK0	O	UTXD1	O	–	–	PIO, I, PU, ST
35	L2	VDDIO	CLOCK	PA7	I/O	XIN32[4]	I	–	–	PWMC0_PWMH3	O	–	–	–	–	PIO, HiZ
36	M2	VDDIO	CLOCK	PA8	I/O	XOUT32[4]	O	PWMC1_PWMH3	O	AFE0_ADTRG	I	–	–	–	–	PIO, HiZ
75	M12	VDDIO	GPIO_AD	PA9	I/O	WKUP6/PIODC3[3]	I	URXD0	I	ISI_D3	I	PWMC0_PWMFI0	I	–	–	PIO, I, PU, ST
66	L9	VDDIO	GPIO_AD	PA10	I/O	PIODC4[2]	I	UTXD0	O	PWMC0_PWMEXTRG0	I	RD	I	–	–	PIO, I, PU, ST
64	J9	VDDIO	GPIO_AD	PA11	I/O	WKUP7/PIODC5[3]	I	QCS	O	PWMC0_PWMH0	O	PWMC1_PWML0	O	–	–	PIO, I, PU, ST
68	L10	VDDIO	GPIO_AD	PA12	I/O	PIODC6[2]	I	QIO1	I/O	PWMC0_PWMH1	O	PWMC1_PWMH0	O	–	–	PIO, I, PU, ST
42	M3	VDDIO	GPIO_AD	PA13	I/O	PIODC7[2]	I	QIO0	I/O	PWMC0_PWMH2	O	PWMC1_PWML1	O	–	–	PIO, I, PU, ST
51	K6	VDDIO	GPIO_CLK	PA14	I/O	WKUP8/PIODCEN1[3]	I	QSCK	O	PWMC0_PWMH3	O	PWMC1_PWMH1	O	–	–	PIO, I, PU, ST
49	L5	VDDIO	GPIO_AD	PA15	I/O	–	–	D14	I/O	TIOA1	I/O	PWMC0_PWML3	O	I2SC0_WS	I/O	PIO, I, PU, ST
45	K5	VDDIO	GPIO_AD	PA16	I/O	–	–	D15	I/O	TIOB1	I/O	PWMC0_PWML2	O	I2SC0_DI	I	PIO, I, PU, ST
25	J1	VDDIO	GPIO_AD	PA17	I/O	AFE0_AD6[5]	I	QIO2	I/O	PCK1	O	PWMC0_PWMH3	O	–	–	PIO, I, PU, ST
24	H2	VDDIO	GPIO_AD	PA18	I/O	AFE0_AD7[5]	I	PWMC1_PWMEXTRG1	I	PCK2	O	A14	O	–	–	PIO, I, PU, ST
23	H1	VDDIO	GPIO_AD	PA19	I/O	AFE0_AD8/WKUP9[6]	I	–	–	PWMC0_PWML0	O	A15	O	I2SC1_MCK	O	PIO, I, PU, ST
22	H3	VDDIO	GPIO_AD	PA20	I/O	AFE0_AD9/WKUP10[6]	I	–	–	PWMC0_PWML1	O	A16/BA0	O	I2SC1_CK	I/O	PIO, I, PU, ST
32	K2	VDDIO	GPIO_AD	PA21	I/O	AFE0_AD1/ PIODCEN2[8]	I	RXD1	I	PCK1	O	PWMC1_PWMFI0	I	–	–	PIO, I, PU, ST
37	K3	VDDIO	GPIO_AD	PA22	I/O	PIODCCLK[2]	I	RK	I/O	PWMC0_PWMEXTRG1	I	NCS2	O	–	–	PIO, I, PU, ST
46	L4	VDDIO	GPIO_AD	PA23	I/O	–	–	SCK1	I/O	PWMC0_PWMH0	O	A19	O	PWMC1_PWML2	O	PIO, I, PU, ST
56	L7	VDDIO	GPIO_AD	PA24	I/O	–	–	RTS1	O	PWMC0_PWMH1	O	A20	O	ISI_PCK	I	PIO, I, PU, ST
59	K8	VDDIO	GPIO_AD	PA25	I/O	–	–	CTS1	I	PWMC0_PWMH2	O	A23	O	MCCK	O	PIO, I, PU, ST
62	J8	VDDIO	GPIO	PA26	I/O	–	–	DCD1	I	TIOA2	O	MCDA2	I/O	PWMC1_PWMFI1	I	PIO, I, PU, ST
70	J10	VDDIO	GPIO_AD	PA27	I/O	–	–	DTR1	O	TIOB2	I/O	MCDA3	I/O	ISI_D7	I	PIO, I, PU, ST
112	C9	VDDIO	GPIO	PA28	I/O	–	–	DSR1	I	TCLK1	I	MCCDA	I/O	PWMC1_PWMFI2	I	PIO, I, PU, ST
129	A6	VDDIO	GPIO	PA29	I/O	–	–	RI1	I	TCLK2	I	–	–	–	–	PIO, I, PU, ST

Table 6-1. 144-lead Package Pinout (Continued)

LQFP Pin	TFBGA Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		PIO Peripheral D		Reset State
				Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
116	A10	VDDIO	GPIO	PA30	I/O	WKUP11[1]	I	PWMC0_PWML2	O	PWMC1_PWMEXTRG0	I	MCDA0	I/O	I2SC0_DO	O	PIO, I, PU, ST
118	C8	VDDIO	GPIO_AD	PA31	I/O	–	–	SPI0_NPCS1	I/O	PCK2	O	MCDA1	I/O	PWMC1_PWMH2	O	PIO, I, PU, ST
21	H4	VDDIO	GPIO	PB0	I/O	AFE0_AD10/ RTCOUT0[7]	I	PWMC0_PWMH0	O	–	–	RXD0	I	TF	I/O	PIO, I, PU, ST
20	G3	VDDIO	GPIO	PB1	I/O	AFE1_AD0/ RTCOUT1[7]	I	PWMC0_PWMH1	O	GTSUCOMP	O	TXD0	I/O	TK	I/O	PIO, I, PU, ST
26	J2	VDDIO	GPIO	PB2	I/O	AFE0_AD5[5]	I	CANTX0	O	–	–	CTS0	I	SPI0_NPCS0	I/O	PIO, I, PU, ST
31	J3	VDDIO	GPIO_AD	PB3	I/O	AFE0_AD2/WKUP12[6]	I	CANRX0	I	PCK2	O	RTS0	O	ISI_D2	I	PIO, I, PU, ST
105	A12	VDDIO	GPIO_MLB	PB4	I/O	TDI[9]	I	TWD1	I/O	PWMC0_PWMH2	O	MLBCLK	I	TXD1	I/O	PIO, I, PD, ST
109	C10	VDDIO	GPIO_MLB	PB5	I/O	TDO/TRACESWO/ WKUP13[9]	O	TWCK1	O	PWMC0_PWML0	O	MLBDAT	I/O	TD	O	O, PU
79	J11	VDDIO	GPIO	PB6	I/O	SWDIO/TMS[9]	I	–	–	–	–	–	–	–	–	PIO,I,ST
89	F9	VDDIO	GPIO	PB7	I/O	SWCLK/TCK[9]	I	–	–	–	–	–	–	–	–	PIO,I,ST
141	A3	VDDIO	CLOCK	PB8	I/O	XOUT[10]	O	–	–	–	–	–	–	–	–	PIO, HiZ
142	A2	VDDIO	CLOCK	PB9	I/O	XIN[10]	I	–	–	–	–	–	–	–	–	PIO, HiZ
87	G12	VDDIO	GPIO	PB12	I/O	ERASE[9]	I	PWMC0_PWML1	O	GTSUCOMP	O	–	–	PCK0	O	PIO, I, PD, ST
144	B2	VDDIO	GPIO_AD	PB13	I/O	DAC0[11]	O	PWMC0_PWML2	O	PCK0	O	SCK0	I/O	–	–	PIO, I, PU, ST
11	E4	VDDIO	GPIO_AD	PC0	I/O	AFE1_AD9[5]	I	D0	I/O	PWMC0_PWML0	O	–	–	–	–	PIO, I, PU, ST
38	J4	VDDIO	GPIO_AD	PC1	I/O	–	–	D1	I/O	PWMC0_PWML1	O	–	–	–	–	PIO, I, PU, ST
39	K4	VDDIO	GPIO_AD	PC2	I/O	–	–	D2	I/O	PWMC0_PWML2	O	–	–	–	–	PIO, I, PU, ST
40	L3	VDDIO	GPIO_AD	PC3	I/O	–	–	D3	I/O	PWMC0_PWML3	O	–	–	–	–	PIO, I, PU, ST
41	J5	VDDIO	GPIO_AD	PC4	I/O	–	–	D4	I/O	–	–	–	–	–	–	PIO, I, PU, ST
58	L8	VDDIO	GPIO_AD	PC5	I/O	–	–	D5	I/O	TIOA6	I/O	–	–	–	–	PIO, I, PU, ST
54	K7	VDDIO	GPIO_AD	PC6	I/O	–	–	D6	I/O	TIOB6	I/O	–	–	–	–	PIO, I, PU, ST
48	M4	VDDIO	GPIO_AD	PC7	I/O	–	–	D7	I/O	TCLK6	I	–	–	–	–	PIO, I, PU, ST
82	J12	VDDIO	GPIO_AD	PC8	I/O	–	–	NWR0/NWE	O	TIOA7	I/O	–	–	–	–	PIO, I, PU, ST
86	G11	VDDIO	GPIO_AD	PC9	I/O	–	–	NANDOE	O	TIOB7	I/O	–	–	–	–	PIO, I, PU, ST
90	F10	VDDIO	GPIO_AD	PC10	I/O	–	–	NANDWE	O	TCLK7	I	–	–	–	–	PIO, I, PU, ST
94	F11	VDDIO	GPIO_AD	PC11	I/O	–	–	NRD	O	TIOA8	I/O	–	–	–	–	PIO, I, PU, ST
17	F4	VDDIO	GPIO_AD	PC12	I/O	AFE1_AD3[5]	I	NCS3	O	TIOB8	I/O	CANRX1	I	–	–	PIO, I, PU, ST
19	G2	VDDIO	GPIO_AD	PC13	I/O	AFE1_AD1[5]	I	NWAIT	I	PWMC0_PWMH3	O	SDA10	O	–	–	PIO, I, PU, ST
97	E10	VDDIO	GPIO_AD	PC14	I/O	–	–	NCS0	O	TCLK8	I	CANTX1	O	–	–	PIO, I, PU, ST
18	G1	VDDIO	GPIO_AD	PC15	I/O	AFE1_AD2[5]	I	NCS1/SDCS	O	PWMC0_PWML3	O	–	–	–	–	PIO, I, PU, ST
100	D11	VDDIO	GPIO_AD	PC16	I/O	–	–	A21/NANDALE	O	–	–	–	–	–	–	PIO, I, PU, ST
103	B12	VDDIO	GPIO_AD	PC17	I/O	–	–	A22/NANDCLE	O	–	–	–	–	–	–	PIO, I, PU, ST

Table 6-1. 144-lead Package Pinout (Continued)

LQFP Pin	TFBGA Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		PIO Peripheral D		Reset State
				Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
111	B10	VDDIO	GPIO_AD	PC18	I/O	–	–	A0/NBS0	O	PWMC0_PWML1	O	–	–	–	–	PIO, I, PU, ST
117	D8	VDDIO	GPIO_AD	PC19	I/O	–	–	A1	O	PWMC0_PWMH2	O	–	–	–	–	PIO, I, PU, ST
120	A9	VDDIO	GPIO_AD	PC20	I/O	–	–	A2	O	PWMC0_PWML2	O	–	–	–	–	PIO, I, PU, ST
122	A7	VDDIO	GPIO_AD	PC21	I/O	–	–	A3	O	PWMC0_PWMH3	O	–	–	–	–	PIO, I, PU, ST
124	C7	VDDIO	GPIO_AD	PC22	I/O	–	–	A4	O	PWMC0_PWML3	O	–	–	–	–	PIO, I, PU, ST
127	C6	VDDIO	GPIO_AD	PC23	I/O	–	–	A5	O	TIOA3	I/O	–	–	–	–	PIO, I, PU, ST
130	B6	VDDIO	GPIO_AD	PC24	I/O	–	–	A6	O	TIOB3	I/O	SPI1_SPCK	O	–	–	PIO, I, PU, ST
133	C5	VDDIO	GPIO_AD	PC25	I/O	–	–	A7	O	TCLK3	I	SPI1_NPCS0	I/O	–	–	PIO, I, PU, ST
13	F2	VDDIO	GPIO_AD	PC26	I/O	AFE1_AD7[5]	I	A8	O	TIOA4	I/O	SPI1_MISO	I	–	–	PIO, I, PU, ST
12	E2	VDDIO	GPIO_AD	PC27	I/O	AFE1_AD8[5]	I	A9	O	TIOB4	I/O	SPI1_MOSI	O	–	–	PIO, I, PU, ST
76	L12	VDDIO	GPIO_AD	PC28	I/O	–	–	A10	O	TCLK4	I	SPI1_NPCS1	I/O	–	–	PIO, I, PU, ST
16	F3	VDDIO	GPIO_AD	PC29	I/O	AFE1_AD4[5]	I	A11	O	TIOA5	I/O	SPI1_NPCS2	O	–	–	PIO, I, PU, ST
15	F1	VDDIO	GPIO_AD	PC30	I/O	AFE1_AD5[5]	I	A12	O	TIOB5	I/O	SPI1_NPCS3	O	–	–	PIO, I, PU, ST
14	E1	VDDIO	GPIO_AD	PC31	I/O	AFE1_AD6[5]	I	A13	O	TCLK5	I	–	–	–	–	PIO, I, PU, ST
1	D4	VDDIO	GPIO_AD	PD0	I/O	DAC1[11]	I	GTXCK	I	PWMC1_PWML0	O	SPI1_NPCS1	I/O	DCD0	I	PIO, I, PU, ST
132	B5	VDDIO	GPIO	PD1	I/O	–	–	GTXEN	O	PWMC1_PWMH0	O	SPI1_NPCS2	I/O	DTR0	O	PIO, I, PU, ST
131	A5	VDDIO	GPIO	PD2	I/O	–	–	GTX0	O	PWMC1_PWML1	O	SPI1_NPCS3	I/O	DSR0	I	PIO, I, PU, ST
128	B7	VDDIO	GPIO	PD3	I/O	–	–	GTX1	O	PWMC1_PWMH1	O	UTXD4	O	RI0	I	PIO, I, PU, ST
126	D6	VDDIO	GPIO_CLK	PD4	I/O	–	–	GRXDV	I	PWMC1_PWML2	O	TRACED0	O	DCD2	I	PIO, I, PU, ST
125	D7	VDDIO	GPIO_CLK	PD5	I/O	–	–	GRX0	I	PWMC1_PWMH2	O	TRACED1	O	DTR2	O	PIO, I, PU, ST
121	A8	VDDIO	GPIO_CLK	PD6	I/O	–	–	GRX1	I	PWMC1_PWML3	O	TRACED2	O	DSR2	I	PIO, I, PU, ST
119	B8	VDDIO	GPIO_CLK	PD7	I/O	–	–	GRXER	I	PWMC1_PWMH3	O	TRACED3	O	RI2	I	PIO, I, PU, ST
113	E9	VDDIO	GPIO_CLK	PD8	I/O	–	–	GMDC	O	PWMC0_PWMFI1	I	–	–	TRACECLK	O	PIO, I, PU, ST
110	D9	VDDIO	GPIO_CLK	PD9	I/O	–	–	GMDIO	I/O	PWMC0_PWMFI2	I	AFE1_ADTRG	I	–	–	PIO, I, PU, ST
101	C12	VDDIO	GPIO_MLB	PD10	I/O	–	–	GCRS	I	PWMC0_PWML0	O	TD	O	MLBSIG	I/O	PIO, I, PD, ST
98	E11	VDDIO	GPIO_AD	PD11	I/O	–	–	GRX2	I	PWMC0_PWMH0	O	GTSUCOMP	O	ISI_D5	I	PIO, I, PU, ST
92	G10	VDDIO	GPIO_AD	PD12	I/O	–	–	GRX3	I	CANTX1	O	SPI0_NPCS2	O	ISI_D6	I	PIO, I, PU, ST
88	G9	VDDIO	GPIO_CLK	PD13	I/O	–	–	GCOL	I	–	–	SDA10	O	–	–	PIO, I, PU, ST
84	H10	VDDIO	GPIO_AD	PD14	I/O	–	–	GRXCK	I	–	–	SDCKE	O	–	–	PIO, I, PU, ST
106	A11	VDDIO	GPIO_AD	PD15	I/O	–	–	GTX2	O	RXD2	I	NWR1/NBS1	O	–	–	PIO, I, PU, ST
78	K11	VDDIO	GPIO_AD	PD16	I/O	–	–	GTX3	O	TXD2	I/O	RAS	O	–	–	PIO, I, PU, ST
74	L11	VDDIO	GPIO_AD	PD17	I/O	–	–	GTXER	O	SCK2	I/O	CAS	O	–	–	PIO, I, PU, ST
69	M10	VDDIO	GPIO_AD	PD18	I/O	–	–	NCS1/SDCS	O	RTS2	O	URXD4	I	–	–	PIO, I, PU, ST
67	M9	VDDIO	GPIO_AD	PD19	I/O	–	–	NCS3	O	CTS2	I	UTXD4	O	–	–	PIO, I, PU, ST

Table 6-1. 144-lead Package Pinout (Continued)

LQFP Pin	TFBGA Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		PIO Peripheral D		Reset State
				Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
65	K9	VDDIO	GPIO	PD20	I/O	–	–	PWMC0_PWMH0	O	SPI0_MISO	I/O	GTSUCOMP	O	–	–	PIO, I, PU, ST
63	H9	VDDIO	GPIO_AD	PD21	I/O	–	–	PWMC0_PWMH1	O	SPI0_MOSI	I/O	TIOA11	I/O	ISI_D1	I	PIO, I, PU, ST
60	M8	VDDIO	GPIO_AD	PD22	I/O	–	–	PWMC0_PWMH2	O	SPI0_SPCK	O	TIOB11	I/O	ISI_D0	I	PIO, I, PU, ST
57	M7	VDDIO	GPIO_CLK	PD23	I/O	–	–	PWMC0_PWMH3	O	–	–	SDCK	O	–	–	PIO, I, PU, ST
55	M6	VDDIO	GPIO_AD	PD24	I/O	–	–	PWMC0_PWML0	O	RF	I/O	TCLK11	I	ISI_HSYNC	I	PIO, I, PU, ST
52	M5	VDDIO	GPIO_AD	PD25	I/O	–	–	PWMC0_PWML1	O	SPI0_NPCS1	I/O	URXD2	I	ISI_VSYNC	I	PIO, I, PU, ST
53	L6	VDDIO	GPIO	PD26	I/O	–	–	PWMC0_PWML2	O	TD	O	UTXD2	O	UTXD1	O	PIO, I, PU, ST
47	J6	VDDIO	GPIO_AD	PD27	I/O	–	–	PWMC0_PWML3	O	SPI0_NPCS3	O	TWD2	O	ISI_D8	I	PIO, I, PU, ST
71	K10	VDDIO	GPIO_AD	PD28	I/O	WKUP5[1]	I	URXD3	I	–	–	TWCK2	O	ISI_D9	I	PIO, I, PU, ST
108	D10	VDDIO	GPIO_AD	PD29	I/O	–	–	–	–	–	–	SDWE	O	–	–	PIO, I, PU, ST
34	M1	VDDIO	GPIO_AD	PD30	I/O	AFE0_AD0[5]	I	UTXD3	0	–	–	–	–	ISI_D10	I	PIO, I, PU, ST
2	D3	VDDIO	GPIO_AD	PD31	I/O	–	–	QIO3	I/O	UTXD3	O	PCK2	O	ISI_D11	I	PIO, I, PU, ST
4	C2	VDDIO	GPIO_AD	PE0	I/O	AFE1_AD11[5]	I	D8	I/O	TIOA9	I/O	I2SC1_WS	I/O	–	–	PIO, I, PU, ST
6	A1	VDDIO	GPIO_AD	PE1	I/O	–	–	D9	I/O	TIOB9	I/O	I2SC1_DO	O	–	–	PIO, I, PU, ST
7	B1	VDDIO	GPIO_AD	PE2	I/O	–	–	D10	I/O	TCLK9	I	I2SC1_DI	I	–	–	PIO, I, PU, ST
10	E3	VDDIO	GPIO_AD	PE3	I/O	AFE1_AD10[5]	I	D11	I/O	TIOA10	I/O	–	–	–	–	PIO, I, PU, ST
27	K1	VDDIO	GPIO_AD	PE4	I/O	AFE0_AD4[5]	I	D12	I/O	TIOB10	I/O	–	–	–	–	PIO, I, PU, ST
28	L1	VDDIO	GPIO_AD	PE5	I/O	AFE0_AD3[5]	I	D13	I/O	TCLK10	I/O	–	–	–	–	PIO, I, PU, ST
3	C3	VDDOUT	Power	VDDOUT	–	–	–	–	–	–	–	–	–	–	–	–
5	C1	VDDIN	Power	VDDIN	–	–	–	–	–	–	–	–	–	–	–	–
8	D2	GND	Reference	VREFN	I	–	–	–	–	–	–	–	–	–	–	–
9	D1	VDDIO	Reference	VREFP	I	–	–	–	–	–	–	–	–	–	–	–
83	H12	VDDIO	RST	NRST	I/O	–	–	–	–	–	–	–	–	–	–	I, PU
85	H11	VDDIO	TEST	TST	I	–	–	–	–	–	–	–	–	–	–	I, PD
30,43,72, 80,96	G8, H6, H7	VDDIO	Power	VDDIO	–	–	–	–	–	–	–	–	–	–	–	–
104	B11	VDDIO	TEST	JTAGSEL	I	–	–	–	–	–	–	–	–	–	–	I, PD
29,33,50, 81,107	E8, H5, H8	VDDCORE	Power	VDDCORE	–	–	–	–	–	–	–	–	–	–	–	–
123	J7	VDDPLL	Power	VDDPLL	–	–	–	–	–	–	–	–	–	–	–	–
134	E7	VDDUTMII	Power	VDDUTMII	–	–	–	–	–	–	–	–	–	–	–	–
136	B4	VDDUTMII	USBHS	HSDM	I/O	–	–	–	–	–	–	–	–	–	–	–
137	A4	VDDUTMII	USBHS	HSDP	I/O	–	–	–	–	–	–	–	–	–	–	–
44,61,95, 115,135,138	F5, F6, G4, G5, G6, G7	GND	Ground	GND	–	–	–	–	–	–	–	–	–	–	–	–

Table 6-1. 144-lead Package Pinout (Continued)

LQFP Pin	TFBGA Ball	Power Rail	I/O Type	Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		PIO Peripheral D		Reset State
				Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, HiZ, ST
–	D5	GNDANA	Ground	GNDANA	–	–	–	–	–	–	–	–	–	–	–	–
–	E5	GNDUTMI	Ground	GNDUTMI	–	–	–	–	–	–	–	–	–	–	–	–
–	E6	GNDPLLUSB	Ground	GNDPLLUSB	–	–	–	–	–	–	–	–	–	–	–	–
–	F7	GNDPLL	Ground	GNDPLL	–	–	–	–	–	–	–	–	–	–	–	–
139	B3	VDDUTMIC	Power	VDDUTMIC	–	–	–	–	–	–	–	–	–	–	–	–
140	C4	–	VBG	VBG	I	–	–	–	–	–	–	–	–	–	–	–
143	F8	VDDPLLUSB	Power	VDDPLLUSB	–	–	–	–	–	–	–	–	–	–	–	–

Notes:
1. WKUPx can be used if the PIO Controller defines the I/O line as "input".
2. To select this extra function, refer to Section 32.5.14 “Parallel Capture Mode”.
3. PIODCEN1/PIODCx has priority over WKUPx. Refer to Section 32.5.14 “Parallel Capture Mode”.
4. Refer to Section 23.4.2 “Slow Clock Generator”.
5. To select this extra function, refer to Section 52.5.1 “I/O Lines”. This selection is independent of the PIO line configuration. PIO lines must be configured according to required settings (PU or PD).
6. Analog input has priority over WKUPx pin. To select the analog input, refer to Section 52.5.1 “I/O Lines”. WKUPx can be used if the PIO controller defines the I/O line as "input".
7. Analog input has priority over RTCOUTx pin. To select the analog input, refer to Section 52.5.1 “I/O Lines”. Refer to Section 27.5.8 “Waveform Generation” to select RTCOUTx.
8. Analog input has priority over WKUPx pin. To select the analog input, refer to Section 52.5.1 “I/O Lines”. To select PIODCEN2, refer to Section 32.5.14 “Parallel Capture Mode”.
9. Refer to the System I/O Configuration Register in Section 19. “Bus Matrix (MATRIX)”.
10. Refer to Section 30.5.3 “Main Crystal Oscillator”. This selection is independent of the PIO line configuration. PIO lines must be configured according to XINxx (I) and XOUTxx (O).
11. DAC0 is selected when DACC_CHER.CH0 is set. DAC1 is selected when DACC_CHER.CH1 is set. Refer to Section 53.7.4 “DACC Channel Enable Register”.