CS230: Practice Problem Set 1 (Autumn 2024)

Date posted: August 13, 2024

These are ungraded practice questions. You are strongly encouraged to solve these independently to ensure you understand the content taught in class.

1. (a) Given X = 0001001111110000 and Y = 0000110001011111. Calculate $Z = X - Y$ using 2's complement subtraction.

   (b) For example, Z = 0000110011001100, the positions of set bits (LSB is position 0) in Z will be the minterms. So, in this case $Z = \sum m(2, 3, 6, 7, 10, 11)$. Minimize the computed Z from (a) using a K-map.

2. Implement the below expression using a single 8 x 1 MUX.
   $F(A, B, C, D) = \sum m(1, 3, 4, 11, 12, 13, 14, 15)$.

3. By now, you must have figured out that NAND and NOR gates are universal gates (any Boolean logic circuit can be constructed using only NAND gates or NOR gates). Find out the minimum number of 2-input NAND gates or NOR gates (find both the counts) required to implement:

   (a) Half Adder

   (b) Full Adder

   (c) Full Subtractor

4. Let m and n be the number of input lines and output lines, respectively, for a decoder that is used to uniquely address a byte-addressable 1 GB RAM, then what is the minimum value of m+n?

5. Design a four-input priority encoder with the help of the table given below. D0 has the **highest** priority, and D3 has the **lowest** priority.

Inputs				**Outputs**		
D3	D2	D1	D0	A	B	C
0	0	0	0	X	X	0
X	X	X	1	0	0	1
X	X	1	0	0	1	1
X	1	0	0	1	0	1
1	0	0	0	1	1	1

Table 1: Truth Table for Priority Encoder

6. How many 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates?

7. Assume a full adder has a worst-case delay of 15 ns for *sum* output and 12 ns for *carry* output. If such adders are used to design a 16-bit ripple carry adder, then compute the worst-case delay of the circuit.

8. If instead of a ripple carry adder design for a 16-bit adder, we use a cascade of four 4-bit carry-lookahead adders, each of which has a worst-case delay of 25 ns for its *carry* output and worst-case delay of 30 ns for its *sum* outputs, then find the worst-case delay of such a 16-bit adder.

9. Let $f(w, x, y, z) = (w'x'y'z' + w'x'y'z + w'xyz' + w'xyz + wx'y'z' + wx'yz)$ be the given function of 4 variables w, x, y, z.
   Suppose only a single 4 x 1 MUX and a single 2-input XOR gate is available. Although inverters are available in plenty. Implement the above logic function using signals w, x to drive the select inputs $s1, s0$ of the multiplexer and single XOR gate and a **minimum** number of inverters.
   Express your solution uniquely by describing the logic expressions for the 4 data inputs $d0, d1, d2, d3$ of the multiplexer. Note that these expressions should adhere to the restriction of using a **single XOR** gate and a **minimum number of inverters**.

10. Using a 4 x 1 MUX with select inputs $S1, S0$ as A, B, implement the following function: $F(A, B, C, D) = \sum m(3, 4, 6, 9, 10, 11, 13, 14)$.
    Draw the circuit. Assume complements of inputs are available. In addition, you may use NOT, OR, AND or XOR gates. An **inefficient** implementation (unnecessary use of gates) will **not** receive full credits.

11. What is the value of xyz if the following expression is solved?
    $(11)_2 + (22)_3 + (33)_4 + (44)_5 = (xyz)_6$. a_b denotes a represented with base b.

12. You have to design a two-bit less than comparator logic circuit ($A < B$). The following incomplete circuit is provided to you. Name the appropriate logic gate for each box to complete the circuit.

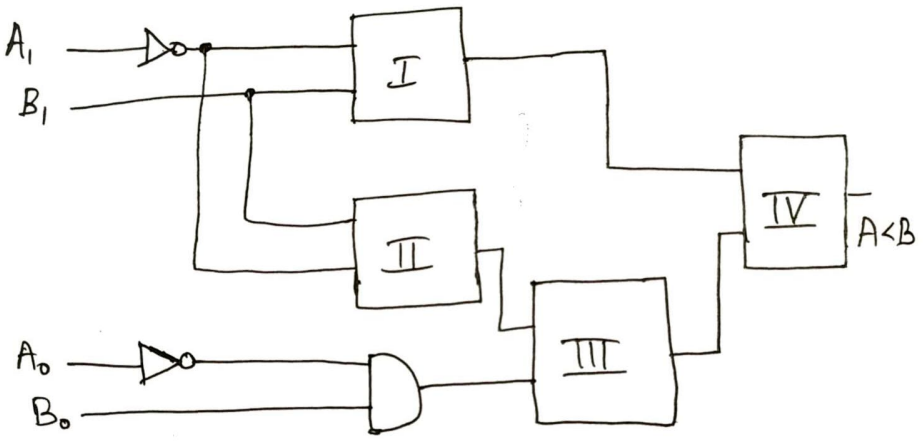

Figure 1: Incomplete circuit for Q.12

13. Minimize and realise the function f $= \overline{\overline{A} + [B + \overline{C} \cdot (\overline{A \cdot B + A \cdot \overline{C}})]}$ using minimum number of 2-input NOR gates.

14. Find dual and complement of the function $F = \overline{X \cdot Y \cdot Z + \overline{X} \cdot \overline{Y}} + Y \cdot Z$

15. What is the minimum number of 2-input NOR gates required to implement a 4-variable function represented in the form of minterms as,
$f = \sum m(0, 2, 5, 7, 8, 10, 13, 15)$? Draw the circuit.

16. Give the map of an irreducible four-variable function whose sum-of-products represents 2^3 minterms. Prove that there exists a function of n variables whose minimal sum-of-products form consists of 2^{n-1} minterms and that no function, when expressed in sum-of-products form, requires more than 2^{n-1} product terms. Derive a bound on the number of literals needed to express any n-variable function.

17. For the three functions shown below, obtain a multi-output minimized two-level implementation using an augmented prime implicant chart. Assume that minimizing the total number of gates is the sole objective.

    (a) $f1 = \sum(2, 3)$

    (b) $f2 = \sum(2, 3, 4, 5, 6, 7)$

    (c) $f3 = \sum(1, 3, 5, 7)$

Best wishes!