CS230: Practice Problem Set 2 (Autumn 2024)

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These are ungraded practice questions. You are strongly encouraged to solve these independently to ensure you understand the content taught in class.

1. Consider a sequential digital circuit consisting of T flip-flops and D flip-flops as shown in the figure. `CLKIN` is the clock input to the circuit. At the beginning, Q_1, Q_2, and Q_3 have values 0, 1, and 1, respectively.

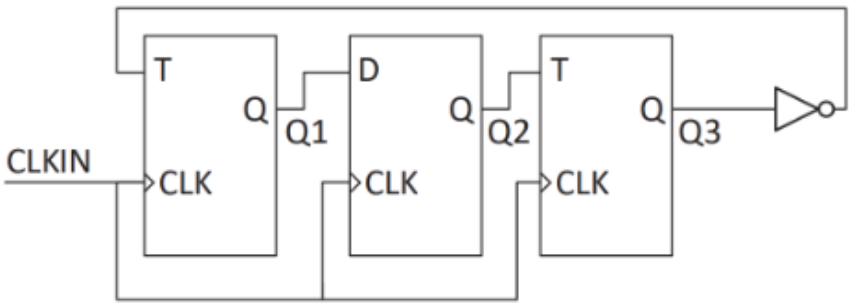

Figure 1: Sequential circuit for Q.18

   Analyze the circuit and determine the possible sequences of states for Q_1, Q_2, and Q_3. Determine the sequence of state of Q_1, Q_2, and Q_3 that can never occur.

2. Consider the circuit given below with initial state $Q_0 = 1$, $Q_1 = Q_2 = 0$. The state of the circuit is given by the value $4Q_2 + 2Q_1 + Q_0$. Note that this represents the decimal value corresponding to a state. For example, $Q_2 = 1$, $Q_1 = Q_0 = 0$ represents decimal value 4. Find the correct state sequence of the circuit.

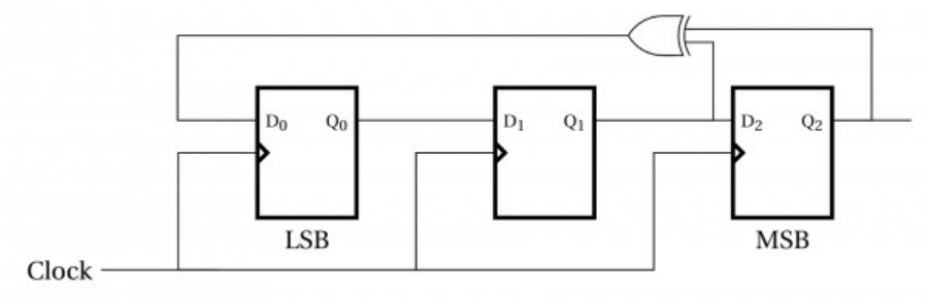

Figure 2: Sequential circuit for Q.2

3. Design a Mealy state machine that detects a sequence '110' in a stream of input bits. The machine should output '1' on the clock cycle following the detection of the sequence and '0' otherwise. Your design should minimize the number of states and transitions.

   (a) Draw the state diagram.

   (b) Derive the state transition table.

   (c) Implement the circuit using D flip-flops and logic gates.

4. A sequential circuit with two D flip-flops A and B, two inputs x and y, and one output z is specified by the following next-state and output equations:

$$A(t+1) = x'y + xB$$
$$B(t+1) = x'A + xB$$
$$z = A$$

   (a) Draw the logic diagram of the circuit.

   (b) List the state table for the sequential circuit.

   (c) Draw the corresponding state diagram.

5. Design a sequential circuit with two JK flip-flops A and B and two inputs E and F. The circuit should operate according to the following rules:

   (a) If $E = 0$, the circuit remains in the same state regardless of the value of F.

   (b) When $E = 1$ and $F = 1$, the circuit should go through the state transitions $00 \rightarrow 01 \rightarrow 10 \rightarrow 11 \rightarrow 00$ and repeat.

   (c) When $E = 1$ and $F = 0$, the circuit should go through the state transitions $00 \rightarrow 11 \rightarrow 10 \rightarrow 01 \rightarrow 00$ and repeat.

6. A Door opens if it ever sees the password 101 in a transmission. More formally, this FSM takes a bitstring consisting of 0's and 1's as its input and continually outputs 0's until it sees the substring 101, after which it outputs 1's continuously. Example execution of the FSM Input: 0001000101000101 Output:0000000001111111.

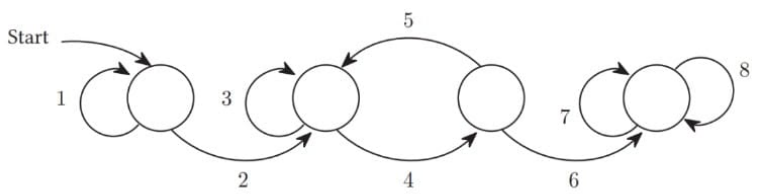

Figure 3: FSM for Q.6

   (a) Mark all the arrows numbered from 1 to 8 with appropriate transitions.

(b) Modify the above FSM to open the door when it detects the string "0110" in the transition.

(c) Extend your FSM to recognize two different patterns: "100" and "010". the FSM should output a continuous 1's after detecting either pattern.

7. Design a sequence detector that identifies the pattern 1101 in any given input, such as 011010110100011 and also detects the pattern 1010. The detector should output a high signal (1) for one clock cycle when either of the sequences is detected. The detector should be able to detect overlapping sequences and sequences that start in the middle of the input stream.

   (a) Draw a state diagram for the sequence detector that detects both patterns 1101 and 1010.

   (b) Decide whether your designed FSM should be a Mealy and/or Moore machine and provide justification for your design choice.

   (c) Draw the state diagram of your chosen machine (Mealy/Moore).

   (d) Draw the state table for your sequence detector. (also check for input stream '01101011010001100010101011101')

8. Design a synchronous counter that counts from 0 to 255 and then wraps around to 0, using only 8 flip-flops and a minimal number of gates.

   (a) Use only 8 flip-flops (D-type or T-type)

   (b) Use a minimal number of gates (AND, OR, NOT, etc.)

   (c) The counter should be synchronous, meaning that all flip-flops are clocked simultaneously

   (d) The counter should count from 0 to 255 and then wrap around to 0

   (e) The counter should have a single clock input and a single reset input

   Hint: You may need to combine binary and gray code to achieve the desired count sequence.

9. Consider the following finite state machine (FSM) table with six states. Minimize the number of states in the FSM using state equivalence while preserving the machine's original behaviour.

Table 1: Table for Q.9

Current State	Input	Next State	Output
A	0	B	0
A	1	C	1
B	0	A	0
B	1	D	1
C	0	E	0
C	1	F	1
D	0	B	0
D	1	C	1
E	0	A	0
E	1	D	1
F	0	C	0
F	1	E	1

(a) The minimized FSM should have the same input alphabet and output alphabet as the original FSM.

(b) The minimized FSM should produce the same output sequence for any given input sequence as the original FSM

Hint: You may need to use the concept of state equivalence

Best wishes!