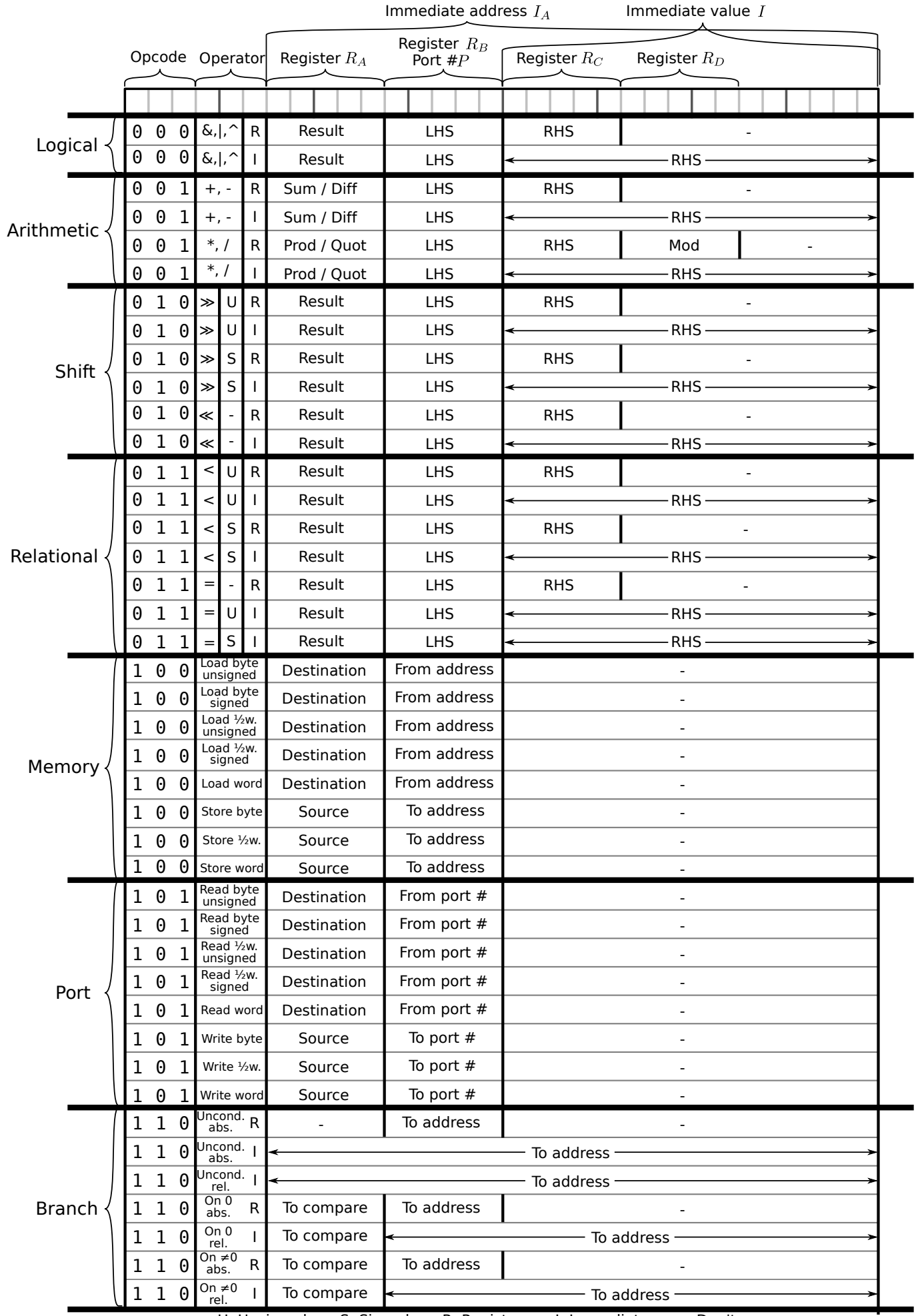

	Opcode	Operator			R_A	R_B / Port #P	R_C	R_D
Logical	0 0 0	&,|,^		R	Result	LHS	RHS	-
	0 0 0	&,|,^		I	Result	LHS	RHS	
Arithmetic	0 0 1	+, -		R	Sum / Diff	LHS	RHS	-
	0 0 1	+, -		I	Sum / Diff	LHS	RHS	
	0 0 1	*, /		R	Prod / Quot	LHS	RHS	Mod -
	0 0 1	*, /		I	Prod / Quot	LHS	RHS	
Shift	0 1 0	≫	U	R	Result	LHS	RHS	-
	0 1 0	≫	U	I	Result	LHS	RHS	
	0 1 0	≫	S	R	Result	LHS	RHS	-
	0 1 0	≫	S	I	Result	LHS	RHS	
	0 1 0	≪	-	R	Result	LHS	RHS	-
	0 1 0	≪	-	I	Result	LHS	RHS	
Relational	0 1 1	<	U	R	Result	LHS	RHS	-
	0 1 1	<	U	I	Result	LHS	RHS	
	0 1 1	<	S	R	Result	LHS	RHS	-
	0 1 1	<	S	I	Result	LHS	RHS	
	0 1 1	=	-	R	Result	LHS	RHS	-
	0 1 1	=	U	I	Result	LHS	RHS	
	0 1 1	=	S	I	Result	LHS	RHS	
Memory	1 0 0	Load byte unsigned			Destination	From address	-	
	1 0 0	Load byte signed			Destination	From address	-	
	1 0 0	Load ½w. unsigned			Destination	From address	-	
	1 0 0	Load ½w. signed			Destination	From address	-	
	1 0 0	Load word			Destination	From address	-	
	1 0 0	Store byte			Source	To address	-	
	1 0 0	Store ½w.			Source	To address	-	
	1 0 0	Store word			Source	To address	-	
Port	1 0 1	Read byte unsigned			Destination	From port #	-	
	1 0 1	Read byte signed			Destination	From port #	-	
	1 0 1	Read ½w. unsigned			Destination	From port #	-	
	1 0 1	Read ½w. signed			Destination	From port #	-	
	1 0 1	Read word			Destination	From port #	-	
	1 0 1	Write byte			Source	To port #	-	
	1 0 1	Write ½w.			Source	To port #	-	
	1 0 1	Write word			Source	To port #	-	
Branch	1 1 0	Uncond. abs.		R	-	To address	-	
	1 1 0	Uncond. abs.		I	To address			
	1 1 0	Uncond. rel.		I	To address			
	1 1 0	On 0 abs.		R	To compare	To address	-	
	1 1 0	On 0 rel.		I	To compare	To address		
	1 1 0	On ≠0 abs.		R	To compare	To address	-	
	1 1 0	On ≠0 rel.		I	To compare	To address		

U: Unsigned S: Signed R: Register I: Immediate -: Don't care
LHS: Left-hand side RHS: Right-hand side