

Demystifying AI Platform Design for Distributed Inference of Next-Generation LLM models

Abhimanyu Rajeshkumar Bambhaniya¹, Ritik Raj¹, Geonhwa Jeong², Souvik Kundu³, Sudarshan Srinivasan⁴, Suvinay Subramanian⁵, Midhilesh Elavazhagan⁴, Madhu Kumar⁴, Tushar Krishna¹
¹Georgia Institute of Technology, ²Meta, ³Intel Labs, ⁴Intel, ⁵Google
Corresponding email: abambhaniya3@gatech.edu

Abstract—Large language models (LLMs) have shown remarkable performance across a wide range of applications, often outperforming human experts. However, deploying these gigantic models efficiently for diverse inference use cases requires carefully designed hardware platforms with ample computing, memory, and network resources. With constant innovation in LLM serving optimizations and model architecture evolving at breakneck speed, the hardware requirements to meet Service Level Objectives (SLOs) remain an open research question. To answer the question, we present an analytical tool, GenZ, to efficiently navigate the relationship between diverse LLM model architectures, LLM serving optimizations, and AI platform design parameters. Our tool estimates LLM inference performance metrics for the given scenario. We have validated against real hardware platforms running various different LLM models, achieving a max geomean error of 5.82%. We use GenZ to identify compute, memory capacity, memory bandwidth, network latency, and network bandwidth requirements across diverse LLM inference use cases. We also study diverse architectural choices in use today (inspired by LLM serving platforms from several vendors) to help inform computer architects designing next-generation AI hardware accelerators and platforms. The source code is available at [GitHub](#). GenZ can also be tried out on its website without any setup on your web browser.

I. INTRODUCTION

The success of LLMs has fueled a growing interest in Generative AI use cases - spanning Question-Answer bots, text summarization, code generation, image generation, video generation, and more. Commercial products like ChatGPT, Gemini, Github Copilot [1], [2], [3], have performed astonishingly well in diverse metrics, often outperforming human experts [4]. LLMs have shown great scaling law properties [5], [6], with larger models [7], [8], [9] demonstrating better performance as compared to smaller ones [10]. Currently, the largest model has $\sim 1.8T$ parameters [11], and future LLMs could potentially have even a few hundred trillion parameters.

The design of LLM serving systems has become a hot area of research. This is due to its unique computational characteristics that set it apart from traditional Deep Learning inference and training. LLM serving involves two distinct stages: *prefill* and *decode*. The prefill stage consists of a single forward pass using all the input tokens. This is followed by an auto-regressive decode stage that generates one output token with each forward pass of the model. The prefill stage often portrays characteristics similar to a traditional forward pass (inference) and has significant computing requirements. In contrast, the

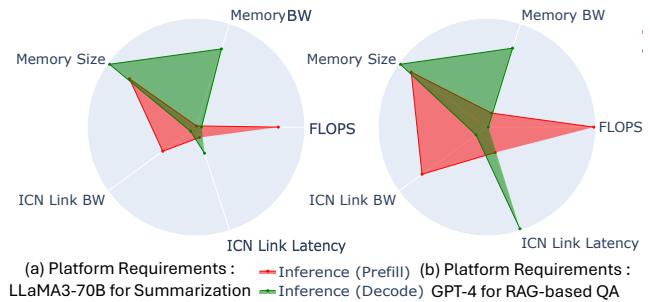


Fig. 1: Platform requirements for two workloads.

decode stage consumes (and generates) one token at a time and leverages a large cache of Key and Value projections of the input tokens, requiring high memory bandwidth (BW) and capacity (especially when processing long context queries). The metrics for LLM serving are also unique - with the use case playing a key role in determining the latency criticality of prefill vs decode tokens.

To state that LLM inference is an active area would be an understatement. The use cases for LLM inference continue to grow by the day. This is fueled by two trends. First, new LLM models with enhanced accuracy are being released at a rapid cadence by multiple competing AI labs [2], [17], [18], [19], [20], [21]. Second, for each model, a plethora of model-level (i.e., lossy) optimizations (such as quantization [22], [23], [24], pruning [25], [26], [27], fast token decoding [28], [29], [30], [31])) and system-level (i.e., lossless) optimizations (such as paged attention [32], flash attention [33], chunked inference [34], [35], scheduling [36]) are employed for enhancing performance by reducing the compute and memory footprint. Many of these optimization techniques have also become part of the popular inference-serving engine such as TensorRT-LLM [37], vLLM [32], and DeepSpeed-FastGen [34].

While GPU-based scaled-out platforms¹ have gone mainstream for large model training, the jury is out on the right architectural platform for LLM inference. Today, there exist

¹We define platform as the complete hardware back-end including multiple NPUs (e.g., GPUs or TPUs), local memories (e.g. HBM) and inter-NPU interconnect (e.g., NVlinks/XeLinks).

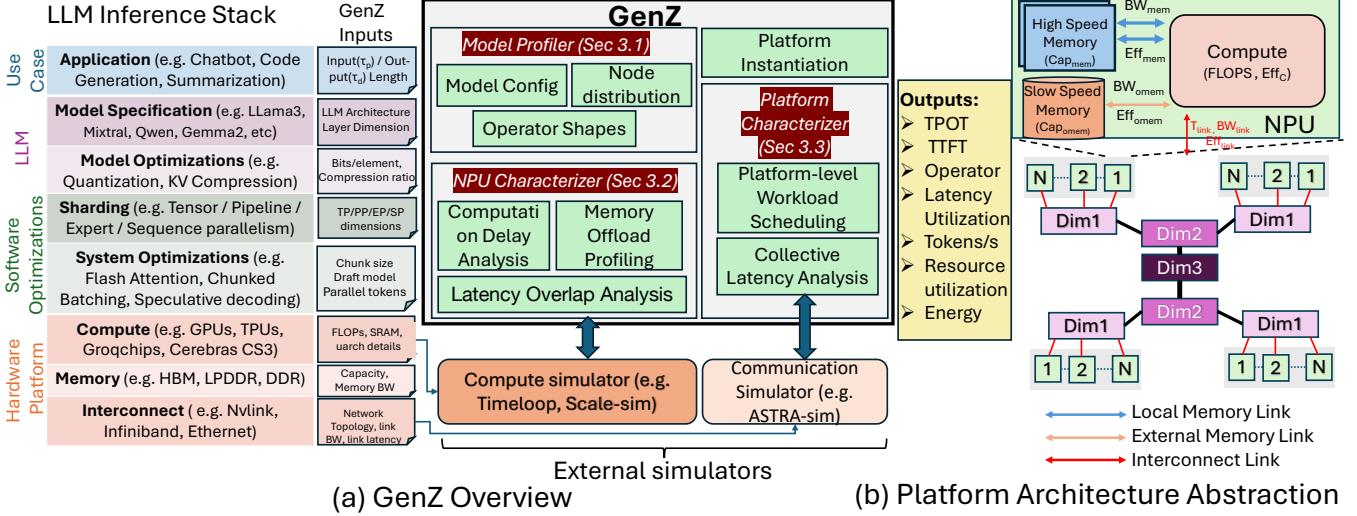


Fig. 2: An overview of GenZ framework.

Framework	LLM Architecture Supported	Model Level Optimizations* System Level Optimizations†	Distributed Platform Modeling		
			Parallelism	Network Hierarchy	Memory Hierarchy
ASTRA-sim [12]	Dense	None ✗	TP, PP	Multi-Level	Multi-Level (HBM + DRAM offload)
LLM-Viewer [13]	Dense, Dense-GQA	Flash-attention†, quantization*	TP	Single Level	Single-Level (HBM)
LLM-Compass [14]	Dense	None ✗	TP, PP	Single Level	Single-Level (HBM)
Vidur [15]	Dense, Dense-GQA	Flash-attention†, chunked prefill†	TP, PP	Real HW only	Single-Level (HBM)
LLMServingSim [16]	Dense	Flash-attention†, quantization*	TP, PP	Multi-Level	Single-Level (HBM)
GenZ (This Work)	Dense, Dense-GQA MoE, Mamba Sliding window attention	Flash-attention†, chunked prefill†, beam-search† speculative decoding†, quantization*, sparsity* mixed precision computation*, KV pruning*	TP, PP, EP	Multi-Level	Multi-Level (HBM + DRAM offload)

TABLE I: Comparison of prior works for modeling LLM inference against this work. TP, PP, and EP identify as Tensor, Pipeline, and Expert parallelism, respectively.

several architecturally distinct platforms that have *all* shown competitive performance across multiple LLM use cases [38]. Examples include GPU-based platforms from NVIDIA and AMD, programmable scaled-out dataflow processors from SambaNova, and SRAM-only architectures from Cerebras (via waferscale) and Groq (via hundreds of interconnected ASICs). There is also a lot of excitement around a plethora of emerging LLM platforms - such as transformer-specific ASICs from Etched [39] and high-speed photonics from Lightmatter [40].

We aim to demystify and quantify design insights for AI platforms across a suite of LLM model architectures, system optimizations and use cases. To this end, we introduce GenZ (Generative LLM analyZer), a framework for modeling and evaluating the relationship between LLM uses cases, model optimizations, software optimizations and the hardware platform and predict the end-to-end LLM inference performance. It should be noted that GenZ does not intend to simulate individual NPUs, rather we focus on simulating the distributed platforms for various LLM architectures combined with inference optimizations. While there exist valuable tools in the community to design NPUs [41], [42], [43] and distributed network fabric architectures [12], GenZ is the first tool, to the best of our knowledge, capturing the full-spectrum of LLM inference optimizations enabling the isolation and study of

specific model/software/hardware optimizations on the end-to-end LLM performance (or energy). Table I contrasts GenZ against related efforts on distributed platform modeling. In fact, GenZ is able to plug-in external tools for compute and communication to enable high-fidelity modeling of the underlying hardware. We validate GenZ thoroughly with various LLMs served across different platforms. Promisingly, across different workloads, GenZ can closely mimic the performance on diverse real platforms, achieving a geomean error of only 5.82%.

We demonstrate the value of GenZ via multiple case studies, answering several open questions surrounding hardware requirements stemming from diverse model types, software optimizations, and architectural choices across diverse use-cases. For instance, Fig. 1 highlights a subset of our key observations for two distinct scenarios.

In summary, this work makes the following contributions:

- ❶ We introduce GenZ, an analytical framework that helps analyze LLMs combined with various inference optimizations on different platforms (Section III). Fig. 2 shows an overview of our proposed framework.
- ❷ Using GenZ, we study the impact of various LLM serving optimizations with current hardware specifications, and present key insights to guide the next-generation design specifications (Section IV).
- ❸

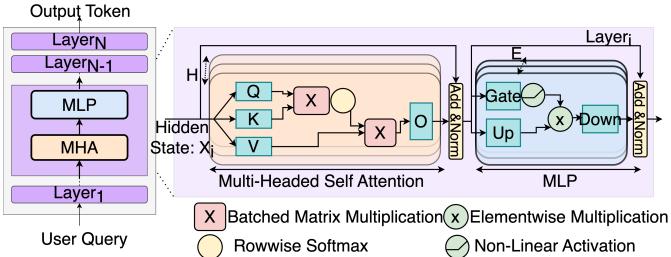


Fig. 3: Typical LLM Model Architecture. Each Layer has multiple parallel heads. For MoE models, there are multiple parallel MLP layers out of which ‘k’ are activated.

We present detailed runtime analysis across various LLM architectures based on both the transformer and state-space models (Section V). ④ Lastly, we showcase GenZ’s modeling capability through four case studies on the next-generation AI inference platform design: (1) isolated scaling of different platform characteristics (Section VII-A); (2) comparison of different AI platform architecture design choices (for example, SRAM-Chiplet, Wafer-Scale, GPUs, ASICs) (Section VII-B); (3) study design space choices of high bandwidth domain (HBD) size as well as associated interconnects (Section VII-C); and (4) study the impact of micro-architecture details and compute offloading(Section VII-D).

II. BACKGROUND

A. LLM Architecture

LLMs are generally designed by stacking multiple transformer decoder layers [44] as shown in Fig. 3. Each layer includes a multi-head self-attention (MHA) and a multi-layer perception (MLP). The key model parameters mainly include the model embedding dimensions (D_{model}), the number of heads (H), the feed-forward hidden dimension (D_{ff}), where D_{ff} is $W_{ff} * D_{model}$, and the number of decoder blocks/layers (L).

For each decoder layer, the input sequence is projected to three linear blocks generating three activations, namely ‘Query (Q)’, ‘Key (K)’, and ‘Value (V)’. The Q/K/V values are then split into H chunks each of width d, where $d = D_{model}/H$ that can be computed in parallel. For LLMs with group query attention (GQA), H_{kv} chunks of K/V are generated, and these chunks are shared by Q in $\frac{H}{H_{KV}}$ heads. For each attention head, corresponding Q and K are fed to a batch matrix multiplication operation that is then scaled and passed through a softmax operation to compute attention scores. The attention score is multiplied with the V chunk, generating output activations that are then projected via another linear layer. The output of MHA is added to the input of MHA and normalized.

The MLP module consists of three linear layers. FF_{up} , and FF_{gate} projects the input from D_{model} to the higher intermediate dimension D_{ff} . The output of FF_{gate} is activated using non-linear operation. This activation matrix is multiplied with the output of FF_{up} using an element-wise multiplication. FF_{down} projects the output of element-wise multiplication back

Model	D_{model}	Layers	Heads (H_{kv})	W_{ff}	Experts (Selected)
Gemma2- 2B [51]	2304	26	8(4)	4	-
LLaMA3- 8B [52]	4096	32	32(8)	3.5	-
Gemma2- 27B [51]	4608	46	32(16)	8	-
Mixtral- 8x22B [47]	6144	56	48(8)	2.66	8(2)
LLaMA3- 70B [52]	8192	80	64(8)	3.5	-
GPT3- 175B [7]	12288	96	96	4	-
LLaMA3- 405B [52]	16384	126	128(8)	3.25	-
GPT4- 1.8T [49]	10752	120	84	4	16(2)
Dense- 5T	49152	128	192(24)	4	-
MoE- 10T	13824	128	108(12)	4	32(4)

TABLE II: Different LLM architectures evaluated in this work.

to D_{model} . The output of MLP is added to the input of MLP and normalized. The final normalized value becomes the input to the decoder layer.

Mixture of Experts (MoE)[45] are special class of LLMs that consist of multiple “expert” multi-layer perceptron (MLP) layers, denoted as ‘E’, out of which ‘K’ experts are selected for each input token. In contrast, dense language models can be considered as a special case of MoEs, where $E = K = 1$, meaning there is only one expert MLP layer, and it is used for every input token. By introducing multiple experts and selectively activating a subset of them for each token, MoEs can effectively scale model capacity while maintaining efficient computation and memory usage, making them a promising approach for building larger and more capable language models. Some popular MoE models are Switch Transformers[45], Mixtral 8x7B[46], Mixtral 8x22B[47], DBRX[48], GROK[20], GPT-4[49], [50], [17]. Table II presents some of the state-of-the-art LLMs and associated dimensions.

B. Generative LLM Inference

Prefill. The prefill stage runs only once on input sequence of τ_p tokens to generate the K and V activations, which are often kept as the KV cache, for each LLM layer. The generated KV cache would be used for all subsequent output token generation. The prefill stage is **mostly compute-bounded** as all input tokens can be processed in parallel.

Decode. After the prefill stage, output tokens are generated auto-regressively, i.e. the last generated token is fed as an input to the LLM in each iteration, and one new output ‘token’ is generated. All the model weights and past KV cache are used to generate a single output token. Since input to the model is a single token, all matrix-matrix multiplications are converted into matrix-vector multiplications. This makes the generation stage **highly memory-bounded**. At the end of each generation step, the newly generated KV cache is padded to the existing KV cache, meaning its linear growth with the output sequence length. Generation stops when a special `<end-token>` is generated or the user limits the maximum number of output tokens. We define τ_d tokens are generated during the decode phase.

Chunked Prefill [35], [53], [54], [34] or *chunking* is a recent serving optimization used to reduce the hardware under-utilization by combining the two stages of LLM generation to provide better throughput. In chunked prefill, a chunk of fixed

size is fed to the model in each iteration. All existing decode batches are processed parallelly in the chunk. The remaining slots are filled by outstanding prefill requests. Since the prefill is broken down into smaller chunks combined with the decode stage, this ameliorates the memory boundedness of the decode stage and improves the overall throughput of the system. This often comes at slightly increased latency for the prefill stage.

Beam search [55], [56] is a heuristic search algorithm used during the decoding stage. It explores multiple potential sequences simultaneously, with the number of parallel sequences, called the beam size (S_b), typically set to 4. After the common prefill stage, two parallel beams are launched during the decode phase. The beam with the highest likelihood is selected as the final output.

C. Metrics for LLM Serving

The key metrics for LLM inference serving[57] are:

- 1) **Time To First Token ($TTFT$)**: Time to complete one forward pass with entire input, τ_p , and generate one output token.
- 2) **Time Per Output Token ($TPOT$)**: Time to generate an output token for each request. Consecutive tokens would have a time that is nearly identical to token generation. $TPOT$ for i^{th} output token is proportional to the model weights and $\tau_p + i$.
- 3) **Latency (T_{lat})**: The overall time it takes for the model to generate the full response for a user. Overall response latency can be calculated using the previous two metrics: $T_{lat} = TTFT + TPOT \times \tau_d$.
- 4) **Throughput (μ_{thr})**: Refers to the number of output tokens per second an inference platform can generate over a batch size of B . $\mu_{thr} = B / TPOT$.

III. GENZ : GENERATIVE LLM ANALYZER

GenZ is an analytical framework that can be used to study different LLM model architectures combined with the latest software optimizations on distributed current and next-generation NPU platforms. GenZ has three key components: 1) model profiler, 2) NPU characterizer, and 3) platform characterizer. We show an overview of GenZ in Fig. 2 and discuss each component in the following sections.

Real Life Application	# of Tokens Input/Output	Beam Width	TTFT / TPOT (s) / (ms)
Question Answering	1000/200	4	0.2 / 10
Chat Services	3000/1000	2	0.2 / 10
QA + RAG	10000/200	4	0.4 / 10
Text Summarization	15000/1000	4	2 / 20
Code Generation	20000/50	4	0.5 / 20

TABLE III: Representative Use Cases of LLM models and their representative input hyperparameters.

A. Model Profiler

Table II shows the parameters of various LLM models that we study in this work. These models serve as a representative set of current and future LLMs. GenZ model can model different LLM

architectures, including MoE-based LLMs (Mixtral-8x7B [46] and GPT4) and Mamba-based models [58]. LLaMA2, LLaMA3, Mixtral, and GPT3 architecture are available openly. We represent GPT4 as a 1.8T parameter mixture-of-experts model, with 120 layers [49], [50], [17]. A single layer of GPT4 has 16 experts of 111B parameters each, and two experts are activated for each token. We also hypothesize two future LLM models ² to represent scaled-up Dense-GQA and MoE models.

GenZ’s support for different architectures enables it to model all the SOTA LLMs. For each new model, GenZ uses the huggingface AutoModels [59] to determine the exact shape of each operator in the model. We store the operator dimension of layers. Using these stored variables, we calculate the number of operations, operator execution engine, operator residency information, operator size, KV cache estimation, collective sizes, and collective groups.

Saving model operators offline allows us to profile larger context lengths for any LLM model quickly. For example, LLaMA2-7B has a context length limit of 4K, but we can extend the context length to any size using this offline modeling.

We also model popular optimizations in this stage of model profiling, including Kernel Fusion (Flash Attention [33], [60], [61], Segment KV Caching [62]), model quantization, chunked prefilling [35], [34], speculative decoding [63], and beam search [55], [56]. Since this work focuses on LLM inference, we use FP8 model quantization for all our experiments and results unless specified otherwise.

B. NPU Characterizer

Our smallest hardware unit is the accelerator (alternatively referred as the NPU), as shown in Fig. 2. We assume each NPU has a certain number of compute cores, which can perform *FLOPS* number of operations per second. We use a variable ($Effc$) to account for the inefficiencies caused by the software and memory synchronization issues. For modeling real systems, GenZ uses the runtime of real systems (e.g. time to execute matmul operation on A100 GPU). This execution time is used to calculate the efficiency factor. This is the same methodology as adopted by previous works like Vidur [15]. For modeling future hypothetical NPUs, the microarchitecture of NPUs plays a crucial role in determining runtime of each operator. To effectively model the effects of microarchitecture, GenZ leverages external high-fidelity tools, such as Timeloop [64] and SCALE-sim [41], which specialize in simulating individual NPU dataflows and microarchitecture details. GenZ generates the operator dimensions for a given model architecture, system optimization, model optimization and parallelism strategy. This operator dimension is feed to the external tool to get the operator runtime, and thus get the hardware efficiency factor. Section VII-D shows a case study in which we model different microarchitecture using SCALE-sim[41] and study their effect on the prefill stage of LLama-3-8B.

Each NPU provides access to two external memories (fast and slow). Faster (smaller) memory represents an HBM/DDR

²We do not train these models for accuracy, which is not the focus of this work. We use it to study its computational behavior.

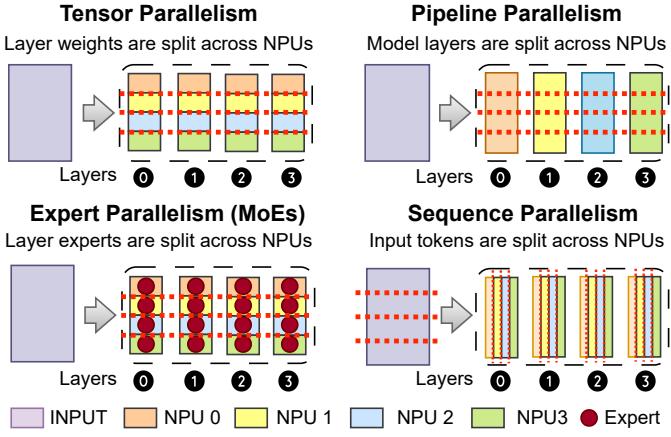


Fig. 4: Various parallelization strategies for neural network training and inference. Each colored box represents an accelerator (NPU), and the numbers correspond to model layers.

Memory Bank providing high BW(BW_{mem}), while Slower (Larger) memory could be PCIe-accessible CPU or CXL-accessible SSD/Flash (BW_{omem}) for offload. We also use an efficiency factor(Eff_{fmem} , Eff_{omem}) with the memory link for accurate memory access time.

Since all operations in LLM inference have pre-determined shapes and we use all model weights and KV cache uniformly, a smart compiler can try to maximize the overlap between the operator computation and memory fetches. Thus, we analyze the model’s performance on an operator-by-operator basis. For each operator, we calculate its corresponding operations per sec (C_{op}) and the number of memory accesses(M_{op}). We follow a roofline-based approach combined with separate efficiency factors (extracted from real hardware or open source simulators) for computation FLOPs and memory BW to calculate each operator’s runtime on the accelerator.

$$T_{op} = \max\left(\frac{C_{op}}{FLOPS \times Eff_C}, \frac{M_{op}}{BW_{mem} \times Eff_{fmem}}\right) \quad (1)$$

This simple yet effective modeling methodology is perfect for quickly estimating LLM serving trends on different hardware. In Section III-D1, we show that **using these efficiency factors, we can simulate the trends generated on real GPUs.**

C. Platform Characterizer

One of the key features of GenZ is its ability to simulate multi-dimensional network topologies for LLM inference. GenZ defines an inference platform as multiple NPUs connected through a multi-dimensional interconnection network (ICN), for scale-up and scale-out, as shown in Fig. 2. Each dimension in ICN has the following properties: link latency (T_{link}), network link bandwidth (BW_{link}), and network link efficiency (Eff_{link}).

Parallelism. Typically distributed LLMs are served using five different types of parallelism strategies: Data Parallel (DP), Tensor parallel (TP) [65], Pipeline parallel (PP) [66], Expert parallel (EP) [45] (Only for MoE models) and Sequence parallel (SP) [67], [68] (primarily for training long sequence). Fig. 4

shows the example of how different parallelism splits the input tokens and model weights. GenZ handles the overlap of physical topology and logical parallelism topology. For our experiments, we use the parallelism order as TP:EP:PP. This order points to how the NPUs are physically located to one other. For TP:EP:PP, the NPUs doing TP are physically the closest; next, NPUs with EP, and finally, nodes with PP. The degree of parallelism can be arbitrary, and GenZ will correctly map the logical parallelism mapping on the multi-dimension physical network topology defined by the user.

Collectives. For each degree of parallelism, GenZ generates the required collective pattern(s). There can be five kinds of collective patterns: AllReduce (TP & EP), All-to-All (EP), Send-Recv (PP), AllGather (SP & TP), and ReduceScatter (TP). GenZ allows the all-reduce collective to be broken down into ReduceScatter followed by AllGather for hiding the communication latencies. To get the runtime for each collective, we simulate it by calling the ASTRA-sim [69] system-layer as that provides implementations for diverse topology-aware collective algorithms. In our modeling, we also have a knob to decide whether to overlap collectives with compute tasks or execute them sequentially. For this work, we use non-overlapping communication similar to SOTA frameworks [70].

D. GenZ Implementation and Validation

1) *GenZ Implementation and Runtime:* GenZ is implemented in over 5,000 lines of Python code and packaged as a single Python module, enabling seamless integration into design space exploration (DSE) workflows via a simple pip installation. The tool is computationally lightweight, requiring approximately 30 milliseconds per forward pass on a standard 8-core CPU, given a batch size of 64 and 1024/256 input/output tokens. Runtime efficiency is further enhanced through operator reuse: GenZ identifies and skips redundant computations by sharing runtime estimates across layers.

2) *GenZ Validation:* We validate GenZ on five different real hardware platforms: a) HGX [71] box with 8 NVIDIA H100 SXM GPUs (80 GB) fully connected by NVLinks, b) 2xA100, c) Intel Gaudi2, d) AMD MI300x, e) 8xSamanova SN40L. To assess GenZ’s accelerator modeling, we analyze prefill, decode, and chunking trends across these systems.

Efficiency Factors: Our measured efficiency factors are derived from profiling real NPUs, following a methodology similar to Vidur [15]. We execute the same kernel multiple times and measure average utilization to obtain realistic efficiency estimates. LLM inference frameworks like vLLM execute static PyTorch computational graphs, ensuring consistent hardware utilization across runs. We validate our approach by comparing predicted runtimes against median measured runtimes, minimizing the impact of outliers. While we observe linearity in the validation data, it arises naturally from the predictable scaling of LLM inference workloads, where execution time for key bottlenecks (e.g., matrix multiplications, attention) scales proportionally with input size or batch size, rather than from manual tuning, as also observed in other works [72]. For each

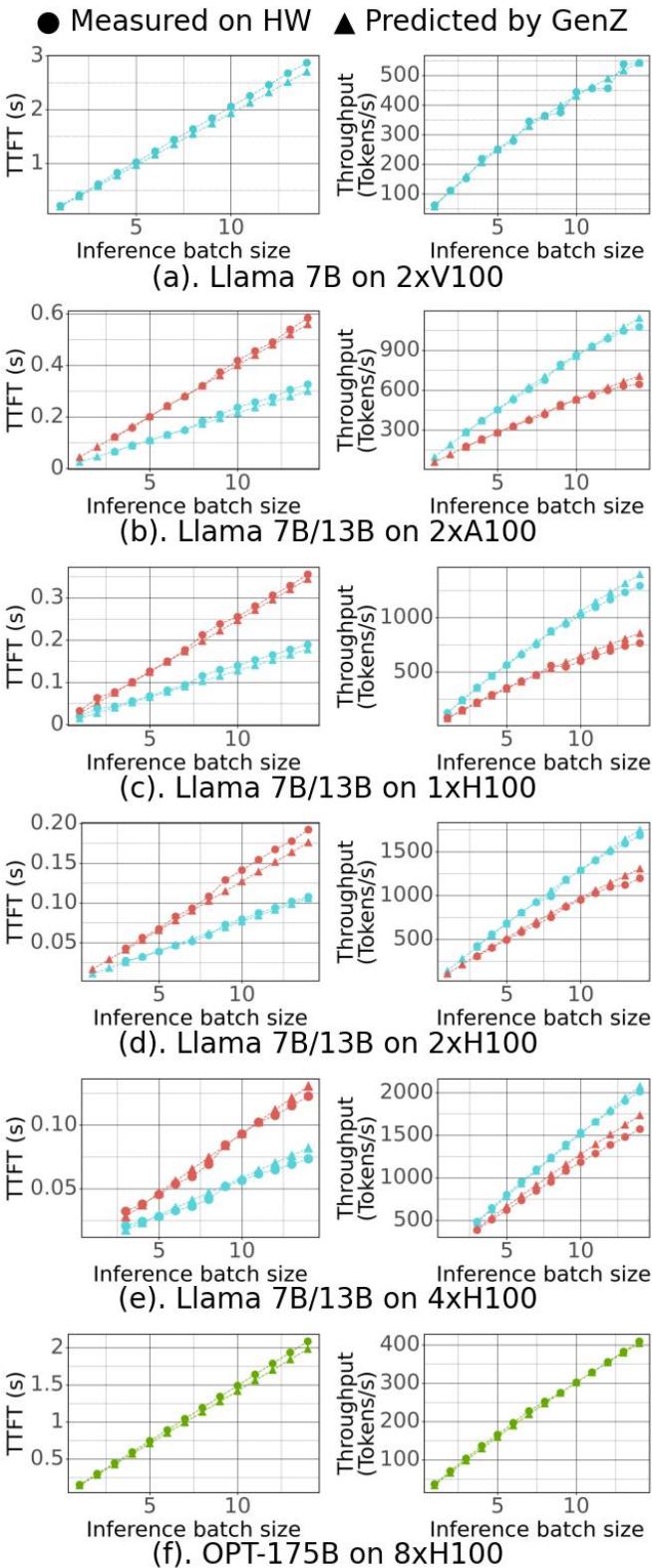


Fig. 5: GenZ LLM inference modeling against vLLM inference in prefill and decode stage for varying batch size on various platforms with different τ_p . Line color blue, red, and green represent LLaMA2-7B, LLaMA2-13B, and OPT-175B.

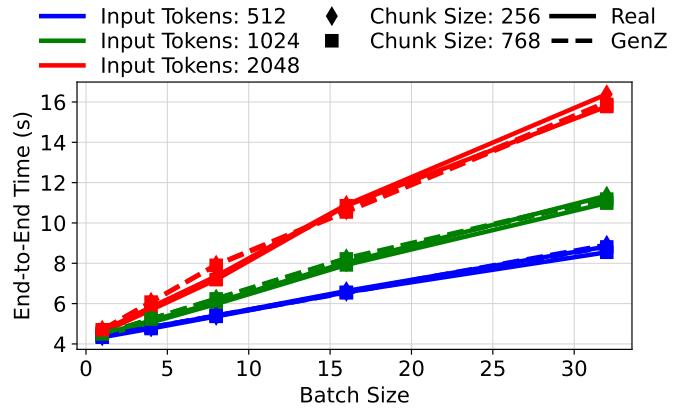


Fig. 6: Validation results comparing GenZ against vLLM inference running chunked prefill on 2xA100 (Eff=0.35). Llama2-7B with varying batch sizes, input lengths, and chunk sizes.

validation study, we report the efficiency factor for the system used.

Prefill & Decode validation: Using vLLM, we evaluate LLaMA2-7B, LLaMA2-13B, and OPT-175B across various platforms, using randomly generated dummy paragraphs as input, ranging from 500 to 2000 tokens, with each model generating a fixed 200 output tokens. Fig. 5 compares the models’ **prefill** TTFT and **decode** throughput on NVIDIA platform. The geomean error in prefill and decode predictions between real and GenZ-predicted values is 2.73% and 1.85%, respectively, across different models and platforms. The average empirically-measured efficiency factors used for different hardware configurations are V100: 0.45, A100: 0.4, 1xH100: 0.55, 2xH100: 0.64, 4xH100: 0.66, and 8xH100: 0.75.

Chunked Validation: We run chunked serving for Llama2-7B (bf16) on 2xA100 using vLLM engine varying batch sizes (1-32), input lengths (512-2048), and chunk sizes (256,768). Fig. 6 compares actual end-to-end serving times against GenZ estimates, yielding a geomean error of 1.43%.

Validation across architectures: We also validate GenZ against three other popular architectures³: (i) 8xSambanova SN40L [73], (ii) 1xAMD MI300X running vLLM [32] and (iii) 1xIntel GaudiV2 running deepspeed [34]. Fig. 7 compares the request serving time on these platforms when running LLaMA3-8B (bf16) with batch size 16, varying input/output lengths, GenZ achieves a geomean error of 5.82% across all different architectures.

Platform interconnect validation: To verify the collectives time at the platform scale, we benchmark all-reduce communication primitive with nccl-tests [74], a communication primitive performance benchmark for NVIDIA GPUs. GenZ’s collective communication times are validated with a platform size of 2 GPUs, 4 GPUs, and 8 GPUs. For collective communications,

³We were unable to get access to the physical node for these architecture, so we used the number from LLM-Inference-Bench [72]. The raw data was accessed from <https://github.com/argonne-lcf/LLM-Inference-Bench>

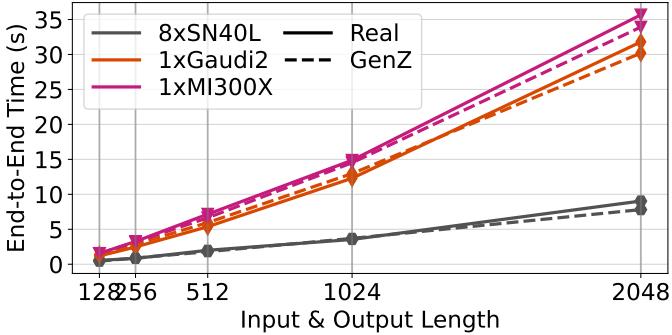


Fig. 7: Validating different architectures running Llama3-8B (bf16). SN40L uses Sambaflow framework (Eff=0.9), MI300X uses vLLM (Eff=0.25) and Gaudi2 uses deepspeed (Eff=0.6).

we observed an average link efficiency of 75% for NVLINK, which gives an effective link BW of 350 GB/s for each GPU in HGX box. We profile all model (Table II for different input and output lengths and collect their all-reduce (AR) message sizes. The message size of each AR call is very small (< 128 KB) for decode, while for prefill, per call message size is a few hundred MBs. Fig. 8 compares the real hardware latency for three different platform sizes and the corresponding latency generated by GenZ . Since the prefill and decode stages have stark differences in message size, we verify the collective time for prefill and decode independently. We found that for decode message sizes, the link latency, T_{Link} is the dominating, thus the latency seems almost constant. While prefill AR messages are large enough, that the link bandwidth, BW_{Link} , is the main contributor to collective time. Collective for all datapoints, there is a 3.89% and 2.7% geomean error for decode and prefill message sizes between real values and GenZ values.

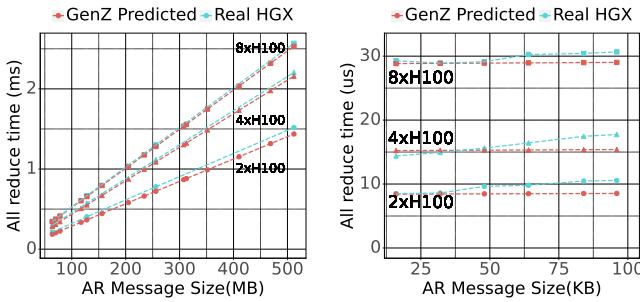


Fig. 8: Comparing All Reduce NCCL latency from GenZ against HGX:8xH100 box. Platform sizes of 2, 4, and 8 GPUs for varying message sizes.

These results confirm that **GenZ accurately captures inference trends observed on real hardware.**

IV. IMPACT OF INFERENCE OPTIMIZATIONS ON HARDWARE

LLM inference is one of the most active fields of research in recent years. This has led to a rapid rise in the number of innovations and optimizations being introduced. Table IV summarizes a few of the most popular techniques and their

Technique	Comment	Compute / Memory Impact
① Foundational model architecture change (Requires pre-training)		
MQA/GQA	Fewer KV heads	- / ↓
MoE	Sparsely activated FFNs	↓ / ↑
Sliding Window	Smaller attention window	↓ / ↓
Layer-wise KV sharing	Multiple layers share KV cache	- / ↓
② Lossless System optimization without any impact on model quality		
Flash Attention	Reduced memory accesses	- / ↓
Chunking prefill	Prefill Split + Decode	↑ / ↓
Parallelism	Distributed inference	- / ↓
Speculative Decoding	Draft model predicts tokens	↓ / ↓
③ Lossy Model optimization with impact on model quality		
Quantization	Reduced bit widths	↓ / ↓
Weight Sparsity	Removing weights	- / ↓
KV pruning	Removing KV cache tokens	↓ / ↓
Mixed precision	Different bit width for storage and computation	↓ / ↓

TABLE IV: Various techniques for optimizing LLMs and their impact on compute and memory requirements.

impact on compute and memory requirements from the AI inference platform. These fall into broadly 3 buckets, i.e., **①** Model architecture change, **②** System and algorithmic optimizations which don't change the model quality, and finally **③** Algorithmic optimization with model quality changes.

GenZ supports almost all of the techniques shown in Table IV, with being the only framework that supports modeling MoEs, mamba, and hybrid models, at the same time supporting sliding window attention, speculative decoding, weight sparsity, KV pruning, and mixed precision computation and storage.

In this section, we use GenZ to model the impact of three optimization techniques and provide insights to build next-generation AI platforms for running with those techniques.

A. Chunked Prefill

Chunked prefill [35] or *chunking* [53], [54] or *SplitFuse* [34] combines the compute-bound prefill and memory-bound decode stages of LLM generation to provide better throughput. All outstanding decode batches are processed parallelly in the chunk. Additional tokens are padded by outstanding prefill requests' tokens to construct chunks of fixed size. This ensures that each forward pass always has a fixed number of tokens. Since the number of tokens in the forward pass is fixed, the runtime of most layers is always fixed.

To understand the effect of chunking, we run two models, i.e., GPT-3 and LLama-3.1-405B, with tensor parallelism of 4 on GB200-like NPU. With $\tau_p = 4096$, $\tau_d = 1024$. We vary the decode batch size from 1 to 128 and the chunk size from 256 to 2048. Fig. 9 shows the runtime breakdown of this study. GPT-3 is unable to fit larger batch sizes as the model has dense architecture. LLama-405B, even with a larger model size, fits a much higher batch size as it uses GQA architecture. For a given chunk size, we observe that the linear GEMM layers have nearly constant latency. Only the latency of logit and attend layers (Q.K' + Softmax + S.V) increases. This is due to the fact that these layers are also memory-bound irrespective of the context length and the batch size. In the GPT-3 dense model, as decoded batches accumulate, the growing KV cache (red bar components) becomes a bottleneck, thus memory bandwidth

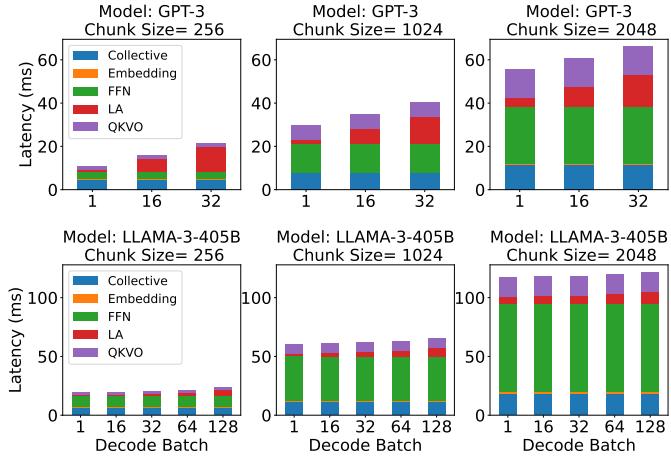


Fig. 9: Runtime breakdown of inference latency with varying chunk size and decode batches.

becomes the bottleneck for dense models. For the LLama-405B model with GQA architecture, the multi-headed attention(logit +attend) component is a very small part of the overall latency, and thus, latency remains didn't increase significantly with decode batch size.

- **Memory bottleneck for dense models:** Memory BW would remain a significant bottleneck due to larger KV caches. A larger memory size would also be required to process more decode batches in parallel.
- **Compute bottleneck for GQA models:** Memory critical layers contribute a very small portion of the total runtime. The compute-bound layers are the primary bottleneck for running models with GQA when doing chunking.

B. Speculative Decoding

Speculative decoding(SD) [63], [28], [75], [76], [77], [78] is a system level optimization technique for accelerating token generation without compromising accuracy. It uses a smaller *draft model* to generate multiple speculative token sequences in an auto-regressive fashion. These tokens serve as "guesses" for the large target model. The large target model evaluates these guesses in a single pass. It either accepts the suggested tokens if they align with its probability distribution or rejects them and adjusts the next output accordingly. On the flip side, if any token generated by the draft model is rejected by the target model, all subsequent tokens are dropped. Thus, the overall output throughput would be reduced.

We use two hyperparameters for modeling SD in GenZ : i) N = number of tokens generated by the draft model before the large full model checks them. ii) γ = probability of each token generated by the smaller model being accepted by the target model. This helps us estimate the expected tokens per pass of the target model as

$$E[T] = \sum_{i=1}^{N-1} i \cdot \gamma^i \cdot (1 - \gamma) + N \cdot \gamma^N$$

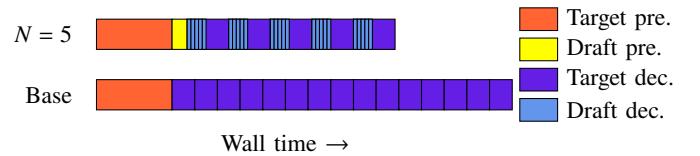


Fig. 10: Comparing baseline LLM inference against inference using speculative decode execution with a draft model and a number of parallel decode tokens, $N = 5$.

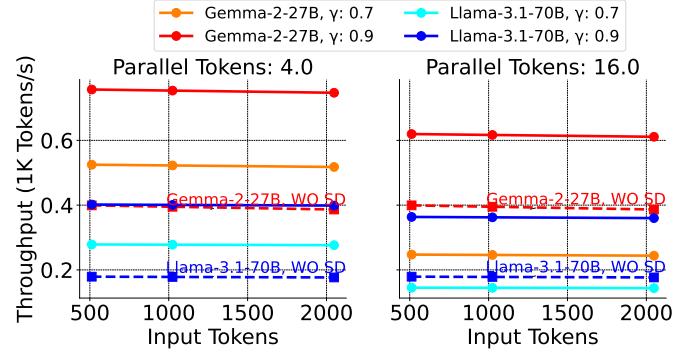


Fig. 11: Decoding Throughput with speculative decoding.

Fig. 11 shows decode throughput on GB200-like NPU with TP=2. We test with $N \in \{4, 16\}$ & $\gamma \in \{0.7, 0.9\}$ for Llama-3.1-70B (draft model: Llama-3.1-8B) and Gemma-2-27B (draft model: Gemma-2-2B). We also vary the $\tau_p, \tau_d \in \{512, 1024, 2048\}$. The dashed lines represent the model throughput without SD. ① We see that as the number of parallel tokens, N , increases, the throughput goes down. This is because of the increased cost of running the draft model. For $\gamma = 0.7$ & $N=16$, both the models perform worse than they would without SD. ② For a given number of parallel decode tokens, i.e., fixed N , γ is directly linked to the throughput gains. We see that for $N = 4$, $\gamma = 0.5$ has roughly the same throughput as the model w/o SD.

The draft models, Gemma-2-2B and Llama-3.1-8B, require 10.8% and 9.6% extra memory for weights and 40% and 28% extra memory for KV cache. For a batch of 4 requests with input/output length 32K, the total additional memory requirements would be 24.7% and 28.2%, respectively.

- **Larger memory capacity:** Keeping 2 models on-device with their corresponding KV cache requires HW with larger memory capacity compared to running a single model.
- **Compute bottleneck:** With multiple parallel tokens being fed to the target model, most operators can be pushed to the compute-bound region. This means that more layers are compute-bound than memory-bound.

C. Optimal Parallelization Strategies for MoEs

While tensor parallelism is generally known to be the best parallelism type for dense LLMs during inference [72], it is still unclear which parallelism technique would work well with MoE models. Using GenZ, we explore different parallelism strategies for a popular MoE, Mixtral-8x22B, on an H100x8 node connected by a switch network shown in Fig. 12. We assume that tokens are distributed among the experts in a balanced fashion for prefill.⁴ However, the small number of tokens makes it very unpredictable during the decode. Thus, TPOT of Mixtral 8x22B on 4 H100 with expert parallelism can vary between 3.23 ms (All tokens distributed equally) and 11.33 ms (All tokens going to a single expert) for batch 32. Although different scenarios and assumptions could result in choosing different parallelism as optimal, we believe our tool, GenZ can be used to find optimal parallelism for future MoEs on any HW platforms.

- EP is preferred when all experts activated:**

For prefill and chunked stages, *load balanced* expert activation, EP is the best parallelism strategy. In case there is an imbalance among experts, EP could perform significantly worse.

- Mix of TP and EP is preferred when partially activated experts:** For the decode stage, where only a subset of experts are activated with very few tokens being routed to each expert, TP only or TP + EP is generally superior for throughput.

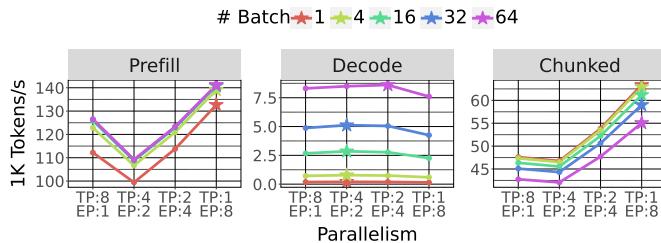


Fig. 12: Comparing different parallelism strategies for Mixtral-8x22B model inference on HGX:H00x8. $S_b = 4$, $\tau_p = 4k$, $\tau_d = 256$, $Chunk = 512$.

V. IMPACT OF MODEL ARCHITECTURES ON HW SCALING

LLM architecture plays a pivotal role in determining their computational efficiency, scalability, and inference behavior. Model architectures are constantly evolving to optimize for specific challenges, such as memory usage, computational cost, and performance across diverse tasks. We compare the four most prominent LLM architectures, covering all SOTA open-source released models.

Traditional Transformers (Dense): Original foundational models like Transformer [44], GPT, and BERT have a fully

⁴Exploring the effect of load imbalance among experts is left as future work.

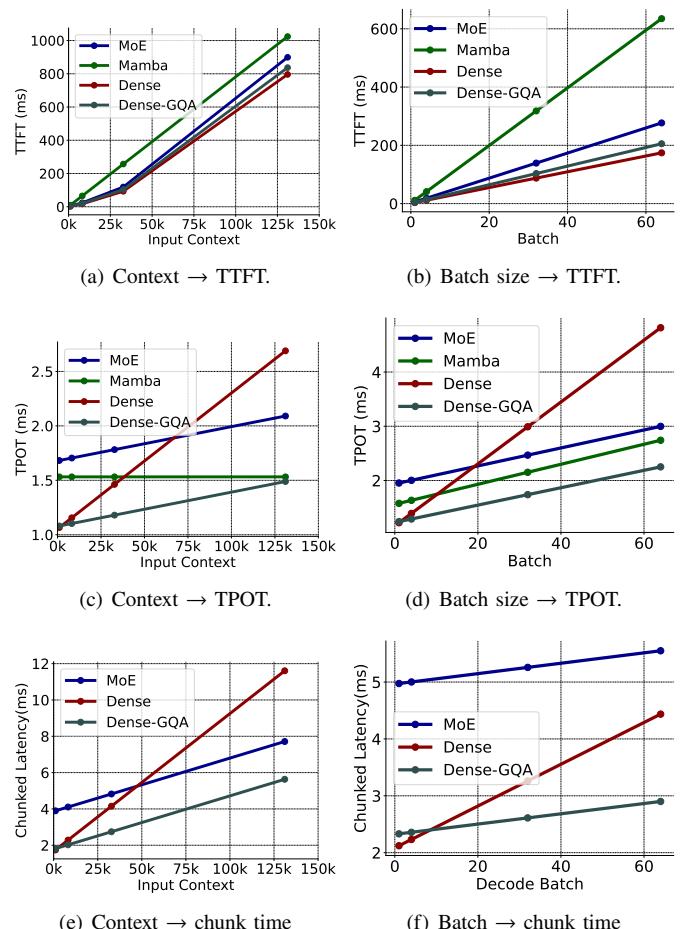


Fig. 13: Effects of context length and batch size on different model architectures during different stages.

connected attention mechanism where every token attends to every other token. This architecture have quadratically scaling compute and memory with input sequence length.

Dense Transformers with Group-query Attention: Group-query attention (GQA) [79] mitigates rising memory costs by sharing key-value caches across heads. This optimizes attention sparsity while maintaining accuracy, improving efficiency for long-context tasks.

Mixture of Experts (MoE): MoEs leverage sparsity by activating only a subset of "expert" sub-networks for each token.

Mamba: The Mamba architecture combines attention mechanisms with flavor of RNNs. Mamba focuses on optimizing memory and compute utilization, making it particularly advantageous for large-scale deployments.

To understand the impact of these model architectures in the various stages of LLM inference, we compare a model of each type of comparable size. We pick LLaMA2-7B [80], LLaMA-3.1-8B [52], Mixtral-8x7B (12.8 Active) [46], and Falcon-Mamba-7B [81] for our comparison. We study the impact of increasing context length & batch size on the latency

of stages.

1 Impact on prefill stage: As the context grows (Fig. 13(a)), All models exhibit linear scaling, for mamba model even though cache size is constant, they still need to have initial scan step linearly. With custom implementation of scan kernels, growth could be made sub-linear [58]. For growing batch sizes (Fig. 13(b)), all architectures show a linear increase in latency. Dense, Dense-GQA, and MoE scales maintain more efficient scaling. We don't see any particular benefit in the Dense-GQA since the model is mainly compute-bounded, and having fewer KV heads doesn't have any effect on the runtime.

2 Impact on decode stage: For increasing context lengths (Fig. 13(c)), Mamba's runtime doesn't change since the generation time is context length independent. Dense sees a significant rise as context length increases due to the quadratic cost of dense attention. The effect on dense-GQA and MoE is mitigated since the KV cache growth factor is much smaller. Growing batch size (Fig. 13(d)), Dense-GQA, mamba, and MoE grows almost linearly, which shows batching can help in increasing the throughput. For the dense model, the growth is linear, but the slope is higher due to the larger size of the KV cache.

3 Impact on chunked stage: In chunked prefill, a chunk of 512 tokens is constructed with multiple decode batches. Rest of the tokens are taken as a small chunk from the prefill request. Increasing context lengths for the decode batches,(Fig. 13 (e)), similar to the decode stage, larger context length equates to larger KV caches, and thus latency increases linearly. For batch sizes scaling (Fig. 13 (f)), Dense-GQA and MoE have a low growth rate due to fewer KV heads leading to smaller cache size. An interesting observation is that the MoE model has a larger latency compared to the dense model since the prefill portion of the chunk will ensure all experts are activated and thus would lead to higher latency.

VI. PLATFORM REQUIREMENTS ESTIMATION

In this section, we answer the question that **given a LLM use case, what should be the platform configuration to meet the SLO requirements?** Prefill and decode phase presents its own set of unique platform requirements. The key platform requirements terms are computation operations (PetaFLOPs), memory bandwidth (TB/s), and memory capacity (GBs). These metrics are crucial for understanding the hardware resources needed to run LLM models on various workloads efficiently. These requirements are dictated by *workload*. Our aim is to quantify these requirements and provide analytical equations to scale the requirements. We study each of the three requirements in isolation by assuming the rest of the components are not the bottleneck for the use case and model.

A. Platform Memory Capacity Requirement

For LLM inference on the platform, there should be enough memory capacity to store complete model parameters + KV cache in the fast memory of NPUs. Where KV cache = $2 * B * (\tau_p + S_b * \tau_d) * H_{kv} * D / H * N_{layers}$.

Figure 14 illustrates the distribution of memory requirements across various models and usage scenarios. For LLaMA2-7B, LLaMA3-70B, and GPT3-175B, all model parameters are utilized in each inference iteration, whereas in Mixtral-8x7B and GPT4-1.8T, only 27% and 15% of the total model parameters are activated per inference cycle.

As model sizes increase, the ratio of KV cache parameters to active weights diminishes progressively. Specifically, the ratio of the largest KV cache size (Code Gen) to active weights is 82%, 11%, 20%, 27%, and 2.8% for LLaMA2-7B, Mixtral-8x7B, LLaMA2-70B, GPT3-175B, and GPT4-1.8T, respectively. Moreover, MoE models exhibit significantly smaller KV caches compared to dense LLMs. Additionally, it is noteworthy that the KV cache expands linearly with the batch size. Furthermore, Mixtral 8x7B and LLaMA3-70B employ GQA to minimize the KV cache footprint, thus enhancing batch size capabilities.

Key Takeaways:

- Fixed-usecase, $\text{MEM-CAP}_{Req} \propto O(\text{ModelSize} + \text{KVcache})$.
- Fixed-model, $\text{MEM-CAP}_{Req} \propto O(B * (\tau_p + S_b * \tau_d))$.

B. Platform Compute Requirement

Given that the prefill stage is predominantly compute-bound, the platform prerequisites for TFLOPs are determined by prefill stage across all scenarios. Fig. 15(a) shows the platform-level compute TFLOPs required to meet the requirements in Table III for various models.

The compute TFLOPS is contingent upon both the model's dimensions and the quantity of input tokens. In cases where there are lenient expectations regarding Time to First Token (TTFT), the required TFLOPS also decreases. When using RAG for question answering, the increased prompt size causes the TFLOPS requirement to go up by 5.41x across all models.

Key Takeaways:

- Fixed-usecase, $\text{TFLOPS}_{Req} \propto O(\frac{\text{ModelSize} + \text{KVcache}}{\text{TTFT}})$.
- Fixed-model, $\text{TFLOPS}_{Req} \propto O(\frac{B * \tau_p}{\text{TTFT}})$.

C. Platform Memory Bandwidth Requirement

The memory bandwidth required to satisfy TPOT constraints dictates the platform requirements. Fig. 15(b) shows the platform level memory BW required to meet the requirements for various workloads. We assume the LLM inference with model weights and KV cache in FP8 format. Changing the dataformat would proportionally scale up or down the bandwidth requirements. For GPT4, the memory bandwidth going from QA to RAG based QA only increased the requirement by 8% even with context length becoming 10x. This is owing to the large size of the model itself.

Key Takeaways:

- Fixed-usecase, $\text{BW}_{Req} \propto O(\frac{\text{ActiveModel} + \text{KVcache}}{\text{TPOT}})$.
- Fixed-model, $\text{BW}_{Req} \propto O(\frac{B * (\tau_p + S_b * \tau_d)}{\text{TPOT}})$.

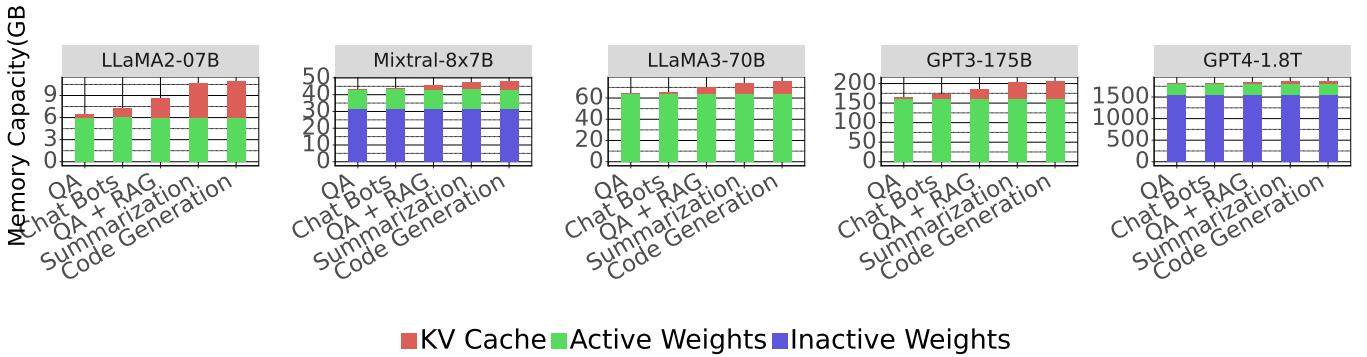
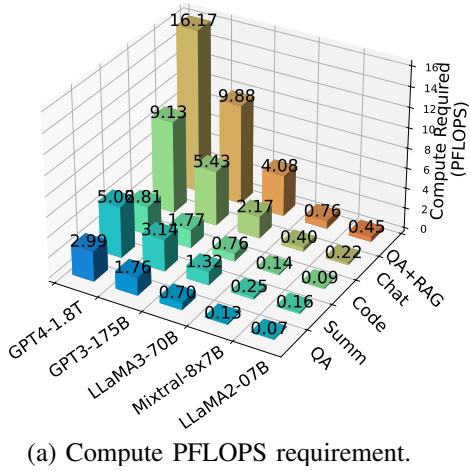
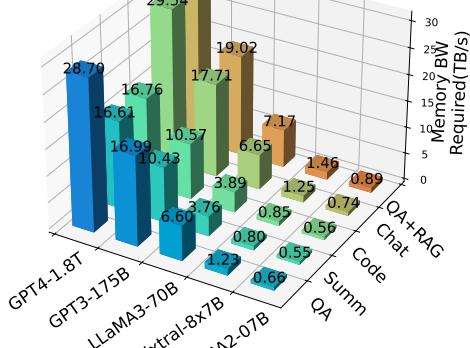


Fig. 14: Memory Capacity (GB) required for various models on different use cases during the decode stage.



(a) Compute PFLOPS requirement.



(b) Memory Bandwidth(TB/s) requirement.

Fig. 15: Platform Scale requirements.

VII. STUDIES ON FUTURE AI INFERENCE PLATFORM DESIGN

In this section, we demonstrate the usefulness of GenZ in generating insights for future AI inference platform design.

A. Case Study I: Scaling HW Characteristics

We study how improving different HW characteristics impacts the latency of different stages. For all our experiments, we assume a hypothetical Dense-GQA-5T parameter model defined in Table II. We explore four key hardware characteristics: TFLOPS, Memory BW , ICN link bandwidth, ICN link latency. To understand the effect of each characteristic on LLM inference performance, we vary each parameter in an isolated fashion. We vary the context length $\in \{1k, 32k\}$, and for running with chunking; we vary the chunk size $\in \{384, 1536\}$ and batch size $\in \{1, 256\}$. Table V summarizes this case study's findings and Fig. 16 quantifies the observed trends.

1) TFLOPS Scaling: We vary the platform TFLOPS to increase the compute-to-memory BW ratio(C:M ratio). A higher C:M ratio benefits the operators with large arithmetic intensity due to additional compute units. The prefill stage, especially with long context, gets a very good reduction in latency as C:M increases. For smaller context, the improvement stops after C:M reaches 2000. The decode doesn't improve as expected due to all layers being memory-bound. For chunking, the larger chunk sizes with fewer decode batches has the highest improvement with an increase in the C:M ratio. With more decode batches, or the smaller chunk size, there is only limited gain from the TFLOPs increase.

2) Memory Bandwidth Scaling: Next, we increase the memory bw of each NPU in the AI platform, thus reducing the C:M ratio. The prefill stage has no benefit from memory BW boost since it is completely compute-bound. The decode stage latency drops proportionally to memory BW increase since the decode stage is traditionally memory-bounded. For the chunking, the primary benefit is for scenarios where decode batches have accumulated and may constitute a significant portion of the overall runtime. For all other cases, there is no improvement in the chunk processing latency due to memory bandwidth improvement.

3) ICN Bandwidth Scaling: Our studies were done with a 32-NPU AI platform. Thus, communication latency composes a significant portion of the total latency. To further reduce the communication latency component, we scale the ICN BW. We see that the prefill stage benefits tremendously from bandwidth

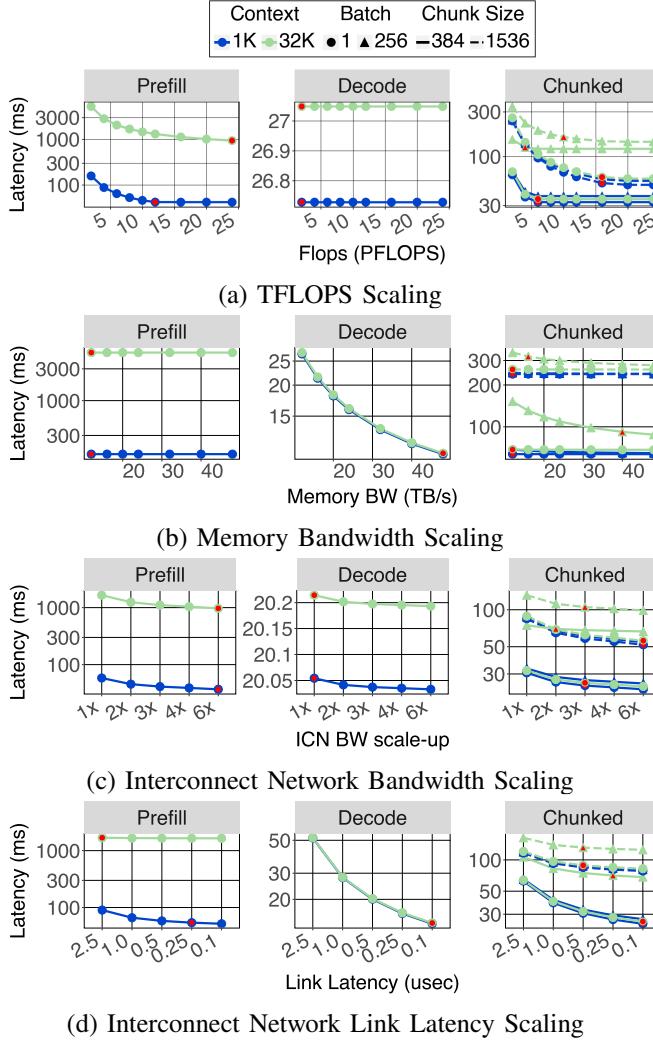


Fig. 16: Impact of scaling individual HW characteristics on runtime of different stages. The red points in the plot represent the optimal points for the stage and workload. The fixed NPU parameters are FLOPs=2PFLOPs, Memory=360 GB @ 12 TB/s and ICN link with 500 us link latency and 1.8 TB/s bandwidth.

scale-up since the large message sizes in the prefill are primarily ICN bandwidth bound. Decode generally has much smaller message sizes, $O(\approx 50\text{-}100 \text{ kB})$; thus, bandwidth scale-up doesn't improve its performance. With chunking, the message sizes are proportional to the chunk sizes. Thus, cases with large chunk-size benefit the most from the ICN BW increase. With chunk size, the benefit is limited since the collective might not be as significant a portion as other layers.

4) *ICN Link Latency Scaling*: Finally, we study the impact of platform interconnect network link latency; we reduce the T_{link} from 2.5 us to 0.1 us. For prefill, the communication component in a large context is smaller, and thus, reducing link latency does not significantly impact the run-time but is helpful for smaller context workloads. In the decoding process,

link latency constitutes the majority of the total time involved. Therefore, a significant reduction in link latency leads to a notable decrease in decode latency. For chunking, reducing link latency has a more pronounced effect on smaller chunk sizes, while its impact on larger chunk sizes is minimal.

B. Case Study II: Comparing Diverse Platforms

LLM inference throughput is heavily correlated to the characteristics of the AI platform used to serve LLMs. How to build next-generation LLMs is an open research question. Even commercially, industrial giants have hedged their bets on different platform architectures. We can categorize these architectural choices into four key buckets:

- (1) **Multiple GPUs**: Traditional general-purpose SIMD or dataflow machines connected with a memory cache on-chip and connected to large memory banks. Examples of these are GPUs [86], [87], [88], [89], [90], TPUs [91], [92], and other AI accelerators [93], [94], [95], [96].
- (2) **Wafer-scale chips** with uber-fast on-wafer interconnect connecting cores and having very large on-chip SRAM, connected to large off-chip memory [83].
- (3) **Multiple SRAM chips**: Cluster of small chipset-based accelerators with large on-chip SRAM without any back-up memory. [84], [97].
- (4) **Transformer-specific ASICs** with a very large number of compute cores with a small memory cache on-chip and connected to large memory banks [39].

Using GenZ⁵, we compare four representative platform architectures defined in Table VI running various workloads for current models (8B, 70B, 405B) and future model architectures (5T, 10T). Since the size and architecture of these platforms are completely different, there are different costs associated with each system. As we can't estimate the cost of all components, we use energy consumed as a proxy and Tokens/kWH as the comparison metric. We calculate the energy used in running workloads on different platforms. The energy consumption of each platform is modeled as a linear function of the utilization of its individual components [98]. We consider four main power components: Static/Idle, Compute, Memory, and Network. For each operator, the total energy is:

$$E_{op} = T_{op} \times (P_{static} + P_C \cdot U_C + P_{mem} \cdot U_{mem} + P_{icn} \cdot U_{icn}) \quad (2)$$

where E_{op}/T_{op} are the operator energy/execution time, P_{static} is the static power, and P_C, P_{mem}, P_{icn} represent the peak power consumption of the compute, memory and network components, respectively. The terms U_C, U_{mem}, U_{icn} denote their corresponding utilization factors for given operator. We use $P_{static} : P_C : P_{mem} : P_{icn} :: 3 : 4 : 2 : 1$ ⁵.

Fig. 17 compares the normalized throughput and normalized throughput/energy of four platform architectures across various workloads and stages of LLM inference. We run all workloads with batch size 4 and $\tau_d = 1024$. For the chunked stage, we use

⁵Future studies can use more fine-grained energy modeling simulators such as Accelergy [99], AccelWatch [98].

Characteristic	Prefill Stage	Decode Stage	Chunked-Prefill
TFLOPS	↑ Large (long context) ↑ Small (short context)	✗ (Memory-bound)	↑ Large (large chunks, fewer batches) ↑ Small (small chunks, more batches)
Memory BW	✗ (Compute-bound)	↑ Proportional	↑ Only when decode accumulates ✗ (otherwise)
ICN BW	↑ Large (ICN-bound large messages)	✗ (Small messages: 50-100kB)	↑ Large chunks ↑ Small (Small chunks)
ICN Link Latency	↑ Small (short context) ✗ (large context)	↑ Significant	↑ Small chunks ↑ Small (Large chunks)

TABLE V: Improvement in LLM Inference at different stages as we scale different platform characteristics.

Configuration	Platform Inspiration	Compute/node PFLOPS	Memory per node (SRAM/HBM)	Network Scale-up Scale-out	Peak Platform Power(kW)
Multiple GPUs	Nvidia-GB200 [82]	4.5	128MB@40 TB/s 192GB@8 TB/s	Switch{8}@900GB/s Switch{4}@900GB/s	57.2 [†]
Single SRAM wafer	Cerebras-CS3 [83]	125	44GB@21 PB/s 12TB@14.6 TB/s	On-Wafer@214 PB/s -	23
Multiple SRAM chips	Groq-GroqChip [84]	0.75	256MB@80 TB/s	FC{64}@3.2TB/s Ring{16}@256GB/s	276.8 [★]
Multiple ASICs	Etched-Soho [39]	45	256MB@80 TB/s 192GB@8 TB/s	Switch{8}@900GB/s Switch{4}@900GB/s	96 [‡]

TABLE VI: Platform architecture designs for comparison. Each of our platform’s architectures is inspired by a current system architecture. [†] Power of 4 x DGX B200 platform(8xB200 GPU) [82]. [‡] Assumed power of a larger ASIC platform (NPUs have 10x flops of B200 GPU). [★]Power of 16 GroqRack[85]. The architectures in the table are mapped to GenZ parameters defined in Section III-B, Section III-C. Column 3 is *FLOPS*, col 4 has BW_{mem} , Cap_{mem} , BW_{sram} , Cap_{sram} , col 5 has scaling dimension along with BW_{link} for each network level.

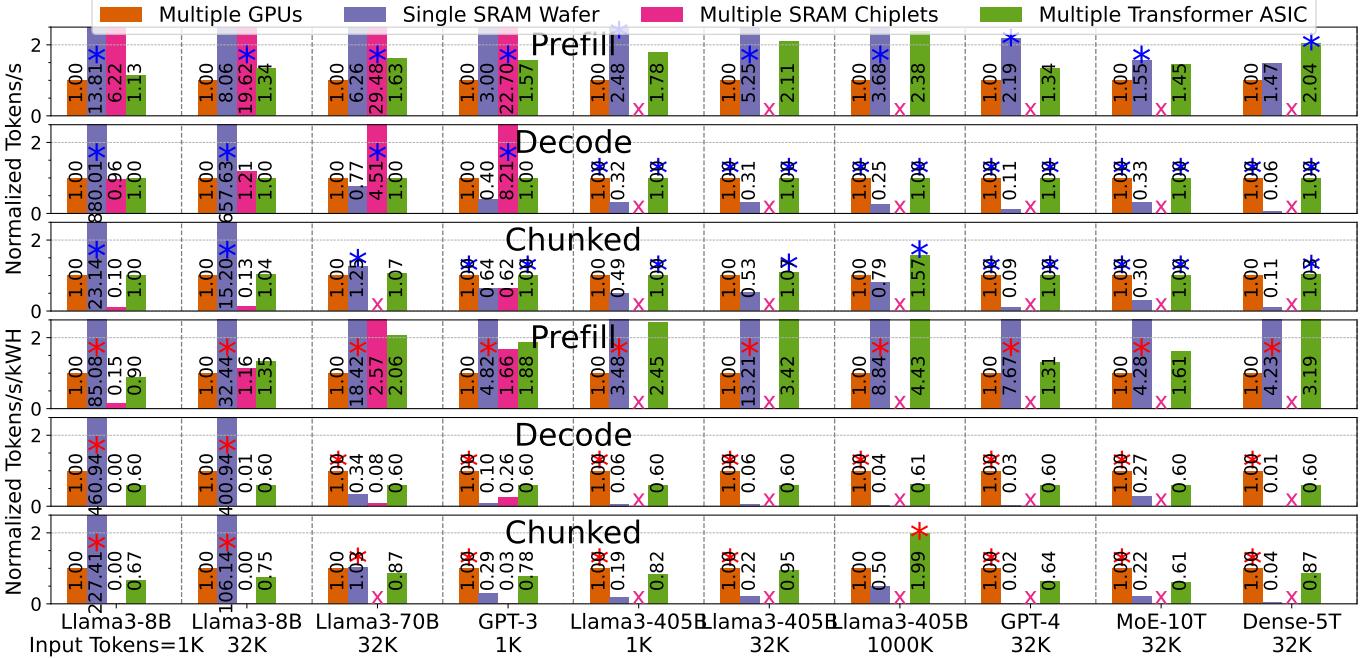


Fig. 17: Comparing normalized throughput and throughput/energy of different platform architectures across various workloads. ‘X’ represents that the architecture is out of memory when running that workload. $*/\star$ represents the platform architecture with the best performance. We run all workloads with batch size 4, $\tau_d = 1024$, and chunk size 512.

a chunk size of 512. For LLama3 & GPT-3, we use TP=8 for GPUs and ASIC, TP=64, and PP=16 for SRAM chipsets. The use case indicates the model that was running and the input context size. For GPT-4, we use TP=32 for GPUs and ASIC. A summary of their performance is as follows:

- 1 GPUs:** Excel in most decode and chunked workloads when the model cannot fit into SRAM, benefiting from high aggregate memory bandwidth.

- 2 Single SRAM Wafer:** Leads in prefill workloads across most use cases due to superior energy efficiency. Performs best in decode and chunked stages when the entire model and weights fit within SRAM.
- 3 SRAM Chiplets:** Optimal when model fits on chips but are consistently outperformed by other architectures in perf/energy, primarily due to their high power consumption owing to their very large platform size O(100s chips).
- 4 Transformer ASICs:** Thrive in high compute demands, especially for future larger models/large context lengths.

- **Choosing platform architecture for Performance:**

SRAM wafer/SRAM chips provide the best performance *when the model fits on SRAM* due to superior on-chip memory BW. ASIC is best in the prefill stage for very large models. In decode and most chunked workloads, ASIC and GPU give similar performance due to similar memory bandwidth.

- **Choosing platform architecture for Perf/energy:**

SRAM Wafer is best for prefill stage and decode/chunked when the entire model fits on SRAM as lower energy used for running a single chip compared to multiple racks of NPUs. GPUs are best for running the rest of the decode and chunked workloads due to lower energy consumption accorded to denser ASIC chip. If the ASIC chip can run with similar or lower power than GPU, it would be the best choice for achieving highest performance/kW in future larger models.

C. Case Study III: Exploring HBD Design Choices

As model sizes continue to scale, the minimum number of NPUs required to meet stringent Service Level Objectives (SLOs) has grown steadily. For instance, running GPT4, demands 64 H100 GPUs. Looking ahead, this baseline is poised to rise further, necessitating careful planning not just for NPU hardware but also for the accompanying network architecture—a challenge in its own right.

The concept of a high-bandwidth domain (HBD), defined as a group of NPUs interconnected via high-bandwidth scale-up links, plays a pivotal role here. Nvidia has progressively expanded the size of HBDs, scaling from 8 NPUs in the DGX H100 system to an impressive 72 NPUs in the GB200 NVL72. This case study delves into determining the optimal HBD size and designing effective interconnections between HBDs. To this end, we explore and compare various network architectures

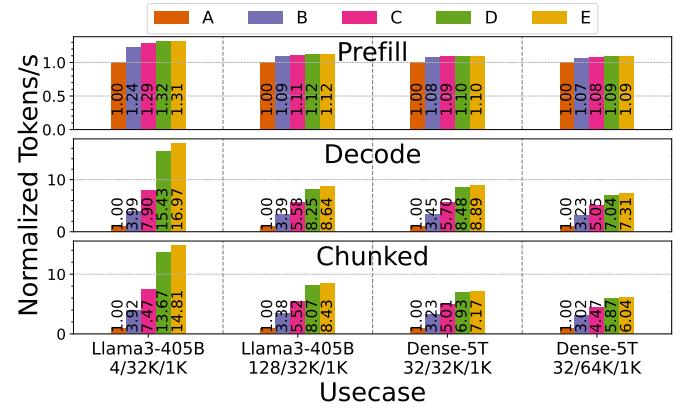


Fig. 18: Comparing throughput for different network config.

across a 256-NPU setup. We use the same individual NPU with 9 PFlops compute and 256 GB HBM, providing 13.5 TB/s for all configurations. Table VII shows the bandwidth and link latency of different interconnect types that we consider for building the platforms. We keep the network topology fixed as 2 levels of switch followed by a ring for the third dimension. Using these, we build five different network architectures shown in Table VIII. We ran models with TP=64 and PP=4.

Fig. 18 shows the throughput of different network configurations across running different workloads on 256 NPUs. Config D with all NPUs connected to a single HBD has the highest throughput but would also be the most costly to build. In contrast, Config B, with 64 NPUs per HBD, gives a similar throughput for the prefill stage at a much lower cost. Config E, with **64 NPUs per HBD connected via optical links as scale-out interconnect**, achieves throughput that is comparable to config D at a lower cost for all stages.

	High BW (SL)	InfiniBand (IB)	Optical
Latency (ns)	500	10000	200
BW (GB/s)	1800	256	900

TABLE VII: Link latency and bandwidth for different interconnects. High bandwidth(SL) is a scale-up link similar to NVlink, Ualink, etc. [100], [101], [102], [90], [103], [104], [105], [106], [107].

Config	NPU Counts	ICN Type	HBD Size
A	8, 8, 4	SL, IB, IB	8
B	8, 8, 4	SL, SL, IB	64
C	8, 16, 2	SL, SL, IB	128
D	8, 8, 4	SL, SL, SL	256
E	8, 8, 4	SL, SL, Optical	64

TABLE VIII: Comparison of different network configurations

D. Case Study IV: Exploring Different NPU Microarchitectures and Offloading Choices

We compare systems with identical platform architectures but differing NPU microarchitectures, using SCALE-sim. The NPUs employ a systolic array with weight-stationary dataflow

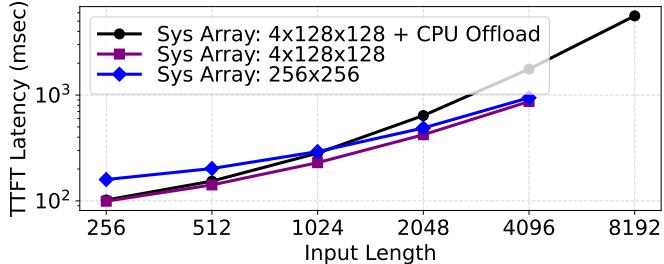


Fig. 19: Comparing different micro-architectures choices and compute offloading running LLaMA-3-8B prefill stage.

and spatial mapping. Keeping the total MAC units constant, we evaluate three configurations: (A) A single 256×256 systolic core. (B) Four 128×128 cores. (C) Four 128×128 cores with CPU offloading for MHA (Logit + Softmax + Attend) and KV cache storage. CPU has 8 TOPS and GPU to CPU link of 128 GB/s using PCIe. All NPUs are connected to a single 16GB HBM3e stack operating at 1.2 TB/s. Fig. 19 compares the prefill latency of these systems running LLaMA 3-8B (BF16) across varying input context sizes. System B achieves the lowest latency due to finer-grained kernel scheduling. System C, despite performance degradation from CPU offloading as the KV cache grows, can handle longer sequences, unlike Systems A and B, which are limited by fixed memory size. This analysis highlights GenZ’s capability to model diverse microarchitectures and offload compute.

E. Extreme Scale Requirements: AI assistant

Examining the trajectory of model scaling over the past couple of years suggests an ongoing trend of increasing model size[11]. Moreover, there has been a steady rise in the maximum context lengths of large language models (LLMs).[108]. For instance, the GPT-4-Prompts dataset, comprising multi-turn conversational prompts, already features prompts of up to 900k tokens.[109]. Recently introduced, Google Gemini can accommodate prompts of up to 1M tokens in production[2]. In this section, we delineate the platform requirements for serving these forthcoming LLMs with extensive context lengths and juxtapose them with the current state-of-the-art standards.

We envision an enormous 10T parameter Super-LLM model as the futuristic model from Table II. Our aim is to employ the Super-LLM as a standard AI assistant capable of engaging in **real-time conversations with humans**, furnishing answers on diverse topics, and retaining recollections of past interactions. Hence, supporting large context windows is imperative for AI assistants. This workload can be characterized as $S_b = 4$, $\tau_p = \text{Variable}$, $\tau_d = 2000$. Given its role as a personal assistant, we would operate it with a batch size of 1. For seamless conversation, we assume it can generate output at the rate at which humans read or listen, which amounts to 300 words per minute[110].

For real-time conversations, the KV cache would grow linearly with context, leading to higher memory capacity and bandwidth requirements. Fig. 20 shows the memory bandwidth and capacity requirements.

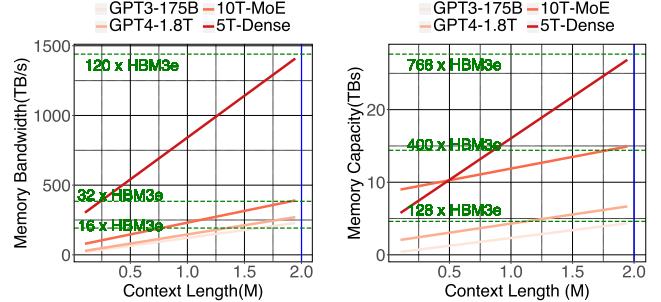


Fig. 20: Platform Scale requirements supporting a real-time conversational AI personal assistant.

and capacity required for using the super LLM as context lengths scale to 2M tokens. To gauge its feasibility, we compare it against the current SOTA memory, HBM3e, with 1.2TB/s BW and 36 GB memory capacity per stack. We require 40 TB/s memory bandwidth to make a super-LLM AI assistant, which equates to roughly 32 HBM3e stacks. On the other hand, it would require around 15 TB of memory capacity, equating to 400 HBM3e stacks.

Key Takeaway:

- The platform memory capacity seems to be a more intensive bottleneck than the memory bandwidth.
- Memory BW is within a reasonable range due to the sparse activation of the model. The growth of memory capacity requirement seems unsustainable.

VIII. RELATED WORKS

LLM inference serving and analysis: We are seeing a massive uprising of works related to LLM inference serving. There are works on optimizing the batching [36], [34], [35], memory optimization [33], [70] and scheduling [111], [29]. Various articles [112], [113], [114], [115], [116], [117], [118] provides metrics, analysis, insights, and best practices for LLM inference performance on current hardware systems. Various works provided a survey [13], [119], [120], [121], [122] of transformer inference and various optimizations in existing transformer architecture on current hardware systems.

Tools for AI Platform Modeling: Table I highlights key differences between GenZ and other performance models for LLMs. Simulators like ASTRA-sim [12], MadMax [123] and vTrain [124] focus on communication optimizations for distributed *training* and do not model different LLM architectures or LLM model optimizations on a distributed inference. Tools like LLM-viewer [13] provide ideal roofline estimation. Vidur [15] is an inference system simulator that focuses on studying the impact of different scheduling techniques on current hardware. LLMServingSim [16] provides a framework to compare scheduling algorithms. LLM-Compass [14] does DSE to optimize and generate ASIC configuration(Systolic arrays, cache sizes) for running dense models. There is a lack of a single tool/framework in the community that can help us

study different LLM model architectures combined with the latest optimizations on distributed NPU platforms.

IX. EXTENSIONS AND FUTURE DIRECTIONS

Our work intentionally abstracts low-level microarchitectural details by encapsulating them as efficiency factors and using external tools for refined performance estimates. We also provide linear energy estimation and aggregated batching support, future works can extend these capabilities with advanced modelling (e.g. additional scheduling modules to simulate disaggregated /heterogeneous serving).

X. CONCLUSIONS

We introduce GenZ, a framework with an indispensable capability of navigating the intricate design space of LLM inference, quantifying the interplay between various model and system-level optimizations, and steering the development of future AI platforms. We also show four key studies to present a roadmap for improving next-generation AI platform characteristics and selecting the appropriate architectural paradigms for running LLM inference. The source code is available at GitHub. GenZ can also be tried out on its website without any setup on your web browser.

XI. ACKNOWLEDGMENT

This work was supported in part by CoCoSys, one of seven centers in JUMP 2.0, a Semiconductor Research Corporation (SRC) program sponsored by DARPA. We thank the anonymous reviewers for their insightful feedback, which significantly improved the quality of this work. We are especially grateful to Amir Yazdanbakhsh for his valuable discussions and feedback, which helped shape the foundation of this research. We also thank Arijit Raychoudhury for his thoughtful discussions that were instrumental in realizing the full potential of this work.

REFERENCES

- [1] Chatgpt, “Introducing chatgpt.” [Online]. Available: <https://openai.com/blog/chatgpt>
- [2] Google, “Introducing gemini: Google’s most capable ai model yet,” 2023. [Online]. Available: <https://blog.google/technology/ai/google-gemini-ai/>
- [3] Microsoft, “Github copilot · your ai pair programmer.” [Online]. Available: <https://github.com/features/copilot>
- [4] E. Roivainen, “I gave chatgpt an iq test. here’s what i discovered — scientific american.” [Online]. Available: <https://www.scientificamerican.com/article/i-gave-chatgpt-an-iq-test-heres-what-i-discovered/>
- [5] J. Kaplan, S. McCandlish, T. Henighan, T. B. Brown, B. Chess, R. Child, S. Gray, A. Radford, J. Wu, and D. Amodei, “Scaling laws for neural language models,” 2020.
- [6] E. Caballero, K. Gupta, I. Rish, and D. Krueger, “Broken neural scaling laws,” 2023.
- [7] T. Brown, B. Mann, N. Ryder, M. Subbiah, J. D. Kaplan, P. Dhariwal, A. Neelakantan, P. Shyam, G. Sastry, A. Askell *et al.*, “Language models are few-shot learners,” *Advances in neural information processing systems*, vol. 33, pp. 1877–1901, 2020.
- [8] Anthropic, “Claude.” [Online]. Available: <https://www.anthropic.com/clause>
- [9] A. Chowdhery, S. Narang, J. Devlin, M. Bosma, G. Mishra, A. Roberts, P. Barham, H. W. Chung, C. Sutton, S. Gehrmann *et al.*, “Palm: Scaling language modeling with pathways,” *arXiv preprint arXiv:2204.02311*, 2022.
- [10] J. Wei, Y. Tay, R. Bommasani, C. Raffel, B. Zoph, S. Borgeaud, D. Yogatama, M. Bosma, D. Zhou, D. Metzler, E. H. Chi, T. Hashimoto, O. Vinyals, P. Liang, J. Dean, and W. Fedus, “Emergent abilities of large language models,” 2022.
- [11] I. is beautiful, “The rise and rise of a.i. large language models (llms).” [Online]. Available: <https://informationisbeautiful.net/visualizations/the-rise-of-generative-ai-large-language-models-llms-like-chatgpt/>
- [12] S. Rashidi, S. Sridharan, S. Srinivasan, and T. Krishna, “ASTRA-SIM: Enabling sw/hw co-design exploration for distributed dl training platforms,” in *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, 2020.
- [13] Z. Yuan, Y. Shang, Y. Zhou, Z. Dong, Z. Zhou, C. Xue, B. Wu, Z. Li, Q. Gu, Y. J. Lee, Y. Yan, B. Chen, G. Sun, and K. Keutzer, “Llm inference unveiled: Survey and roofline model insights,” 2024.
- [14] H. Zhang, A. Ning, R. Prabhakar, and D. Wentzlaff, “A hardware evaluation framework for large language model inference,” *arXiv preprint arXiv:2312.03134*, 2023.
- [15] A. Agrawal, N. Kedia, J. Mohan, A. Panwar, N. Kwatra, B. Gulavani, R. Ramjee, and A. Tumanov, “Vidur: A large-scale simulation framework for llm inference,” 2024. [Online]. Available: <https://arxiv.org/abs/2405.05465>
- [16] J. Cho, M. Kim, H. Choi, G. Heo, and J. Park, “Llmservingsim: A hw/sw co-simulation infrastructure for llm inference serving at scale,” 2024. [Online]. Available: <https://arxiv.org/abs/2408.05499>
- [17] OpenAI, “Gpt-4 architecture, infrastructure, training dataset, costs, vision, moe.” [Online]. Available: <https://www.semianalysis.com/p/gpt-4-architecture-infrastructure>
- [18] “Claude 3.7 sonnet and claude code \ anthropic,” [Online; accessed 2025-04-10]. [Online]. Available: <https://www.anthropic.com/news/claude-3-7-sonnet>
- [19] X. Bi, D. Chen, G. Chen, S. Chen, D. Dai, C. Deng, H. Ding, K. Dong, Q. Du, Z. Fu *et al.*, “Deepseek llm: Scaling open-source language models with longtermism,” *arXiv preprint arXiv:2401.02954*, 2024.
- [20] “Grok-1.” [Online]. Available: <https://github.com/xai-org/grok-1>
- [21] “The llama 4 herd: The beginning of a new era of natively multimodal ai innovation,” [Online; accessed 2025-04-10]. [Online]. Available: <https://ai.meta.com/blog/llama-4-multimodal-intelligence/>
- [22] A. Gholami, S. Kim, Z. Dong, Z. Yao, M. W. Mahoney, and K. Keutzer, “A survey of quantization methods for efficient neural network inference,” in *Low-Power Computer Vision*. Chapman and Hall/CRC, 2022, pp. 291–326.
- [23] H. Kang, Q. Zhang, S. Kundu, G. Jeong, Z. Liu, T. Krishna, and T. Zhao, “Gear: An efficient kv cache compression recipe for near-lossless generative inference of llm,” 2024.
- [24] G. Xiao, J. Lin, M. Seznec, H. Wu, J. Demouth, and S. Han, “Smoothquant: Accurate and efficient post-training quantization for large language models,” *PMLR*, pp. 38 087–38 099, 2023.
- [25] E. Frantar and D. Alistarh, “Sparsegpt: Massive language models can be accurately pruned in one-shot,” in *International Conference on Machine Learning*. PMLR, 2023, pp. 10 323–10 337.
- [26] A. R. Bambhaniya, A. Yazdanbakhsh, S. Subramanian, S.-C. Kao, S. Agrawal, U. Evci, and T. Krishna, “Progressive gradient flow for robust n:m sparsity training in transformers,” 2024.
- [27] G. Jeong, P.-A. Tsai, A. R. Bambhaniya, S. W. Keckler, and T. Krishna, “Abstracting sparse dnn acceleration via structured sparse tensor decomposition,” 2024.
- [28] S. Kim, K. Mangalam, S. Moon, J. Malik, M. W. Mahoney, A. Gholami, and K. Keutzer, “Speculative decoding with big little decoder,” *Advances in Neural Information Processing Systems*, vol. 36, 2024.
- [29] Y. Fu, P. Bailis, I. Stoica, and H. Zhang, “Break the sequential dependency of llm inference using lookahead decoding,” *arXiv preprint arXiv:2402.02057*, 2024.
- [30] M. Elbayad, J. Gu, E. Grave, and M. Auli, “Depth-adaptive transformer,” *arXiv preprint arXiv:1910.10073*, 2019.
- [31] Y. Chen, X. Pan, Y. Li, B. Ding, and J. Zhou, “Ee-llm: Large-scale training and inference of early-exit large language models with 3d parallelism,” *arXiv preprint arXiv:2312.04916*, 2023.
- [32] W. Kwon, Z. Li, S. Zhuang, Y. Sheng, L. Zheng, C. H. Yu, J. E. Gonzalez, H. Zhang, and I. Stoica, “Efficient memory management for large language model serving with paggedattention,” in *Proceedings of the ACM SIGOPS 29th Symposium on Operating Systems Principles*, 2023.
- [33] T. Dao, D. Y. Fu, S. Ermon, A. Rudra, and C. Ré, “Flashattention: Fast and memory-efficient exact attention with io-awareness,” 2022.
- [34] C. Holmes, M. Tanaka, M. Wyatt, A. A. Awan, J. Rasley, S. Rajbhandari, R. Y. Aminabadi, H. Qin, A. Bakhtiari, L. Kurilenko *et al.*, “Deepspeed-fastgen: High-throughput text generation for llms via mii and deepspeed-inference,” *arXiv preprint arXiv:2401.08671*, 2024.

- [35] A. Agrawal, A. Panwar, J. Mohan, N. Kwatra, B. S. Gulavani, and R. Ramjee, "Sarathi: Efficient llm inference by piggybacking decodes with chunked prefixes," *arXiv preprint arXiv:2308.16369*, 2023.
- [36] G.-I. Yu, J. S. Jeong, G.-W. Kim, S. Kim, and B.-G. Chun, "Orca: A distributed serving system for {Transformer-Based} generative models," in *16th USENIX Symposium on Operating Systems Design and Implementation (OSDI 22)*, 2022, pp. 521–538.
- [37] NVIDIA, "Nvidia. tensorrt-llm." 2023. [Online]. Available: <https://github.com/NVIDIA/TensorRT-LLM>
- [38] "Artificial analysis - independent analysis of ai models and api providers." [Online]. Available: <https://artificialanalysis.ai/>
- [39] "Etched is making the biggest bet in ai," 2024, (Accessed on 2/21/2025). [Online]. Available: <https://www.etched.com/announcing-etched>
- [40] C. Trueman, "Photonic computing company lightmatter valued at \$4.4bn in \$400m funding round - dc'd," 10 2024, [Online; accessed 2025-04-09]. [Online]. Available: <https://www.datacenterdynamics.com/en/news/photonic-computing-company-lightmatter-achieves-44bn-valuation-from-400m-series-d-round>
- [41] A. Samajdar, J. M. Joseph, Y. Zhu, P. Whatmough, M. Mattina, and T. Krishna, "A systematic methodology for characterizing scalability of dnn accelerators using scale-sim," in *2020 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, 2020, pp. 58–68.
- [42] A. Parashar, P. Raina, Y. S. Shao, Y.-H. Chen, V. A. Ying, A. Mukkara, R. Venkatesan, B. Khailany, S. W. Keckler, and J. Emer, "Timeloop: A systematic approach to dnn accelerator evaluation," in *2019 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, 2019, pp. 304–315.
- [43] H. Kwon, P. Chatarsi, V. Sarkar, T. Krishna, M. Pellauer, and A. Parashar, "Maestro: A data-centric approach to understand reuse, performance, and hardware cost of dnn mappings," *IEEE Micro*, vol. 40, no. 3, pp. 20–29, 2020.
- [44] A. Vaswani, N. Shazeer, N. Parmar, J. Uszkoreit, L. Jones, A. N. Gomez, L. Kaiser, and I. Polosukhin, "Attention is all you need," *Advances in neural information processing systems*, vol. 30, 2017.
- [45] W. Fedus, B. Zoph, and N. Shazeer, "Switch transformers: Scaling to trillion parameter models with simple and efficient sparsity," *arXiv preprint arXiv:2101.03961*, 2021.
- [46] A. Q. Jiang, A. Sablayrolles, A. Roux, A. Mensch, B. Savary, C. Bamford, D. S. Chaplot, D. d. I. Casas, E. B. Hanna, F. Bressand et al., "Mixtral of experts," *arXiv preprint arXiv:2401.04088*, 2024.
- [47] "Mixtral-8x22b." [Online]. Available: <https://huggingface.co/mistral-community/Mixtral-8x22B-v0.1>
- [48] "Dbrx, a large language model by databricks." [Online]. Available: <https://github.com/databricks/dbrx>
- [49] J. Achiam, S. Adler, S. Agarwal, L. Ahmad, I. Akkaya, F. L. Aleman, D. Almeida, J. Alten Schmidt, S. Altman, S. Anadkat et al., "Gpt-4 technical report," *arXiv preprint arXiv:2303.08774*, 2023.
- [50] P. MCGUINNESS, "Gpt-4 architecture details." [Online]. Available: <https://patmcguinness.substack.com/p/gpt-4-details-revealed>
- [51] G. Team, M. Riviere, S. Pathak, P. G. Sessa, C. Hardin, S. Bhupatiraju, L. Huszenot, T. Mesnard, B. Shahriari, A. Ramé, J. Ferret, P. Liu, P. Tafti, A. Friesen, M. Casbon, S. Ramos, R. Kumar, C. L. Lan, S. Jerome, A. Tsitsulin, N. Vieillard, P. Stanczyk, S. Girgin, N. Momchev, M. Hoffman, S. Thakoor, J.-B. Grill, B. Neyshabur, O. Bachem, A. Walton, A. Severyn, A. Parrish, A. Ahmad, A. Hutchison, A. Abdagic, A. Carl, A. Shen, A. Brock, A. Coenen, A. Laforge, A. Paterson, B. Bastian, B. Piot, B. Wu, B. Royal, C. Chen, C. Kumar, C. Perry, C. Welty, C. A. Choquette-Choo, D. Sinopalnikov, D. Weinberger, D. Vijaykumar, D. Rogozinska, D. Herbison, E. Bandy, E. Wang, E. Noland, E. Moreira, E. Senter, E. Eltyshev, F. Visin, G. Rasskin, G. Wei, G. Cameron, G. Martins, H. Hashemi, H. Klimeczak-Plucińska, H. Batra, H. Dhand, I. Nardini, J. Mein, J. Zhou, J. Svensson, J. Stanway, J. Chan, J. P. Zhou, J. Carrasqueira, J. Iljazi, J. Becker, J. Fernandez, J. van Amersfoort, J. Gordon, J. Lipschultz, J. Newlan, J. yeong Ji, K. Mohamed, K. Badola, K. Black, K. Millican, K. McDonell, K. Nguyen, K. Sodhia, K. Greene, L. L. Sjoesund, L. Usui, L. Sifre, L. Heuermann, L. Lago, L. McNealus, L. B. Soares, L. Kilpatrick, L. Dixon, L. Martins, M. Reid, M. Singh, M. Iverson, M. Görner, M. Velloso, M. Wirth, M. Davidow, M. Miller, M. Rahtz, M. Watson, M. Risdal, M. Kazemi, M. Moynihan, M. Zhang, M. Kahng, M. Park, M. Rahman, M. Khatwani, N. Dao, N. Bardoliwalla, N. Devanathan, N. Dumai, N. Chauhan, O. Wahltinez, P. Botarda, P. Barnes, P. Barham, P. Michel, P. Jin, P. Georgiev, P. Culliton, P. Kuppala, R. Comanescu, R. Merhej, R. Jana, R. A. Rokni, R. Agarwal, R. Mullins, S. Saadat, S. M. Carthy, S. Cogan, S. Perrin, S. M. R. Arnold, S. Krause, S. Dai, S. Garg, S. Sheth, S. Ronstrom, S. Chan, T. Jordan, T. Yu, T. Eccles, T. Hennigan, T. Kociský, T. Doshi, V. Jain, V. Yadav, V. Meshram, V. Dharmadhikari, W. Barkley, W. Wei, W. Ye, W. Han, W. Kwon, X. Xu, Z. Shen, Z. Gong, Z. Wei, V. Cotruta, P. Kirk, A. Rao, M. Giang, L. Peran, T. Warkentin, E. Collins, J. Barral, Z. Ghahramani, R. Hadsell, D. Sculley, J. Banks, A. Dragan, S. Petrov, O. Vinyals, J. Dean, D. Hassabis, K. Kavukcuoglu, C. Farabet, E. Buchatskaya, S. Borgeaud, N. Fiedel, A. Joulin, K. Kenealy, R. Dadashi, and A. Andreev, "Gemma 2: Improving open language models at a practical size," 2024. [Online]. Available: <https://arxiv.org/abs/2408.00118>
- [52] "Meta llama 3." [Online]. Available: <https://github.com/meta-llama/llama3>
- [53] "Streamlining AI Inference Performance and Deployment with NVIDIA TensorRT-LLM Chunked Prefill — NVIDIA Technical Blog - funding developer.nvidia.com," <https://developer.nvidia.com/blog/streamlining-ai-inference-performance-and-deployment-with-nvidia-tensorrt-llm-chunked-prefill>, 2024, [Accessed 22-11-2024].
- [54] "Demystifying AI Inference Deployments for Trillion Parameter Large Language Models — NVIDIA Technical Blog — developer.nvidia.com," <https://developer.nvidia.com/blog/demystifying-ai-inference-deployments-for-trillion-parameter-large-language-models/>, 2024, [Accessed 22-11-2024].
- [55] H. Sun, X. Liu, Y. Gong, Y. Zhang, D. Jiang, L. Yang, and N. Duan, "Allies: Prompting large language model with beam search," in *Findings of EMNLP*, 2023.
- [56] C. W. Kim, "Guiding text generation with constrained beam search in transformers," Mar 2022. [Online]. Available: <https://huggingface.co/blog/constrained-beam-search>
- [57] M. Agarwal, A. Qureshi, N. Sardana, L. Li, J. Quevedo, and D. Khudia, "Llm inference performance engineering: Best practices," Oct 2023. [Online]. Available: <https://www.databricks.com/blog/llm-inference-performance-engineering-best-practices>
- [58] A. Gu and T. Dao, "Mamba: Linear-time sequence modeling with selective state spaces," 2024. [Online]. Available: <https://arxiv.org/abs/2312.00752>
- [59] "Huggingface generate infereface." [Online]. Available: <https://huggingface.co/docs/transformers/en/main%5Fclasses/text%5Fgeneration>
- [60] R. Dao, "Flash-decoding for long-context inference." [Online]. Available: <https://pytorch.org/blog/flash-decoding/>
- [61] S.-C. Kao, S. Subramanian, G. Agrawal, and T. Krishna, "An optimized dataflow for mitigating attention performance bottlenecks," *arXiv preprint arXiv:2107.06419*, 2021.
- [62] H. Wu, Y. Gan, F. Yuan, J. Ma, W. Zhu, Y. Xu, H. Zhu, Y. Zhu, X. Liu, and J. Gu, "Efficient llm inference solution on intel gpu," 2023.
- [63] Y. Leviathan, M. Kalman, and Y. Matias, "Fast inference from transformers via speculative decoding," 2023. [Online]. Available: <https://arxiv.org/abs/2211.17192>
- [64] A. Parashar, P. Raina, Y. S. Shao, Y.-H. Chen, V. A. Ying, A. Mukkara, R. Venkatesan, B. Khailany, S. W. Keckler, and J. Emer, "Timeloop: A systematic approach to dnn accelerator evaluation," in *2019 IEEE international symposium on performance analysis of systems and software (ISPASS)*. IEEE, 2019, pp. 304–315.
- [65] M. Shoeybi, M. Patwary, R. Puri, P. LeGresley, J. Casper, and B. Catanzaro, "Megatron-lm: Training multi-billion parameter language models using model parallelism," *arXiv preprint arXiv:1909.08053*, 2019.
- [66] Y. Huang, Y. Cheng, A. Bapna, O. Firat, M. X. Chen, D. Chen, H. Lee, J. Ngiam, Q. V. Le, Y. Wu, and Z. Chen, "Gpipe: Efficient training of giant neural networks using pipeline parallelism," 2019.
- [67] S. A. Jacobs, M. Tanaka, C. Zhang, M. Zhang, S. L. Song, S. Rajbhandari, and Y. He, "Deepspeed ulysses: System optimizations for enabling training of extreme long sequence transformer models," 2023.
- [68] S. Li, F. Xue, C. Baranwal, Y. Li, and Y. You, "Sequence parallelism: Long sequence training from system perspective," 2022.
- [69] W. Won, T. Heo, S. Rashidi, S. Sridharan, S. Srinivasan, and T. Krishna, "Astra-sim2, 0: Modeling hierarchical networks and disaggregated systems for large-model training at scale," in *2023 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*. IEEE, 2023, pp. 283–294.
- [70] W. Kwon, Z. Li, S. Zhuang, Y. Sheng, L. Zheng, C. H. Yu, J. Gonzalez, H. Zhang, and I. Stoica, "Efficient memory management for large

- language model serving with pagedattention,” in *Proceedings of the 29th Symposium on Operating Systems Principles*, ser. SOSP ’23. New York, NY, USA: Association for Computing Machinery, 2023, p. 611–626. [Online]. Available: <https://doi.org/10.1145/3600006.3613165>
- [71] “Nvidia hgx.” [Online]. Available: <https://www.nvidia.com/en-us/data-center/hgx/>
- [72] K. T. Chitty-Venkata, S. Raskar, B. Kale, F. Ferdaus, A. Tanikanti, K. Raffenetti, V. Taylor, M. Emani, and V. Vishwanath, “Llm-inference-bench: Inference benchmarking of large language models on ai accelerators,” 2024. [Online]. Available: <https://arxiv.org/abs/2411.00136>
- [73] “Sambaflow developer documentation :: Sambanova documentation,” [Online; accessed 2025-02-21]. [Online]. Available: <https://docs.sambanova.ai/developer/latest/index.html>
- [74] “Nccl tests.” [Online]. Available: <https://github.com/NVIDIA/nccl-tests/tree/master>
- [75] S. Bae, J. Ko, H. Song, and S. Yun, “Fast and robust early-exiting framework for autoregressive language models with synchronized parallel decoding,” in *Proceedings of the 2023 Conference on Empirical Methods in Natural Language Processing, EMNLP 2023, Singapore, December 6-10, 2023*, H. Bouamor, J. Pino, and K. Bali, Eds. Association for Computational Linguistics, 2023, pp. 5910–5924. [Online]. Available: <https://doi.org/10.18653/v1/2023.emnlp-main.362>
- [76] C. Hooper, S. Kim, H. Mohammadzadeh, H. Genc, K. Keutzer, A. Gholami, and S. Shao, “Speed: Speculative pipelined execution for efficient decoding,” 2024. [Online]. Available: <https://arxiv.org/abs/2310.12072>
- [77] A. Santilli, S. Severino, E. Postolache, V. Maiorca, M. Mancusi, R. Marin, and E. Rodola, “Accelerating transformer inference for translation via parallel decoding,” in *Proceedings of the 61st Annual Meeting of the Association for Computational Linguistics (Volume 1: Long Papers)*. Association for Computational Linguistics, 2023. [Online]. Available: <http://dx.doi.org/10.18653/v1/2023.acl-long.689>
- [78] H. Xia, T. Ge, P. Wang, S.-Q. Chen, F. Wei, and Z. Sui, “Speculative decoding: Exploiting speculative execution for accelerating seq2seq generation,” 2023. [Online]. Available: <https://arxiv.org/abs/2203.16487>
- [79] D. A. Hudson and C. D. Manning, “Gqa: A new dataset for real-world visual reasoning and compositional question answering,” in *Proceedings of the IEEE/CVF conference on computer vision and pattern recognition*, 2019, pp. 6700–6709.
- [80] H. Touvron, L. Martin, K. Stone, P. Albert, A. Almahairi, Y. Babaei, N. Bashlykov, S. Batra, P. Bhargava, S. Bhosale *et al.*, “Llama 2: Open foundation and fine-tuned chat models,” *arXiv preprint arXiv:2307.09288*, 2023.
- [81] J. Zuo, M. Velikanov, D. E. Rhaiem, I. Chahed, Y. Belkada, G. Kunsch, and H. Hacid, “Falcon mamba: The first competitive attention-free 7b language model,” 2024. [Online]. Available: <https://arxiv.org/abs/2410.05355>
- [82] AMAX, “Comparing nvidia blackwell configurations,” 3 2024, [Online; accessed 2025-02-18]. [Online]. Available: <https://www.amax.com/comparing-nvidia-blackwell-configurations/>
- [83] K. Rocki, D. Van Essendelft, I. Sharapov, R. Schreiber, M. Morrison, V. Kibardin, A. Portnoy, J. F. Dietiker, M. Syamlal, and M. James, “Fast stencil-code computation on a wafer-scale processor,” in *SC20: International Conference for High Performance Computing, Networking, Storage and Analysis*. IEEE, 2020, pp. 1–14.
- [84] “Groqchip.” [Online]. Available: <https://groq.com/wp-content/uploads/2022/10/GroqChip-Processor-Product-Brief-v1.5.pdf>
- [85] Groq, “Groqracktm compute cluster - product brief v1.7.” [Online]. Available: <https://groq.com/wp-content/uploads/2024/08/GroqRack%2E%84%A2-Compute-Cluster-Product-Brief-v1.7.pdf>
- [86] “NVIDIA Blackwell Platform Arrives to Power a New Era of Computing — nvidianews.nvidia.com,” <https://nvidianews.nvidia.com/news/nvidia-blackwell-platform-arrives-to-power-a-new-era-of-computing>, 2024, [Accessed 20-11-2024].
- [87] “Nvidia h100 tensor core gpu datasheet,” <https://resources.nvidia.com/en-us-tensor-core/nvidia-tensor-core-gpu-datasheet>, 2023, (Accessed on 11/22/2024).
- [88] “hpc-datasheet-sc23-h200-datasheet-3002446.pdf,” <https://nvdam.widen.net/s/nb5zzsjdf/hpc-datasheet-sc23-h200-datasheet-3002446>, 2024, (Accessed on 11/22/2024).
- [89] “Amd instinct mi300x platform.” [Online]. Available: <https://www.amd.com/en/products/accelerators/instinct/mi300.html#case-studies>
- [90] “Intel hls-gaudi2.” [Online]. Available: <https://habana.ai/wp-content/uploads/2023/10/HLS-Gaudi2%5FDatasheet%5F10%5F23.pdf>
- [91] “Google tpu pods.” [Online]. Available: <https://cloud.google.com/blog/topics/tpus/google-showcases-cloud-tpu-v4-pods-for-large-model-training>
- [92] N. P. Jouppi, , C. Young, N. Patil, D. Patterson, G. Agrawal, R. Rajwa, S. Bates, S. Bhatia, N. Boden, A. Borchers, R. Boyle, P. l. Cantin, C. Chao, C. Clark, J. Coriell, M. Daley, M. Dau, J. Dean, B. Gelb, T. V. Ghaemmaghami, R. Gottipati, W. Gulland, R. Hagmann, C. R. Ho, D. Hogberg, J. Hu, R. Hundt, D. Hurt, J. Ibarz, A. Jaffey, A. Jaworski, A. Kaplan, H. Khaitan, D. Killebrew, A. Koch, N. Kumar, S. Lacy, J. Laudon, J. Law, D. Le, C. Leary, Z. Liu, K. Lucke, A. Lundin, G. MacKean, A. Maggiore, M. Mahony, K. Miller, R. Nagarajan, R. Narayanaswami, R. Ni, K. Nix, T. Norrie, M. Omernick, N. Penukonda, A. Phelps, J. Ross, M. Ross, A. Salek, E. Samadiani, C. Severn, G. Sizikov, M. Snelham, J. Souter, D. Steinberg, A. Swing, M. Tan, G. Thorson, B. Tian, H. Toma, E. Tuttle, V. Vasudevan, R. Walter, W. Wang, E. Wilcox, and D. H. Yoon, “In-datacenter performance analysis of a tensor processing unit,” in *Proceedings of the 44th Annual International Symposium on Computer Architecture (ISCA)*, 2017.
- [93] SambaNova, “Sambanova whitepaper,” 2021. [Online]. Available: <https://sambanova.ai/wp-content/uploads/2021/06/SambaNova%5FRDA%5FWWhitepaper%5FEnglish.pdf>
- [94] “Aws graviton4 - annapurna labs (amazon) - wikichip,” https://en.wikichip.org/wiki/annapurna_labs/graviton/graviton4, 2024, (Accessed on 11/22/2024).
- [95] “Prod_brief_qcom_cloud_ai_100_ultra.pdf,” https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/Prod_Brief_QCOM_Cloud_AI_100_Ultra.pdf, 2021, (Accessed on 11/22/2024).
- [96] “Hotchips2020_ml_inference_baidu_kunlun_v5.pdf,” https://www.hc32.hotchips.org/assets/program/conference/day2/HotChips2020_ML_Inference_Baidu_Kunlun_v5.pdf, 2020, (Accessed on 11/22/2024).
- [97] H. Peng, S. Davidson, R. Shi, S. L. Song, and M. Taylor, “Chiplet cloud: Building ai supercomputers for serving large generative language models,” 2023.
- [98] V. Kandiah, S. Peverelle, M. Khairy, J. Pan, A. Manjunath, T. G. Rogers, T. M. Aamodt, and N. Hardavellas, “Accelwattch: A power modeling framework for modern gpus,” in *MICRO-54: 54th Annual IEEE/ACM International Symposium on Microarchitecture*, ser. MICRO ’21. New York, NY, USA: Association for Computing Machinery, 2021, p. 738–753. [Online]. Available: <https://doi.org/10.1145/3466752.3480063>
- [99] Y. N. Wu, J. S. Emer, and V. Sze, “Accelergy: An Architecture-Level Energy Estimation Methodology for Accelerator Designs,” in *IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, 2019.
- [100] R. Urata, H. Liu, K. Yasumura, E. Mao, J. Berger, X. Zhou, C. Lam, R. Bannon, D. Hutchinson, D. Nelson, L. Poutievski, A. Singh, J. Ong, and A. Vahdat, “Mission apollo: Landing optical circuit switching at datacenter scale,” 2022. [Online]. Available: <https://arxiv.org/abs/2208.10041>
- [101] “Optimization of collective communication operations in mpich.” [Online]. Available: <https://web.cels.anl.gov/~thakur/papers/ijhpc-coll.pdf>
- [102] “Optical interconnects set to achieve bandwidth benchmark — features — jul 2018 — photonics spectra,” https://www.photonics.com/Articles/Optical_Interconnects_Set_to_Achieve_Bandwidth/a63495, 2018, (Accessed on 11/22/2024).
- [103] “solution-overview-gtcspring24-quantum-x800-3175164.pdf,” <https://nvdam.widen.net/s/hbp8zz7fvt/solution-overview-gtcspring24-quantum-x800-3175164>, 2024, (Accessed on 11/23/2024).
- [104] “Ib_intro_wp_190.pdf,” https://network.nvidia.com/pdf/whitepapers/Ib_Intro_WP_190.pdf, 2023, (Accessed on 11/23/2024).
- [105] “Hyperion-research-special-analysis-ualink-group-created-for-accelerator-interconnect-july-2024.pdf,” <chrome-extension://efaidnbmnniibpcajpcgkclefindmkaj/> <https://hyperionresearch.com/wp-content/uploads/2024/07/Hyperion-Research-Special-Analysis-UALink-Group-Created-for-Accelerator-Interconn.pdf>, 2024, (Accessed on 11/23/2024).
- [106] M. Khani, M. Ghobadi, M. Alizadeh, Z. Zhu, M. Glick, K. Bergman, A. Vahdat, B. Klenk, and E. Ebrahimi, “Sip-ml: high-bandwidth optical network interconnects for machine learning training,” in *Proceedings*

- of the 2021 ACM SIGCOMM 2021 Conference*, ser. SIGCOMM '21. New York, NY, USA: Association for Computing Machinery, 2021, p. 657–675. [Online]. Available: <https://doi.org/10.1145/3452296.3472900>
- [107] A. Li, S. L. Song, J. Chen, J. Li, X. Liu, N. R. Tallent, and K. J. Barker, “Evaluating modern gpu interconnect: Pcie, nvlink, nv-sli, nvswitch and gpudirect,” *IEEE Transactions on Parallel and Distributed Systems*, vol. 31, no. 1, p. 94–110, Jan. 2020. [Online]. Available: <http://dx.doi.org/10.1109/TPDS.2019.2928289>
- [108] “Openai’s plans according to sam altman,” 2023. [Online]. Available: <https://web.archive.org/web/20230601163710/https://humanloop.com/blog/openai-plans>
- [109] “Multi-turn conversational prompts from chatgpt-4 (10k+ tokens).” [Online]. Available: <https://huggingface.co/datasets/erfanzar/GPT-4-Prompts>
- [110] M. Brysbaert, “How many words do we read per minute? a review and meta-analysis of reading rate,” *Journal of Memory and Language*, vol. 109, p. 104047, 2019. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0749596X19300786>
- [111] Y. Sheng, L. Zheng, B. Yuan, Z. Li, M. Ryabinin, D. Y. Fu, Z. Xie, B. Chen, C. Barrett, J. E. Gonzalez, P. Liang, C. Ré, I. Stoica, and C. Zhang, “Flexgen: High-throughput generative inference of large language models with a single gpu,” 2023.
- [112] “Llm inference performance engineering: Best practices.” [Online]. Available: <https://www.databricks.com/blog/llm-inference-performance-engineering-best-practices>
- [113] F. team, “Accelerating self-attentions for llm serving with flashinfer.” [Online]. Available: <https://flashinfer.ai/2024/02/02/introduce-flashinfer.html>
- [114] L. Chen, “Dissecting batching effects in gpt inference.” [Online]. Available: <https://le.qun.ch/en/blog/2023/05/13/transformer-batching/>
- [115] Kippy, “Transformer inference arithmetic.” [Online]. Available: <https://kippy.ly/transformer-inference-arithmetic/>
- [116] AWS, “Generative llm inference with neuron.” [Online]. Available: <https://awsdocs-neuron.readthedocs-hosted.com/en/latest/general/appnotes/transforms-neuronx/generative-llm-inference-with-neuron.html#what-batch-size-should-i-use>
- [117] V. Shenoy and P. Kiely, “A guide to llm inference and performance.” [Online]. Available: <https://www.baseten.co/blog/llm-transformer-inference-guide/>
- [118] NVIDIA, “Mastering llm techniques: Inference optimization.” [Online]. Available: <https://developer.nvidia.com/blog/mastering-llm-techniques-inference-optimization/>
- [119] S. Kim, C. Hooper, T. Wattanawong, M. Kang, R. Yan, H. Genc, G. Dinh, Q. Huang, K. Keutzer, M. W. Mahoney *et al.*, “Full stack optimization of transformer inference: a survey,” *arXiv preprint arXiv:2302.14017*, 2023.
- [120] K. T. Chitty-Venkata, S. Mittal, M. Emani, V. Vishwanath, and A. K. Soman, “A survey of techniques for optimizing transformer inference,” 2023.
- [121] S. Minaee, T. Mikolov, N. Nikzad, M. Chenaghlu, R. Socher, X. Amatriain, and J. Gao, “Large language models: A survey,” 2024. [Online]. Available: <https://arxiv.org/abs/2402.06196>
- [122] A. Fan, B. Gokkaya, M. Harman, M. Lyubarshiy, S. Sengupta, S. Yoo, and J. M. Zhang, “Large language models for software engineering: Survey and open problems,” 2023. [Online]. Available: <https://arxiv.org/abs/2310.03533>
- [123] S. Hsia, A. Golden, B. Acun, N. Ardalani, Z. DeVito, G.-Y. Wei, D. Brooks, and C.-J. Wu, “Mad-max beyond single-node: Enabling large machine learning model acceleration on distributed systems,” in *2024 ACM/IEEE 51st Annual International Symposium on Computer Architecture (ISCA)*. IEEE, 2024, pp. 818–833.
- [124] J. Bang, Y. Choi, M. Kim, Y. Kim, and M. Rhu, “vtrain: A simulation framework for evaluating cost-effective and compute-optimal large language model training,” *arXiv preprint arXiv:2312.12391*, 2023.