Imperial College London

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Second Year Design Project

ELEC50003/ELEC50008

The MARS Rover

Gorup 1

Georgio Chaimali
Dimitrios Georgakopoulos
Edvard J.S. Holen
Hyunjoon Jeon
Josiah Mendes
Raghav Viswakumar

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Figure 1: Sample Figure

Sample Reference[1]

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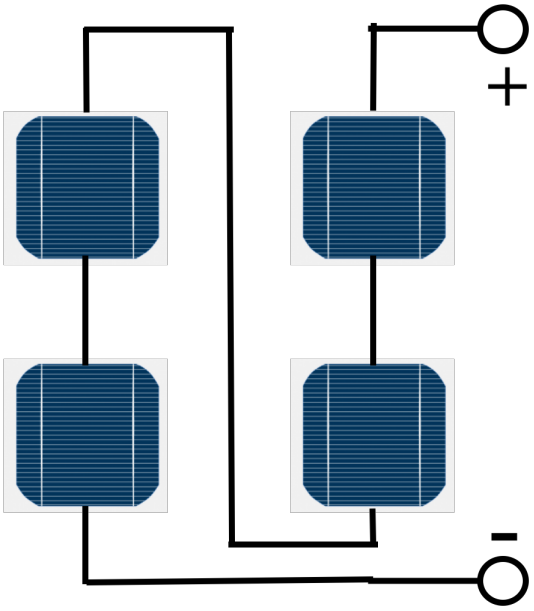
Hello



2.4 Vision

Abstract

The purpose of the Vision module is threefold: 1. Capture data from camera module; 2. Detect objects of interest within the current view and send their location to the Control module; and 3. Send image data to Control for streaming to Command.

2.4.1 Hardware Organisation

The Vision module comprises of two main hardware elements: the Terasic DE10-Lite, a cost-effective Altera MAX 10 based FPGA board [2] and the Terasic D8M-GPIO camera package [3] that interfaces with the FPGA through the onboard GPIO connectors.

These hardware choices were made by the project organisers, but are also sufficient and capable of carrying out the tasks at hand. As the FPGA's hardware is configurable, it is more flexible than other embedded systems that are limited to a general purpose processor, and is also able to handle both streaming and processing of high resolution images without significant compromises on framer-

ate or data speed through the use of concurrent operations and dedicated blocks for signal processing applications like multiplication. This particular FPGA is also equipped with a 4-bit VGA output which is useful for debugging object detection live, and also has a connector for an Arduino Uno R3 shield, [2] which can be used to interface with the ESP32 used for control.

In order to perform general purpose operations like to configure camera settings and to provide a debugging interface, a Nios II soft core was instantiated on the FPGA. Alternatively, to implement a more advanced image processing algorithm or to reduce hardware components, a FPGA with a hard core, known as a FPGA System-On-Chip (FPGA SoC) [4]

3 Evaluation and Conclusion

References

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[2] T. Inc. "De10-lite board." (), [Online]. Available: https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English%5C&No=1021.

[3] ——, "D8m gpio - 8 mega pixel digital camera package with gpio interface." (), [Online]. Available: https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English%5C&No=1011.

[4] I. Corporation. "Intel® fpgas & soc fpgas." (), [Online]. Available: https://www.intel.co.uk/content/www/uk/en/products/details/fpga.html.