

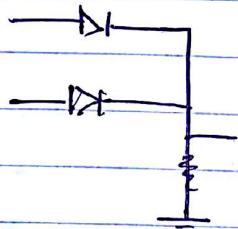
Logic circuit Implementation

Diode logic Gates

(1) Forward biased

Reverse bias

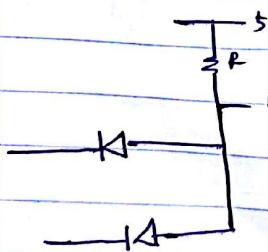
Applications of Diodes - switch



A	B	F
0	0	0
0	5	4.3
5	0	4.3
5	5	4.3



A	B	F
0	0	0
0	1	1
1	0	1
1	1	1

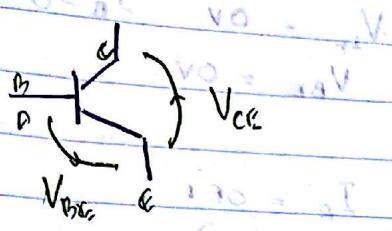


A	B	F
0	0	0.7
0	5	0.7
5	0	0.7
5	5	5V

A	B	F
0	0	0
0	1	0
1	0	0

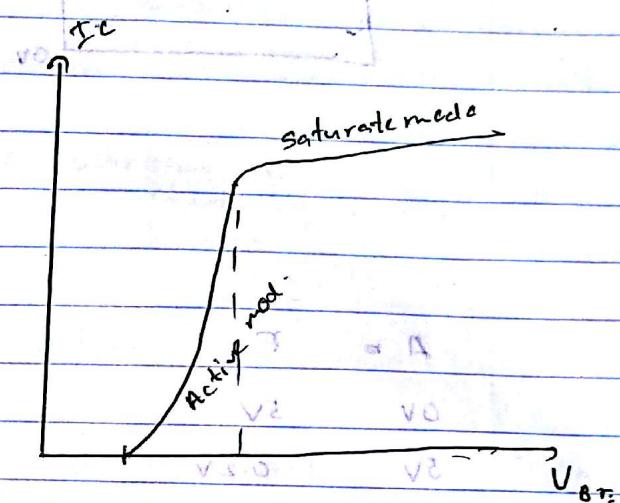
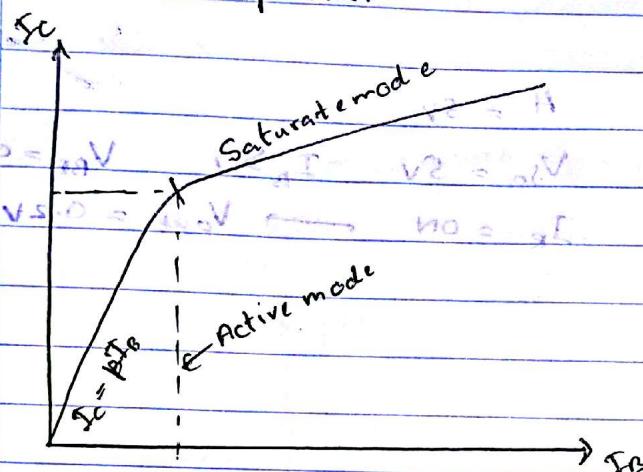


Resistor - Transistor logic family



As a switch - $V_{BE} = 0.7V$

As a amplifier



when V_{BE} beyond the (0.7) that value

To turn on / transistor

(1) & forward bias B-E

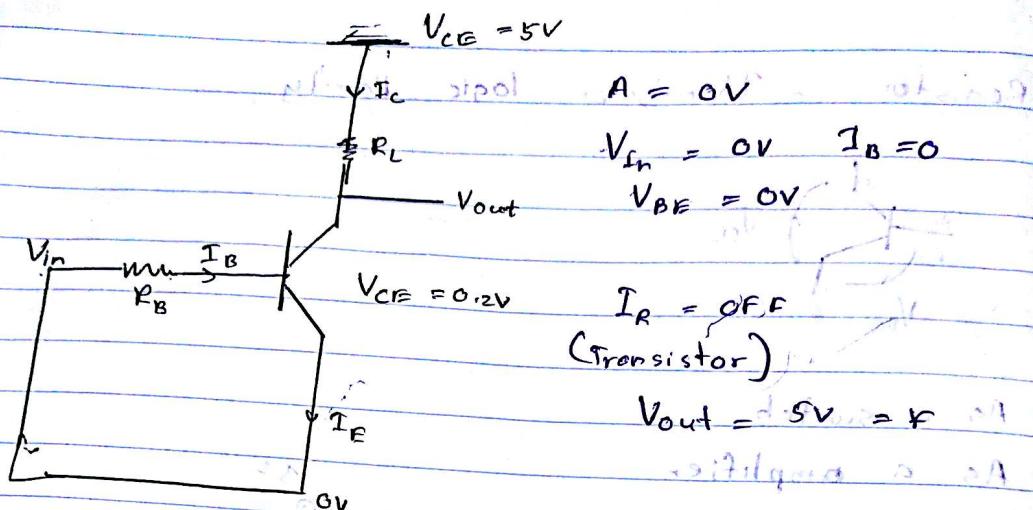
Before $V_{BE} = 0.7$, that means transistor is turn off

when the Active mode

$$I_C \propto I_B$$

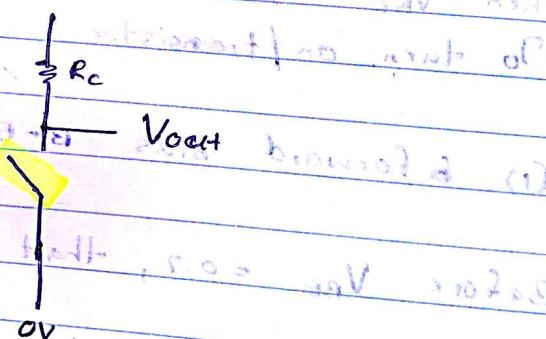
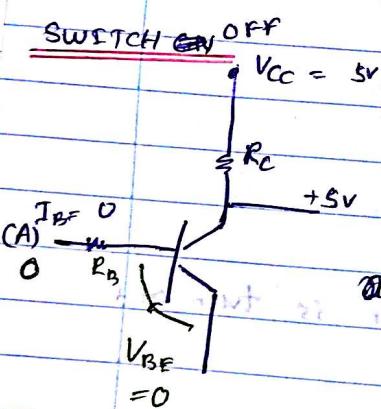
$$(1) I_C = \beta I_B$$

$$(2) I_E = I_C + I_B$$

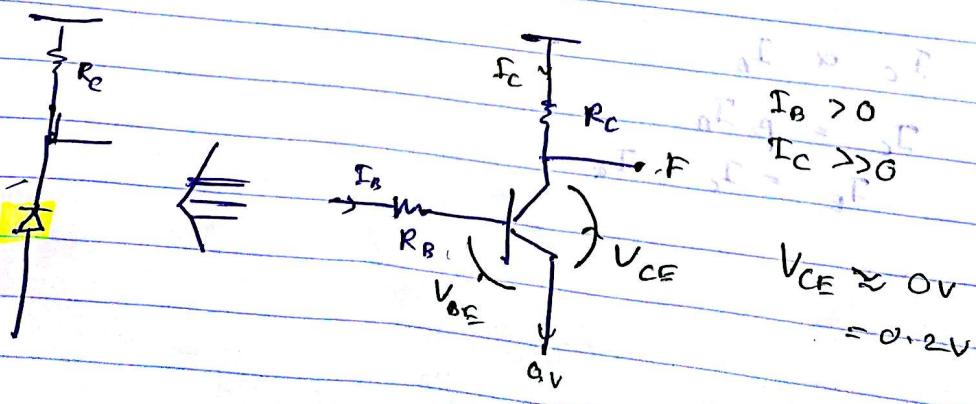


$A = 5V$
 $V_{In} = 5V$, $I_B > 0$, $V_{BE} = 0.2V$
 $I_R = ON \rightarrow V_{out} = 0.2V = b$

$A = F$
 $0V$
 $5V$
 $0.2V$

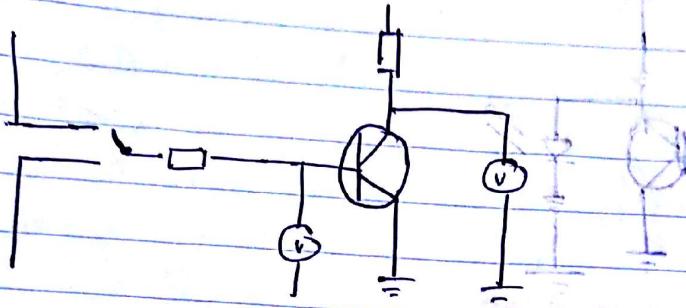


SWITCH ON



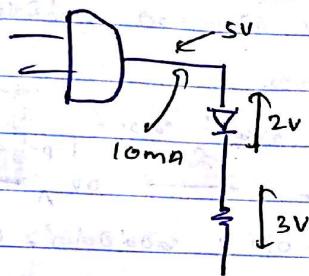
Atlas

Not gate



Note

5 ~ 20 mA - Generally Led working current
 Led working voltage - 2 V



Special Note

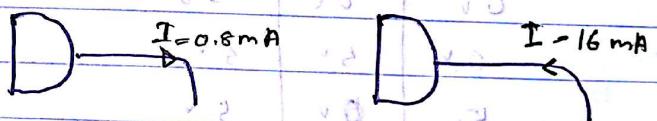
IC එක හැඳුනුවේ current නී
 0.6mA නිස්පානි IC එක හැඳුනුවේ current නී 16 mA නිස්පානි

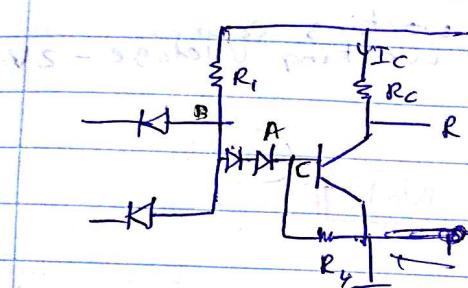
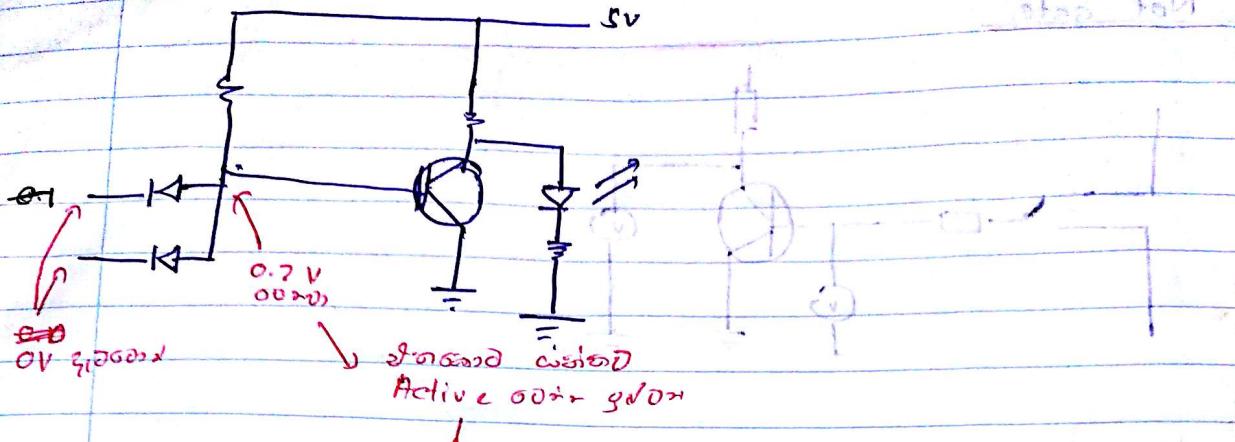
$$\frac{3}{10 \times 10^{-3}} = R$$

$$300\Omega = R$$

වෙනත් පරිභේදවල

Range සඳහා සිදු කළ තොරතුරු,
 සිදු කළ තොරතුරු විට මිනිමු
 470 Ω නො නොවන
 Brightness යුතු කළ හෝ
 ගිංචර් පෙන්වන





* A - यह वर्गमूलक रोजानीवाले, जिसमें Input = 0V होता है। B का उत्तर = 0.7V होता है और उत्तर का उत्तर द्वारा बनाया जाता है।

* यहां पर्याप्त सिर्फ एक अंतर्भूत त्रिविधि है। यहां एक अंतर्भूत त्रिविधि है।

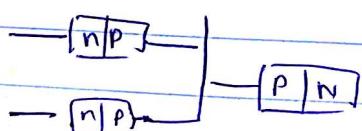
उत्तर = 0.7V होता है, जबकि उत्तर = 0V होता है।

A	B	R
0V	0V	5V
0V	5V	5V
5V	0V	5V
5V	5V	0V

logical 0 के लिए, जब वाला वर्गमूलक होता है।

वर्गमूलक होता है 0.7V होता है।

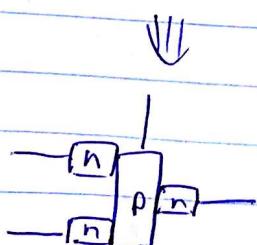
वाला वर्गमूलक होता है तो उत्तर द्वारा बनाया जाता है।



* C - A द्वारा बनाया गया Input त्रिविधि

वाला वर्गमूलक होता है जिसमें B = 0V होता है।

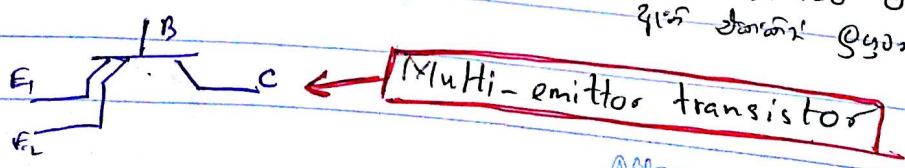
जब वाला वर्गमूलक होता है, A द्वारा बनाया जाता है। वाला वर्गमूलक होता है, जबकि वाला वर्गमूलक होता है।



Rule

प्रत्येक ट्रांजिस्टर का एक विकल्प है जिसके द्वारा यह त्रिविधि बनायी जा सकती है। यह त्रिविधि वाला वर्गमूलक होता है।

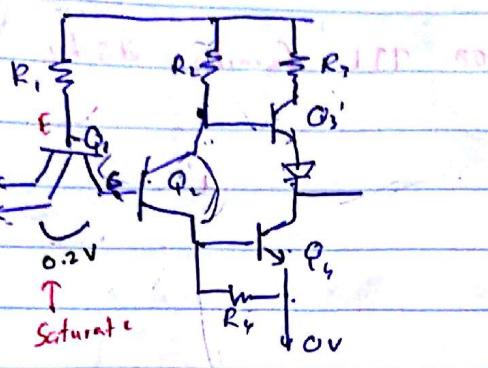
यह त्रिविधि वाला वर्गमूलक होता है। यह त्रिविधि वाला वर्गमूलक होता है।



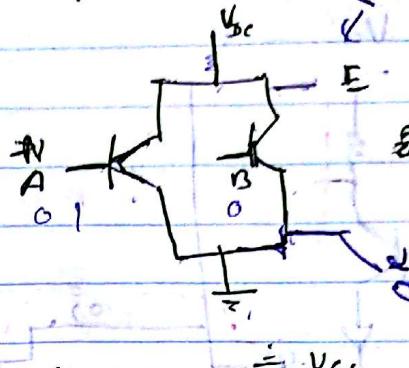
Allas

Transistor - Transistor logic family (TTL Family)

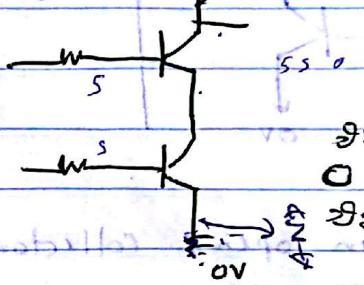
NOR



PL



NAND



If any input is 0V

$Q_1 = \text{ON}$ (saturated)

$Q_2 = \text{OFF}$ $\leftarrow C = 0.2V$

$Q_4 = \text{OFF}$ $\leftarrow Q_2 \text{ OFF}$

$Q_3 = \text{ON}$ through R_2

$$F = 4.1V \text{ or } 4.3V$$

Key point 2: Q_2 is off
(-) position (+) position

(+) position (-) position

When $A = B = 5V$

$Q_1 = \text{ON} \Rightarrow Q_2 = \text{OFF}$

B-C P-N junction Forward Biased

(inverse mode) off d transistor.

$Q_1 = \text{ON}$ (saturated)

$Q_2 = \text{ON} \Rightarrow Q_4 = \text{ON}$

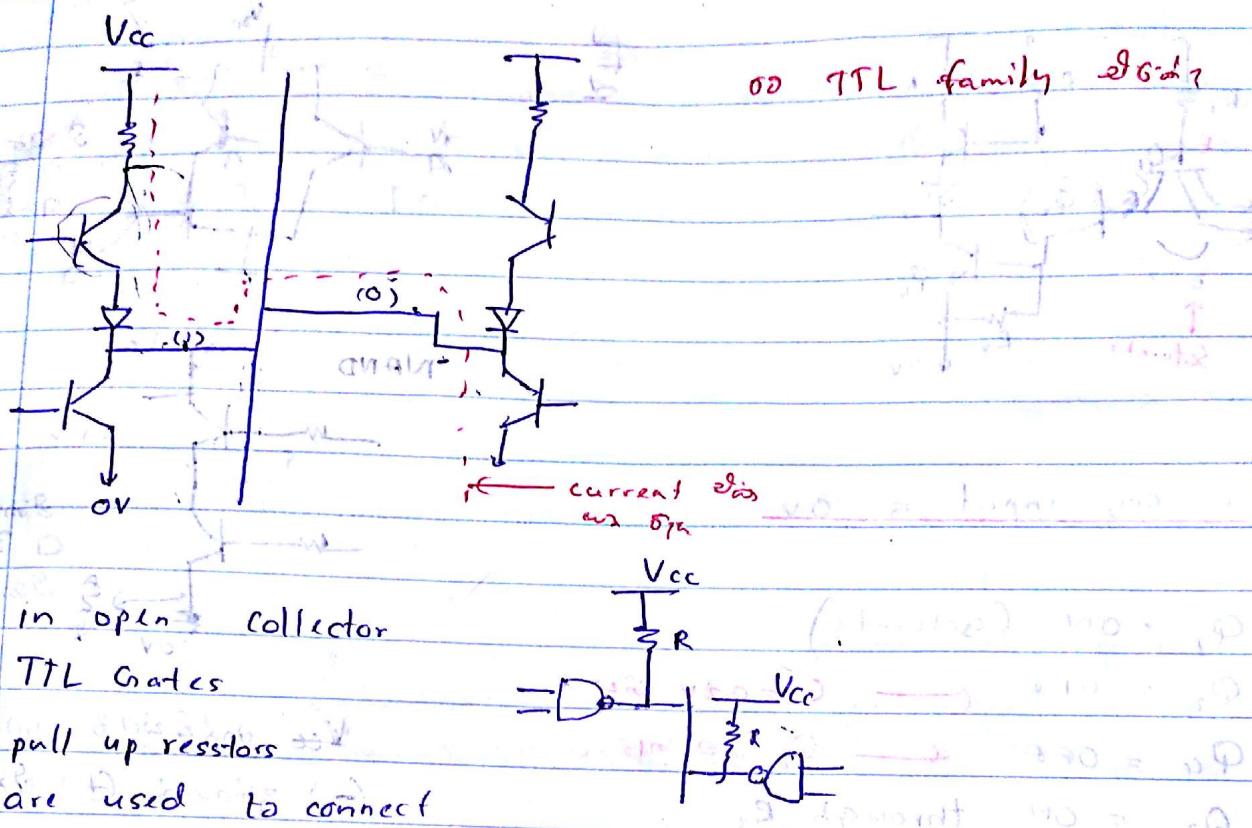
$Q_3 = \text{ON}$ (saturation mode)

$Q_3 = \text{OFF}$

EC നേരിലെ മാറ്റവേദന
കുറയുന്ന പ്രത്യേകിയ വിവരങ്ങൾ
ഒരു ഉപാധി കൂടി കുറയുന്നത്
ഒരു സൈറ്റിൽ നിന്നും
മുൻപു തിരുത്തിരുത്തി

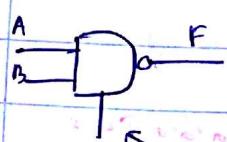
$$F = 0V$$

$$F = '0'$$



But we can't use gates in high speed functions

Therefore we are using Tri-state TTL Family



CI Tri-state
Input

Output
is 0 or 1 or Z
depends on C
and B, A

This is the practical
high speed function

Output F = 0

Output F = 1

Output F = Z

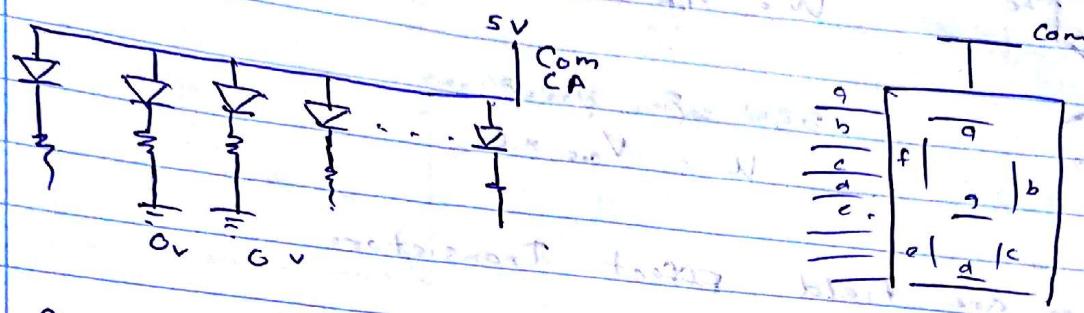
Output F = 0

Output F = 1

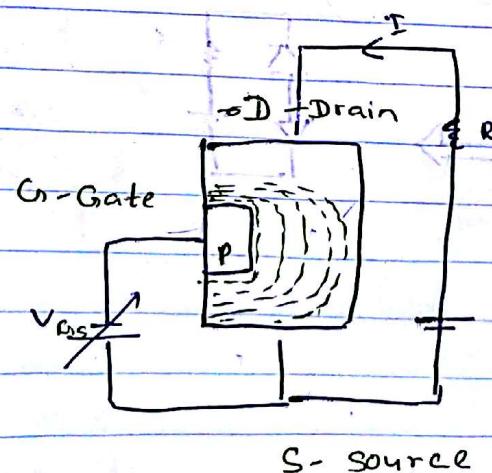
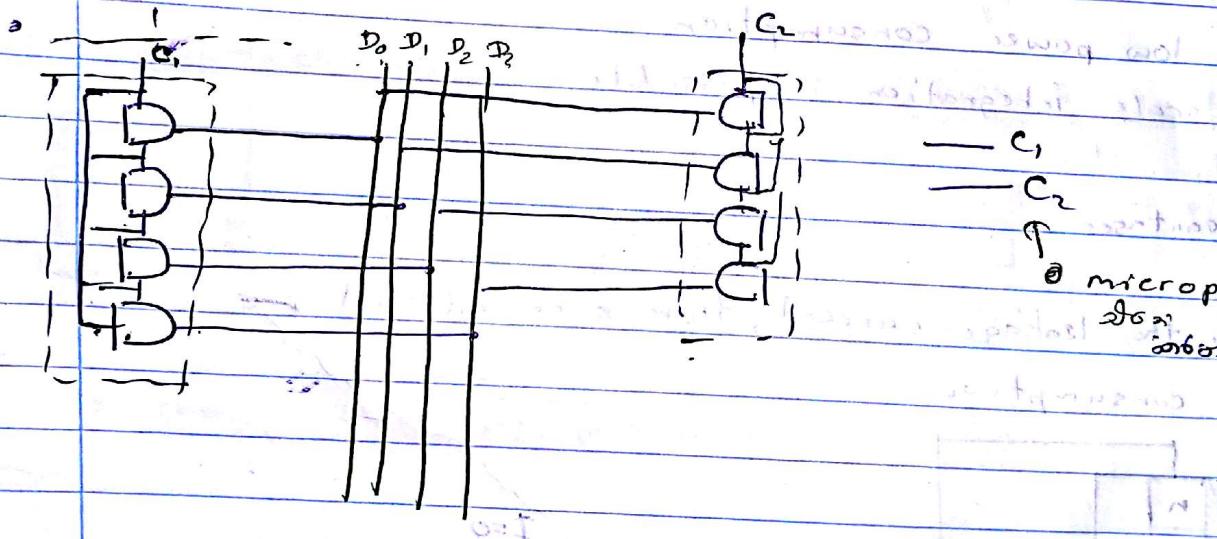
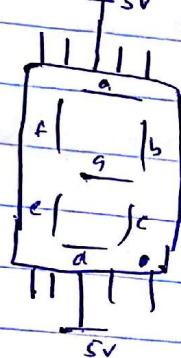
High independent state

Therefore we can use common bus to turn on the A... which we want

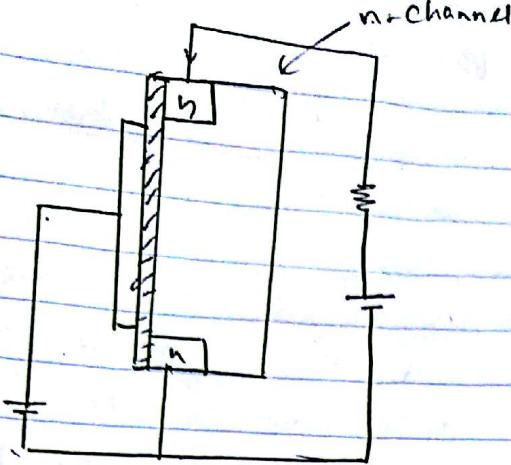
Common anode



common anode 0@2 2nd year



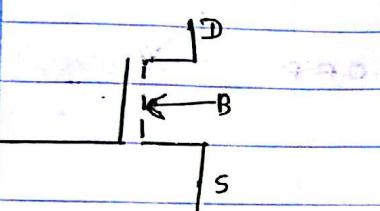
$$V_{GS} \propto I$$



$$V_{GS} \uparrow = I_D \uparrow$$

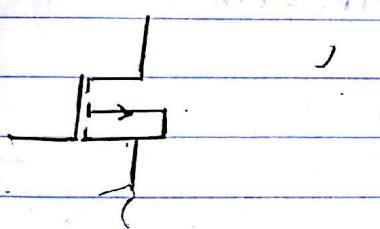
Metal Oxide Semiconductor

N - Channel FET

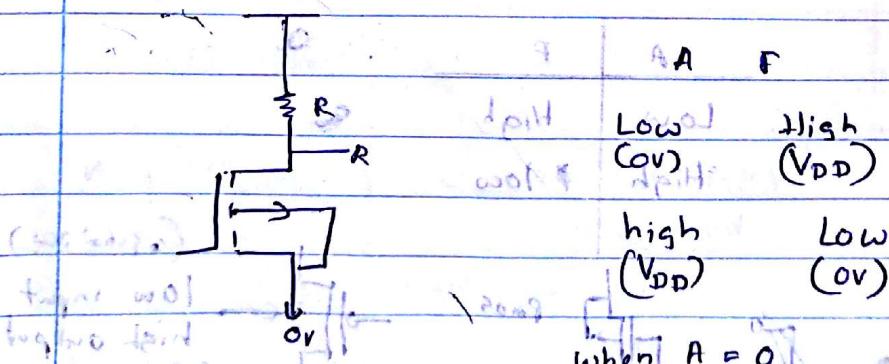


MOS - N - ch. FET

MOS - P - ch. FET



N channel MOS FET - NOT Gate,



There is a power consumption in R

resistor. It's the disadvantage of this gate.

$$\text{TR - OFF} \Rightarrow I_D = 0 \Rightarrow F = V_{DD}$$

$$\text{TR - ON} \Rightarrow I_D > 0 \Rightarrow F = 0$$

Advantages

Advantages

$$V_{DD} = V_{SS}$$

Low power consumption

less leak current

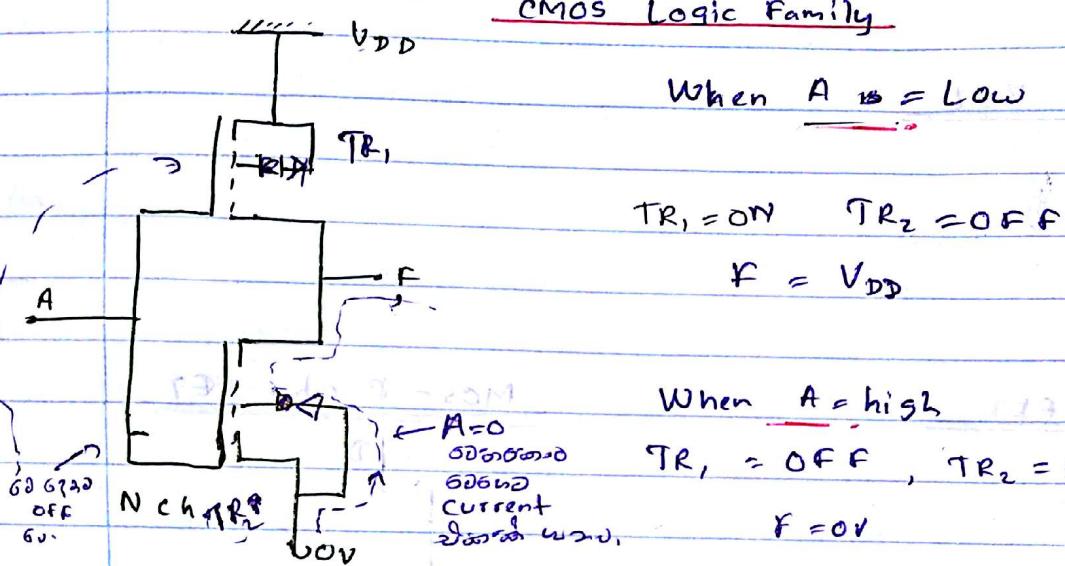
W

Disadvantages

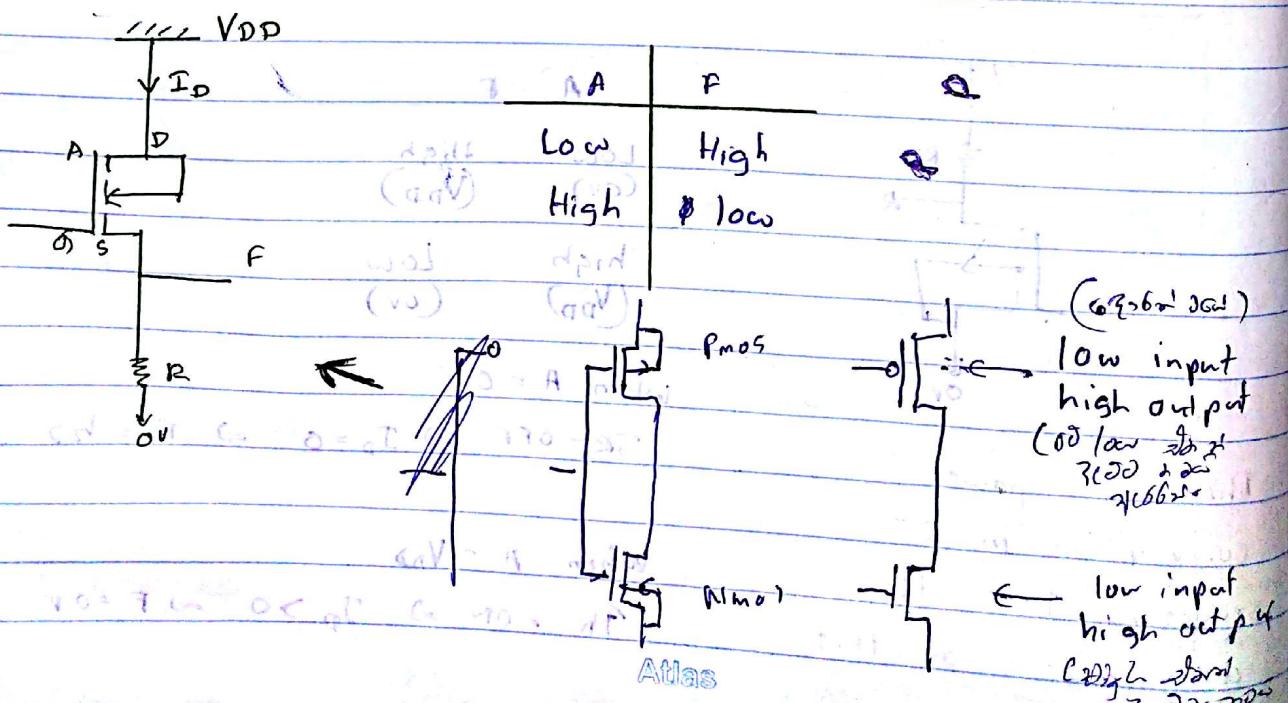
In the external resistance, There is power consumption.

complementary metal oxide semiconductor logic family

CMOS Logic Family



ಸಂಕ್ಷಿಪ್ತ ಮಾರ್ಪಳದಲ್ಲಿ ವಿವರ ಏಕ ಸಂಗ್ರಹಿತ



MOS Family

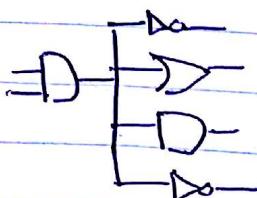
- 1) NMOS FET
 - 2) PMOS FET
 - 3) CMOS FET
 - 4) VMOS } - Gates, low level
 - 5) DMOS } high level integration
MPS, memories
- SSI, MSI, chips, memories

	TTL	CMOS
Family Name	74XX - Series	4000 - Series
	7400 NAND	40XX
	7432 - OR	45XX
sub families	74LS00 low power 74L00 - low power 74F00 - Fast 74ALS00 - Advanced low power	4000B ← static charges 45XXB
Supply voltages	5V ± 0.25V	3V ~ +18V
logic levels	+5V → 0.0V ~ 0.4V generated 2.4V → 2.4V ~ 5V (Generated) '0' → 0.0V ~ 0.8V (Recognized) '1' → 2.0V ~ 5V (Recognized)	'0' = 0V ~ $\frac{1}{3}V_{DD}$ $V_{DD} = \frac{2}{3}V_{DD} \sim V_{DD}$

Fan out

10

3~8



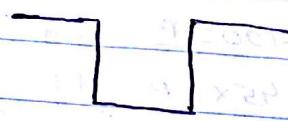
Fanout is 4

Powerup buffer එකකින්
මෙයේ තුළ මෙහෙයුම් හැරු,
තවද නො පෙන්වනු ලබන්න
රහස්‍ය.

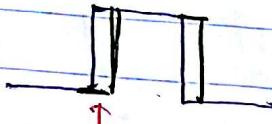
propagation Delay

3 ~ 10ns (MHz) ~~135 ns~~
(slow)

D_n



Out



Summary

Fast

Reliable

Slow

Cost Effective

less

power consumption

More

Entire Digital electronics

Combinational
circuits

sequential

circuits

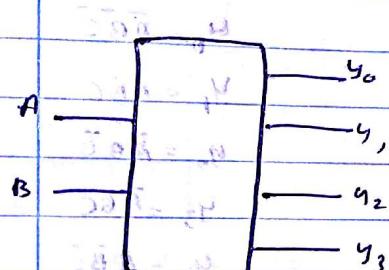
circuits

Combinational circuits

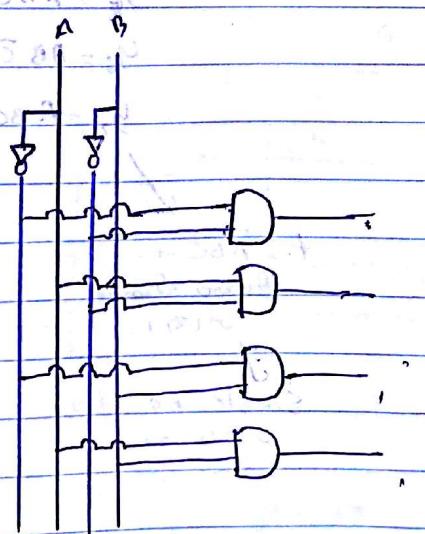
Output depends on inputs

Decoder (standard)

2 to 4 Decoder



A	B	y ₀	y ₁	y ₂	y ₃
0	0	1	0	0	0
1	0	0	1	0	0
0	1	0	0	0	1
1	1	0	0	0	1



$$y_0 = \bar{A}\bar{B}$$

$$y_1 = \bar{A}B$$

$$y_2 = A\bar{B}$$

$$y_3 = AB$$

minimize minterms

maximize maxterm

Y₀

Y₁

Y₂

Y₃

Y₀

Y₁

Y₂

Y₃

Y₀

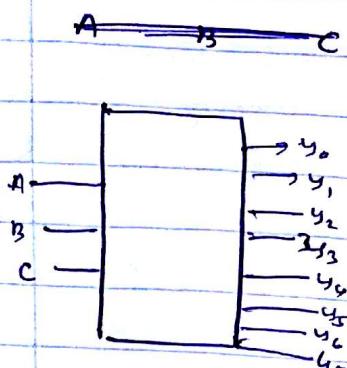
Y₁

Y₂

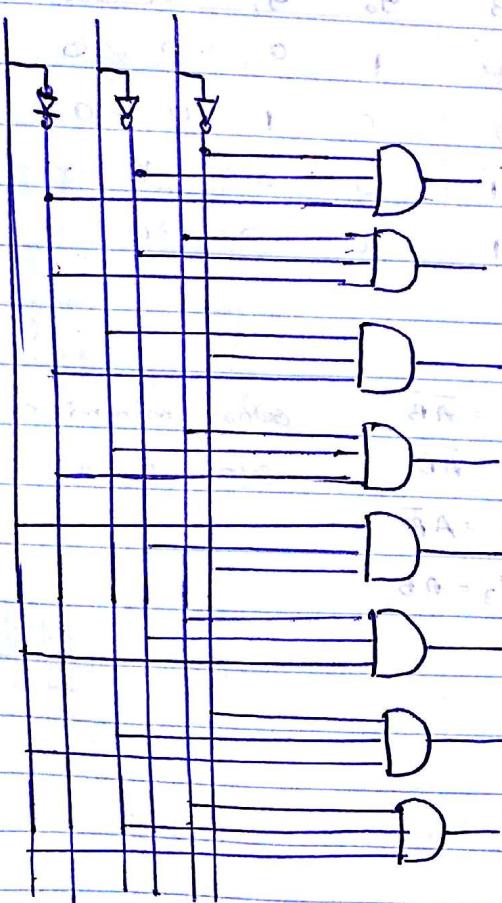
Y₃

Ans

3 to 8 Decoder



A	B	C	y_0	y_1	y_2	y_3	y_4	y_5	y_6	y_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1



$$y_0 = \bar{A}\bar{B}\bar{C}$$

$$y_1 = \bar{A}\bar{B}C$$

$$y_2 = \bar{A}BC$$

$$y_3 = A\bar{B}\bar{C}$$

$$y_4 = A\bar{B}C$$

$$y_5 = AB\bar{C}$$

$$y_6 = A\bar{B}C$$

$$y_7 = ABC$$

✓

$$f = \bar{A}\bar{B}\bar{C} + \dots$$

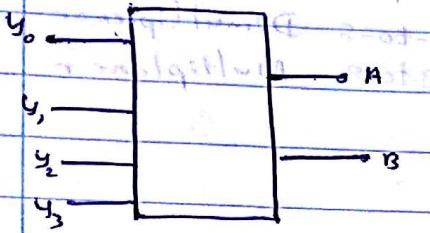
சீர்க்க விரைவு கூடுதல்.

J
Single equation
கீழே கொடுக்க.

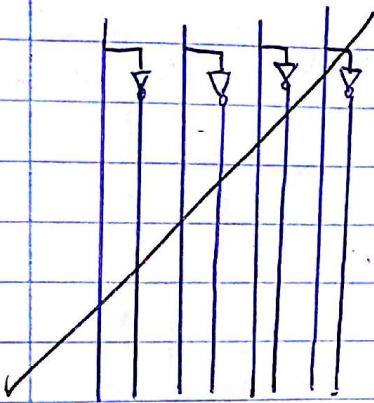
Combined

Encoder

4 to 2 Encoder



y_0	y_1	y_2	y_3	A	B
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

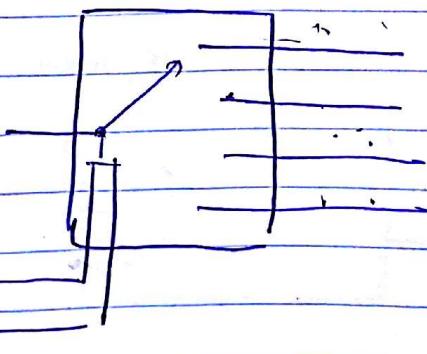


$$A = \bar{y}_0 \bar{y}_1 y_2 \bar{y}_3 + \bar{y}_0 \bar{y}_1 \bar{y}_2 y_3$$

$$B = \bar{y}_0 y_1 \bar{y}_2 \bar{y}_3 + \bar{y}_0 \bar{y}_1 \bar{y}_2 y_3$$

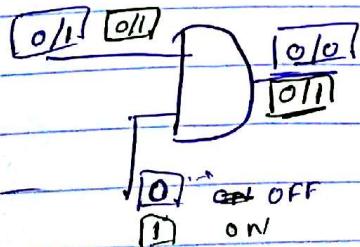
encoders @ Input End ~~11~~ 12

Demultiplexer

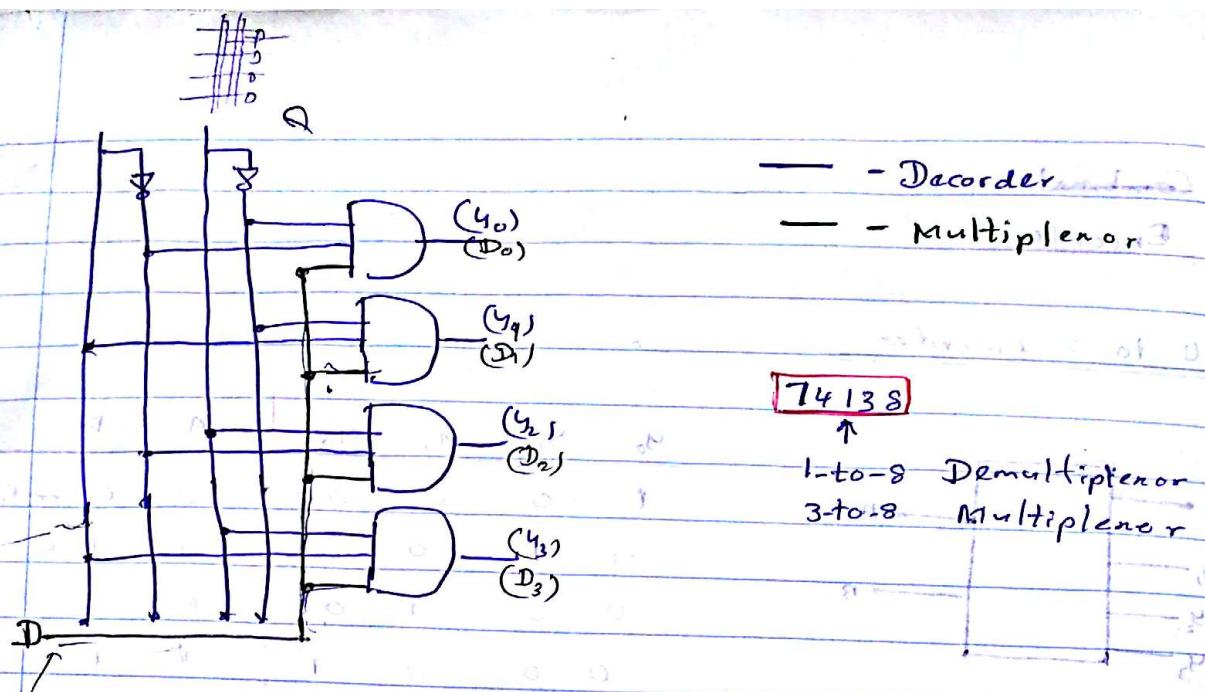


A	B	Action
0	0	D \rightarrow D ₀
0	1	D \rightarrow D ₁
1	0	D \rightarrow D ₂
1	1	D \rightarrow D ₃

1-4 Demux



Atlas

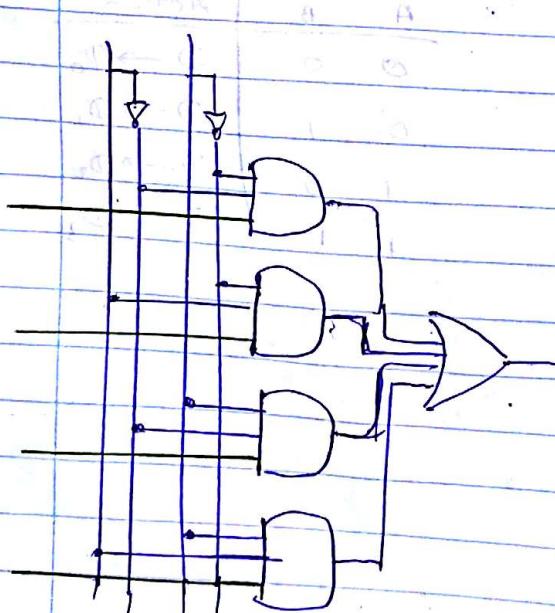
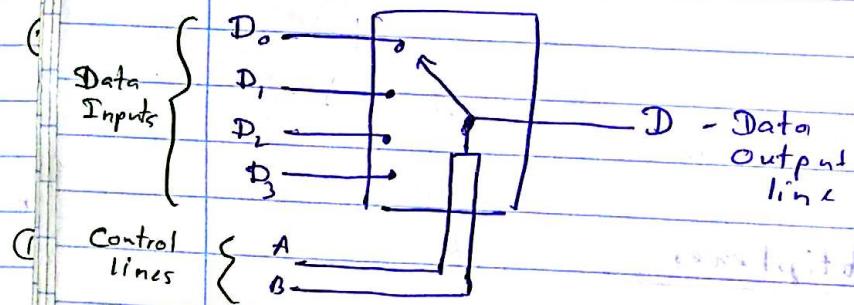


74138

↑
1-to-8 Demultiplexer
3-to-8 Multiplexer

Design the 1-to-8 Demultiplexer

Multiplexer



Atlas

Design 8 to 3 maximization

Design 2-bit adder

A B ~~Sum~~ Carry

0 0 0 0

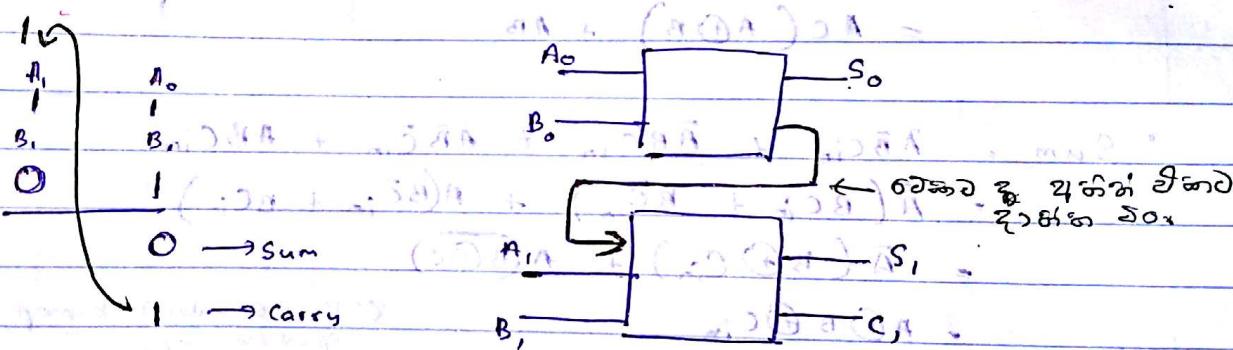
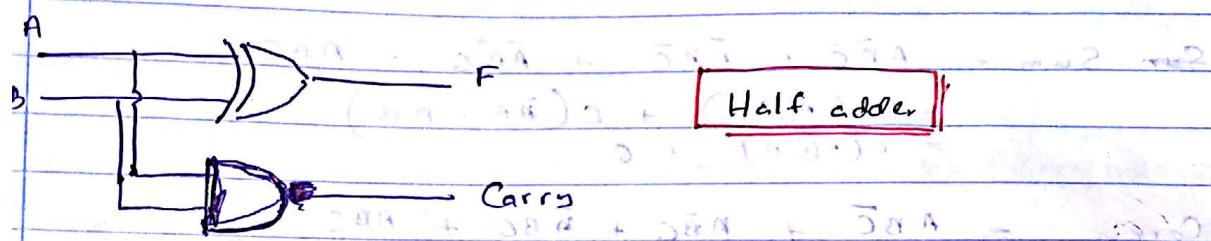
0 1 0 1

1 0 1 0

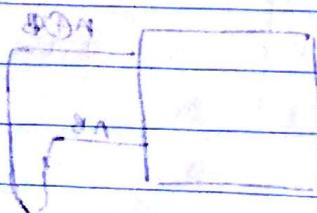
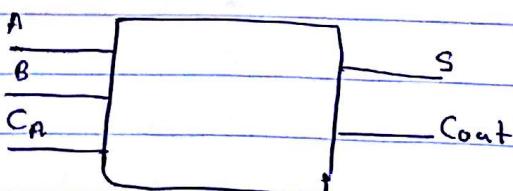
1 1 0 1

$$\text{Sum} = \bar{A}B + A\bar{B} = A \oplus B$$

$$\text{Carry} = AB$$



Full adder



$$S = A \oplus B \oplus C_{in}$$

$$(A \oplus B) + C_{in} = A \oplus B \oplus C_{in}$$

Alles

A	B	Cin	Sum	Cout
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

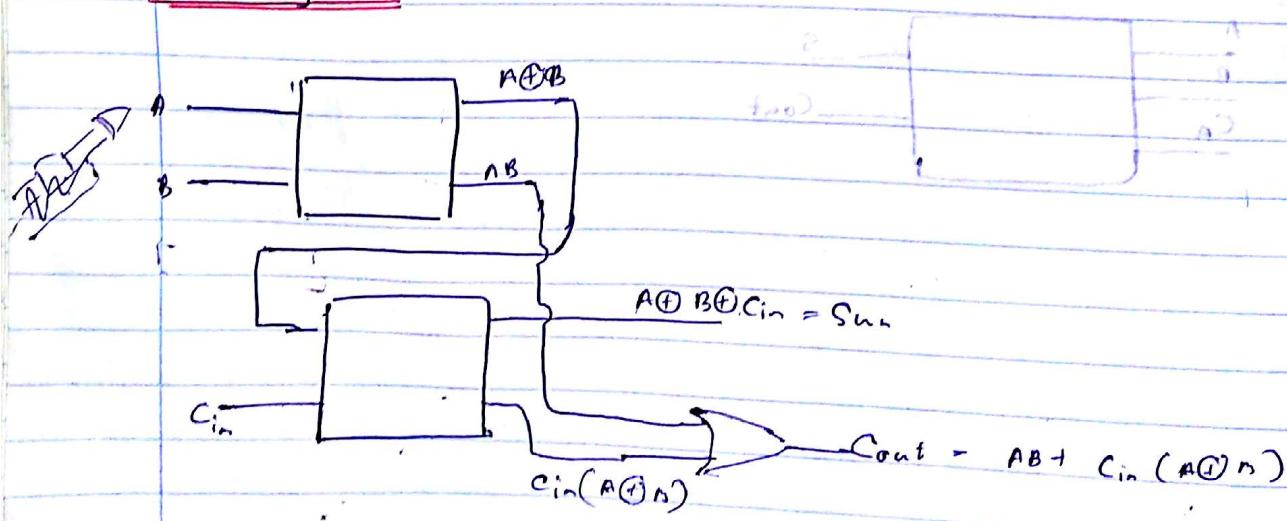
$$\begin{aligned}
 \text{Sum} &= A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC \\
 &= \bar{C}(A \oplus B) + C(\bar{A}B + AB) \\
 &= \bar{C}(A \oplus B) + C
 \end{aligned}$$

$$\begin{aligned}
 \text{Carry} &= A\bar{B}\bar{C} + A\bar{B}C + \bar{A}BC + ABC \\
 &= AC(A \oplus B) + AB
 \end{aligned}$$

$$\begin{aligned}
 \text{Sum} &= \bar{A}\bar{B}C_{in} + \bar{A}\bar{B}\bar{C}_{in} + A\bar{B}\bar{C}_{in} + ABC_{in} \\
 &= \bar{A}(\bar{B}C_{in} + B\bar{C}_{in}) + A(\bar{B}\bar{C}_{in} + BC_{in}) \\
 &= \bar{A}(B \oplus C_{in}) + A(\bar{B} \oplus C) \\
 &= A \oplus B \oplus C_{in}
 \end{aligned}$$

XOR, \oplus \rightarrow k-map
method only

Design a full adder using half adders and necessary other gates

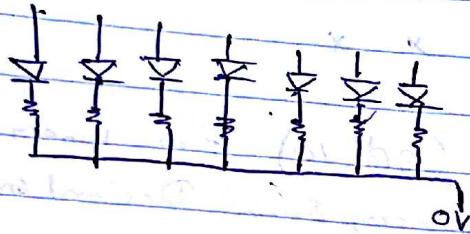


Atlas

Binary number එකාඟු කොන්ට්‍රුයුවෙහි වේ, Decimal කොන්ට්‍රුයුවෙහි

Seven segment display

Common cathode

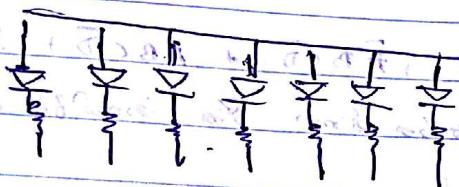


මෙතැන් රෝසක් නම් ගැලීයෙන 5V ප්‍රධාන ප්‍රතිඵලුව,

ප්‍රතිඵලුව,

(Common Cathode - 5V)

Common anode

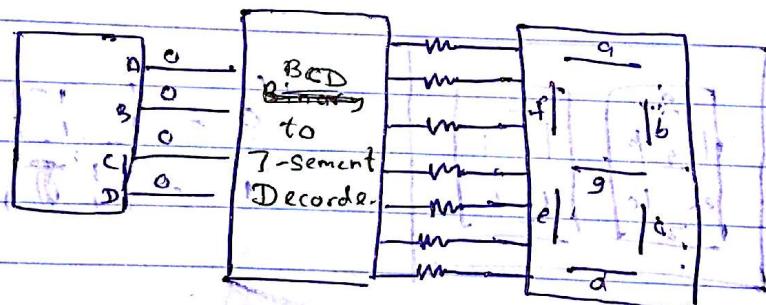


මෙතැන් රෝසක් නම් ගැලීයෙන 0V ප්‍රතිඵලුව

ප්‍රතිඵලුව, ප්‍රතිඵලුව,

ප්‍රතිඵලුව සියලුම ප්‍රතිඵලුව

ALERT, STATUS, BUZZ, POWER



P	A ₃	A ₂	A ₁	A ₀
0	1	0	0	0
0	0	0	0	1
0	0	1	0	
0	0	1	1	
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0

P	a	b	c	d	e	f	g	A
1	1	1	1	1	1	0	0	0
0	0	1	0	1	0	0	1	BCD
1	1	0	1	1	1	0	1	to
1	1	1	1	0	0	1	1	7-segment
0	1	1	1	0	0	0	1	Decoder
1	0	0	1	1	1	1	1	
1	0	0	0	1	1	1	1	
1	1	1	0	0	0	0	0	
1	1	1	1	1	1	1	1	
1	1	1	1	0	0	0	1	
1	1	1	1	1	0	0	1	

Atlas

1010	x x x x x x	x x x x x x	x x x x x x
1011	x x x x x x	x x x x x x	x x x x x x
1100	x x x x x x	x x x x x x	x x x x x x
1101	x x x x x x	x x x x x x	x x x x x x
1110	x x x x x x	x x x x x x	x x x x x x
1111	x x x x x x	x x x x x x	x x x x x x

எனக்கு விடையில் ஒரு எண் நினைவு (ஒ. 10) என்க binary

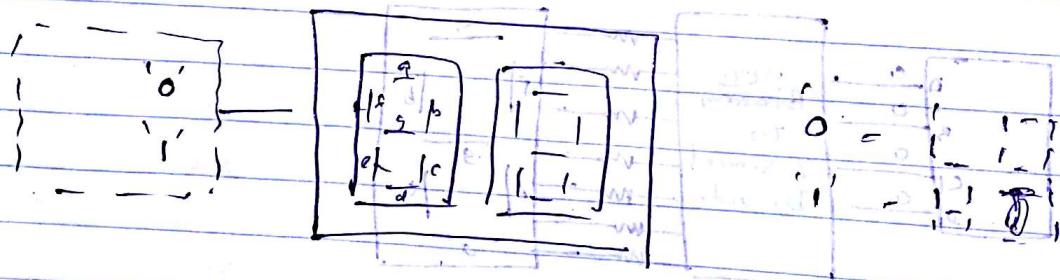
Decimal எண்களை விடை என்க. கூறுவது Binary எண்கள் Decimal என்று (BCD - Binary coded Decimal)

for a

$$f_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}CD + A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}D + D\bar{A}\bar{B}\bar{C}\bar{D}$$

இது ஒரே மூலத் தீர்வு என்று அழைப்பது விரைவாக ஆகும். இது சமீபத்தில் உருவாக்கப்பட்டுள்ளது. இது குறிப்பாக ஒரு குறிப்பாக IC என்று அழைப்பது.

7447, 7448, 74247, 74248



A a. b. c. d. e. f. g. a₂ b₂ c₂ d₂ e₂ f₂ g₂

0 0 0 0 0 1 1 1 0 1 1 1 1 0 0 1 1 1 0 1 0 1 0 1 0

1 0 1 0 1 0 0 1 1 0 1 0 0 0 0 1 0 1 0 0 0 0 0 0 0

0 1 0 0 1 1 1 1 1 0 0 1 1 1 0 0 1 1 0 0 0 0 0 0 0

1 0 1 1 1 0 0 0 0 0 1 1 1 1 1 0 0 1 1 0 0 0 0 0 0

0 0 0 0 1 1 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 0 0 0

1 1 1 1 0 1 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 0 0 0

1 1 0 0 1 1 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 0 0 0

0 0 1 1 1 1 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 0 0 0

1 1 1 1 0 1 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 0 0 0

Atlas

g₀ = 0

d₀ = 1

e₀ = 1

f₀ = 1

a₀ = 1

b₀ = 1

c₀ = 1

d₀ = 1

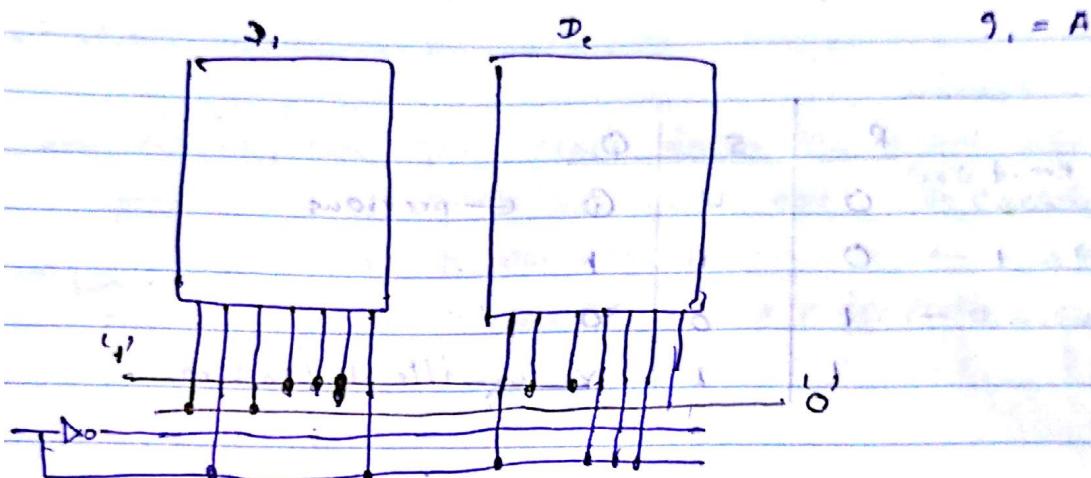
e₀ = 1

f₀ = 1

g₀ = 1

$\bar{D} + A$	a ₁ , b ₁ , c ₁ , d ₁ , e ₁ , f ₁ , g ₁	$a_1 = 0$
0	0 0 0 0 1 1 0	$b_1 = 1$
1	0 1 0 1 0 1 1	$c_1 = 0$
		$d_1 = 1$
		$e_1 = 1$

∴ various state from Q memory $\rightarrow f_1 = 1$

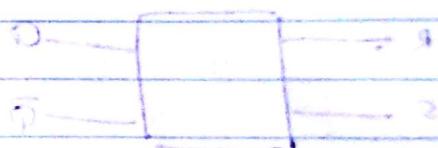


Sequential circuits

Output values of sequential circuits depend on not only present but also previous output value.

Edge flip flop \rightarrow

Flip-Flops \rightarrow



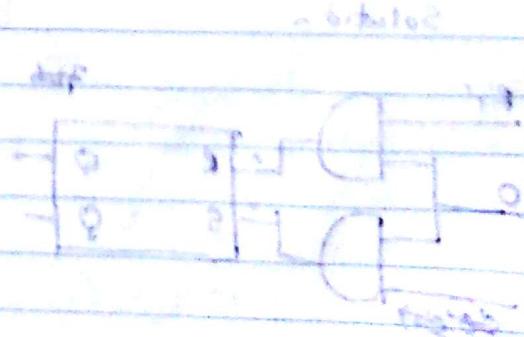
Basic building block of sequential circuits

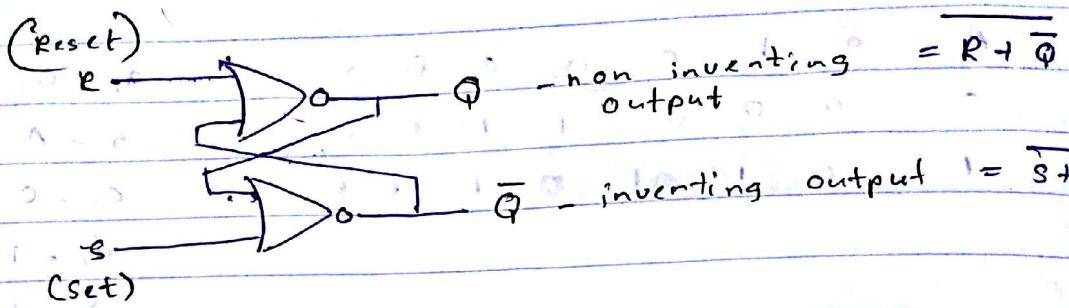
Flip-flop can store 1 bit.

- R-S flipflops

- J-K flipflops

- D-type flipflops





To determine present Q to and take previous \bar{Q}

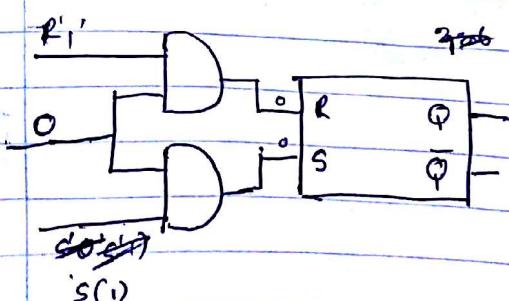
R	S	Q_i			
0	0	0	← previous		
0	1	1			
1	0	0			
1	1	x	← illegal / Forbidden		

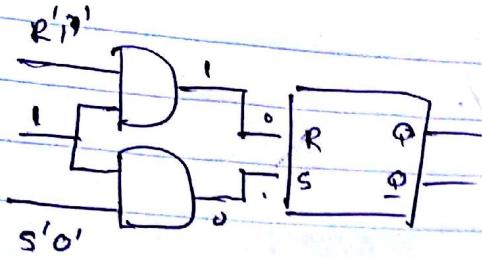


R	S	Q , this is happening to present input
0	0	Initial State
1	1	→ \bar{Q} is changing to Q
1	0	→ Q is changing to \bar{Q}

நிலையின் முப்பொடி தீவிரமாக்கினால் சமான வெளியீடுகளை எடுத்து வரும். இதை அடிக்காட்டி எடுத்து வரும் விளைவை காணும்.

Solution



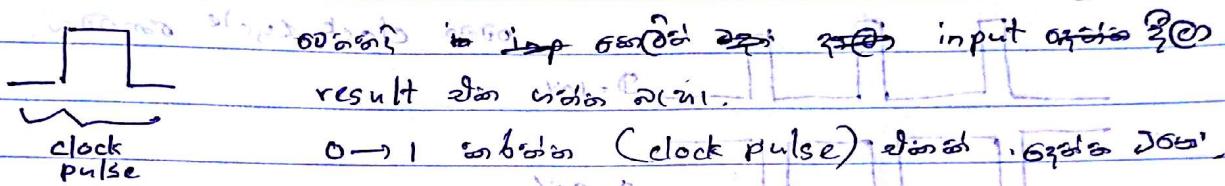


② ஒத்துப் போடு

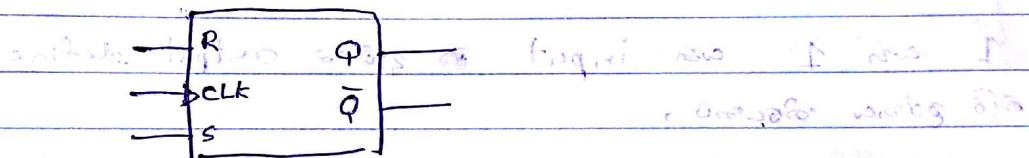
என.

ஒத்துப் போடு

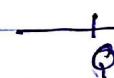
ஒத்துப் போடு என்ற பொருள் குறிப்பு செய்யும்.



$0 \rightarrow 1$ நிலைமே (Clock pulse) என்ற சொல்லும்.



Before applying
clock pulse

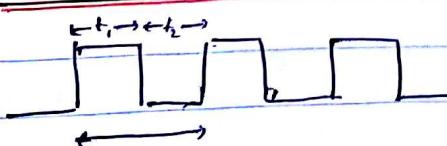


After applying
clock pulse



R	S	Q_{n+1}
0	0	Q_n
0	1	.1
1	0	0
1	1	X

clock signal



① Mark : space = 1:1

$$f = \frac{1}{T}$$

$$\textcircled{2} t_1 = t_2$$

Atlas

$$\begin{aligned}
 \textcircled{3} \quad \text{Duty cycle} &= \frac{\text{on time}}{\text{periodictak}} \times 100\% \\
 &= \frac{t_1}{t_1 + t_2} \times 100\% \\
 &= 50\%.
 \end{aligned}$$

clock signal එහෙන් කිවෙකුම් ඇත්තා නැත්තේ ①, ②, ③ වලින්

clock pulses

විශාල ප්‍රමාණයෙන් පෙන්වනු ලබයි සීමා ප්‍රමාණයෙන් පෙන්වනු ලබයි.

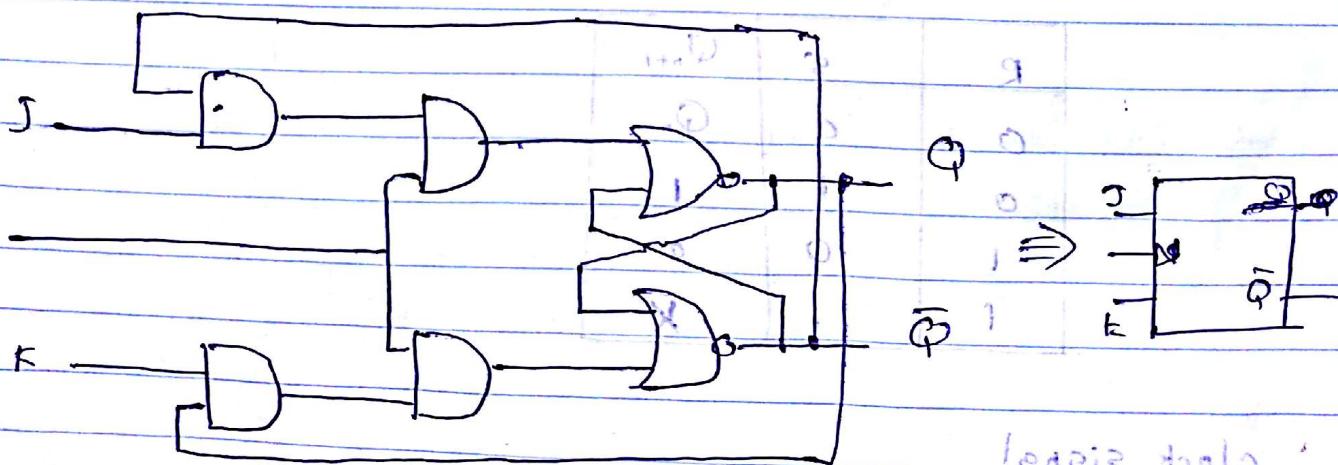
විශාල ප්‍රමාණයෙන් පෙන්වනු ලබයි. $D = 10\%$ න්‍යා නොවා.

විශාල ප්‍රමාණයෙන් පෙන්වනු ලබයි. $D = 90\%$.

1 මෙහි 1 මෙහි input මෙහිලා output define කර ඇති තියෙන්,

Solution
 input 1: \bar{Q}
 output 1: \bar{Q}
 input 2: \bar{Q}
 output 2: \bar{Q}

T-K flipflops

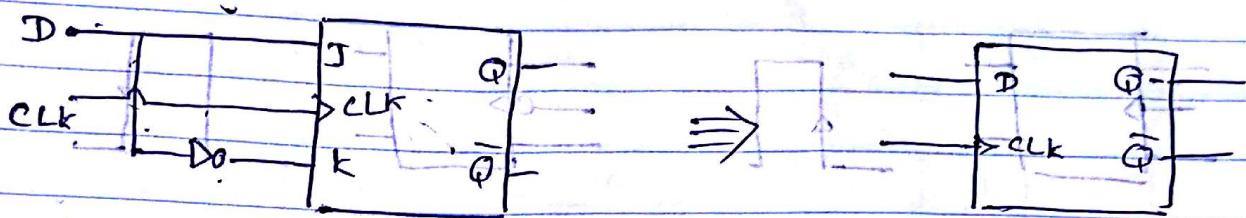


$$\frac{1}{T} = f$$

$$f = \frac{1}{T}$$

J	K	Q_{n+1}	To standard parallel?
0	0	Q_n	not setting
0	1	0	Set setting
1	0	1	Set parallel
1	1	\bar{Q}_n	Reset parallel

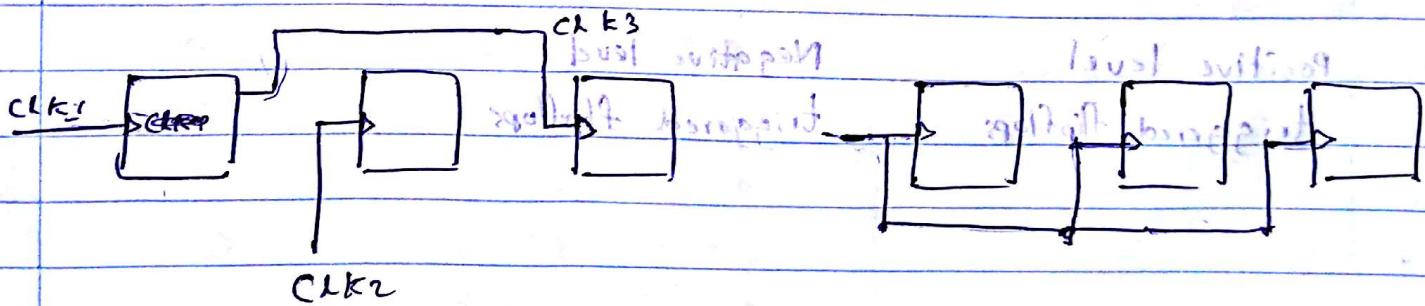
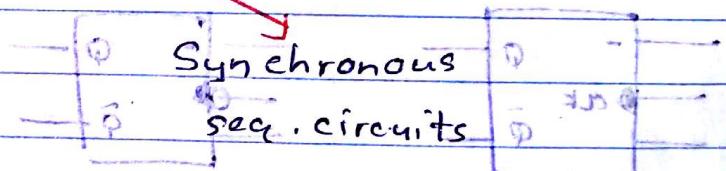
D type Flip-flops



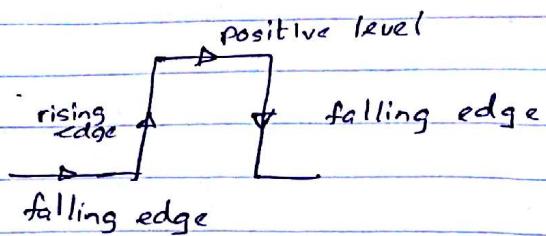
D	Q_{n+1}	edges or on/off goes to memory, then
0	0	0 or 1 can be written
1	1	last writing

Sequential circuits

Asynchronous
sequential circuits

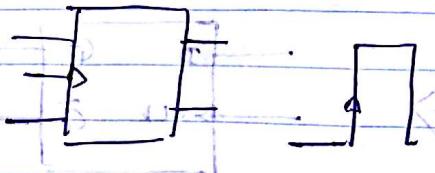


Triggering methods of flip-flops



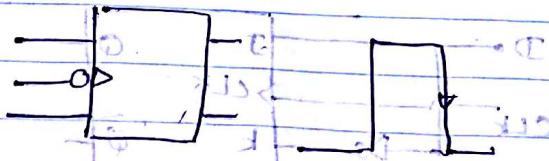
K	C
0	0
0	1
1	0
1	1
1	1

reset, set, reset Q



rising edge

edge triggered flip flops
positive level



falling edge triggered

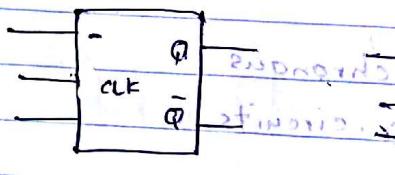
flip flops

0	1
0	0

Negative level

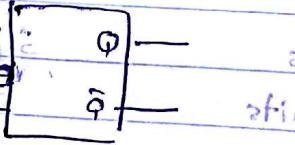
triggered flip flops

chaining flip flops



Positive level

triggered flip flops

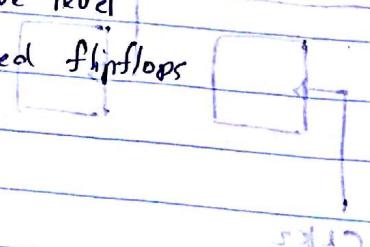


Negative level

triggered flip flops

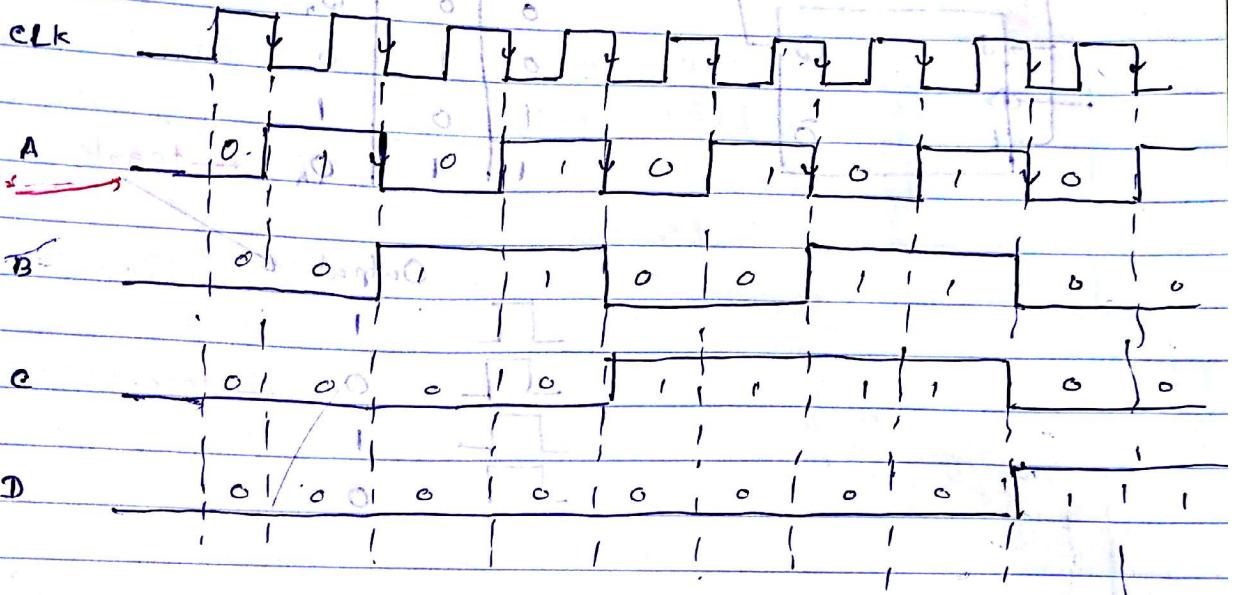
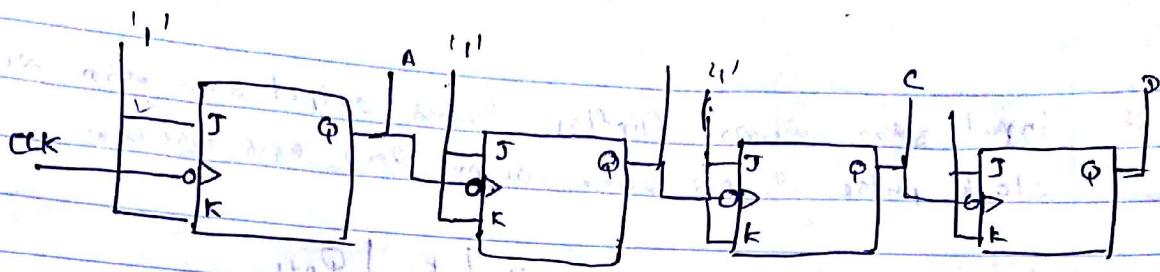
level triggered
flip flops

0	1
1	0



Up Counter

4 bit binary Up Counter



D C B A

0 0 0 0 → 0

0 0 0 1 → 1

0 0 1 0 → 2

0 0 1 1 → 3

0 1 0 0 → 4

0 1 0 1 → 5

0 1 1 0 → 6

0 1 1 1 → 7

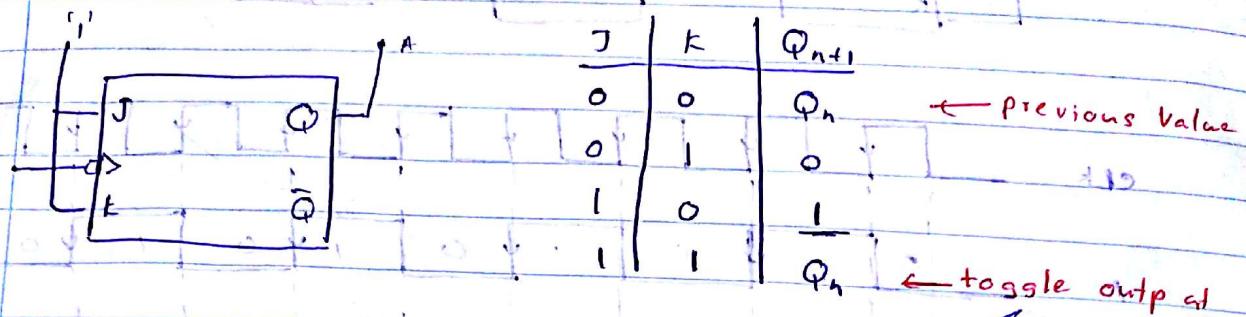
1 0 0 0 → 8

1 0 0 1 → 9

ATL logic gates ~~gates~~ 0@0 1 - 5V
0 - 0V

CMOS logic gates 0@0 1 - (3V - 18V)

* input signal \rightarrow flip-flop receives output from previous stage
 clock pulse \rightarrow input to Q16 of 74LS262

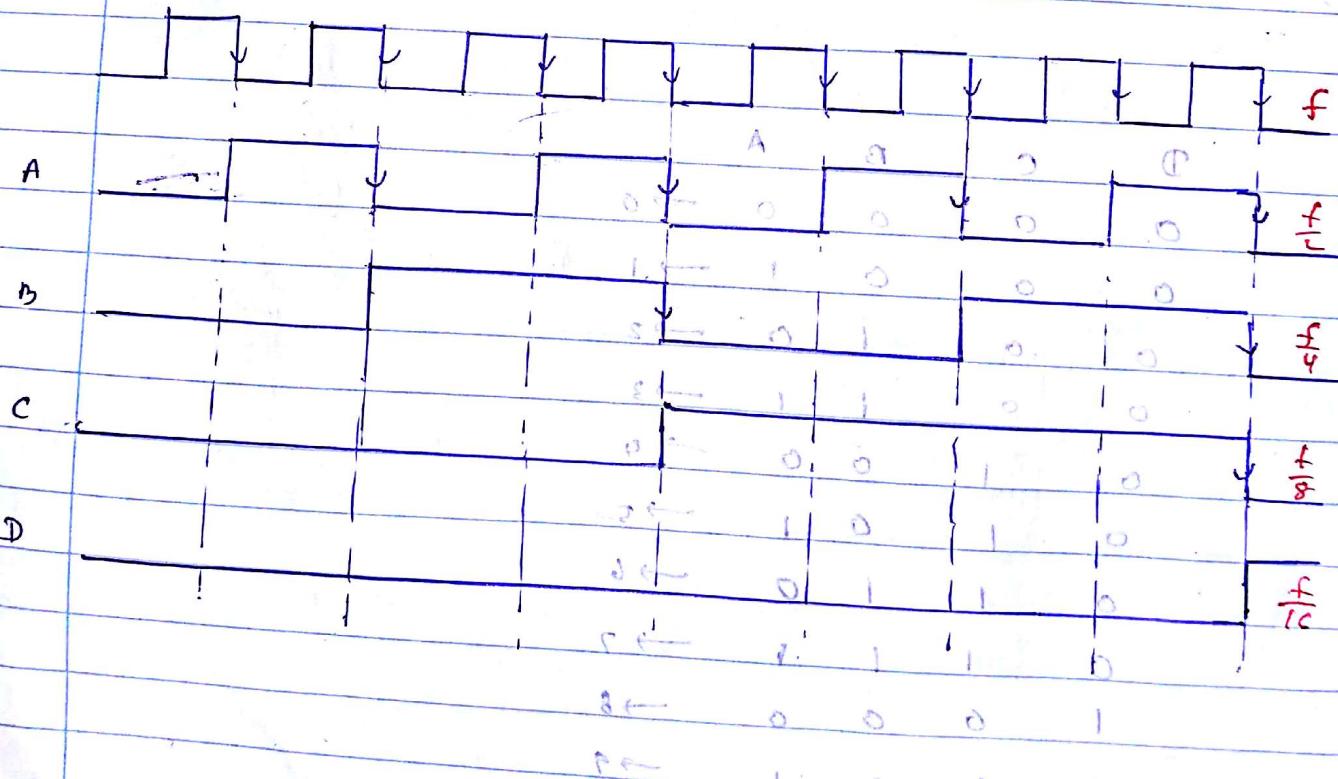


Output



← toggle

edge
trigger
flip

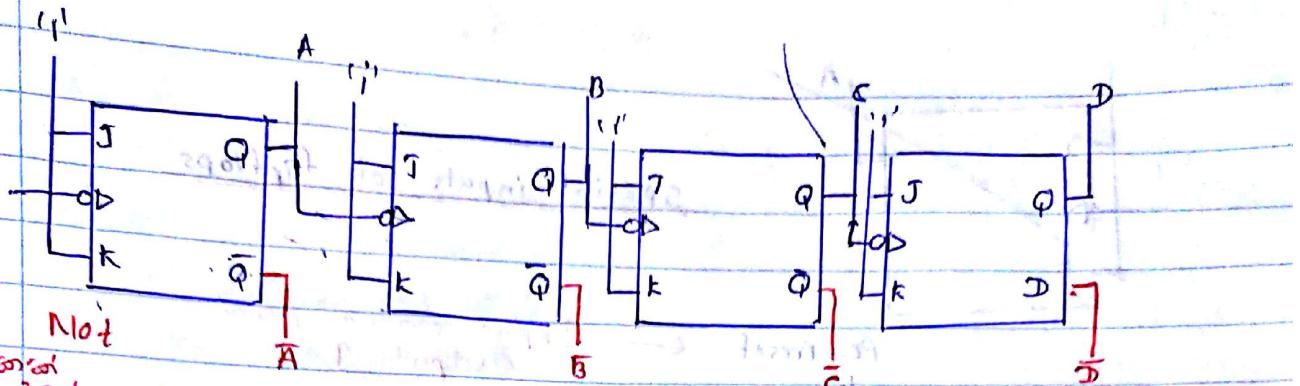


$$v_2 = 1$$

$$v_0 = 0$$

(out \oplus) = 1 6th step (100) 1PP
 6th step (100) 201111

Allas



A එකඟ
gate සිංහල
දුන්ත පෙන්
මාන.

4 bit Binary up counter (GCBIA)

Down counter (\bar{GCBIA})

D	C	B	A	\bar{D}	\bar{C}	\bar{B}	\bar{A}
0	0	0	0	1	1	1	1
0	0	0	1	1	1	1	0
0	0	1	0	1	0	1	1
0	0	1	1	1	0	0	0
0	1	0	0	0	1	0	0
0	1	0	1	1	0	1	0
0	1	1	0	0	1	0	0
1				0	1	1	0
1				1	1	0	0
				1	x	x	0
							1

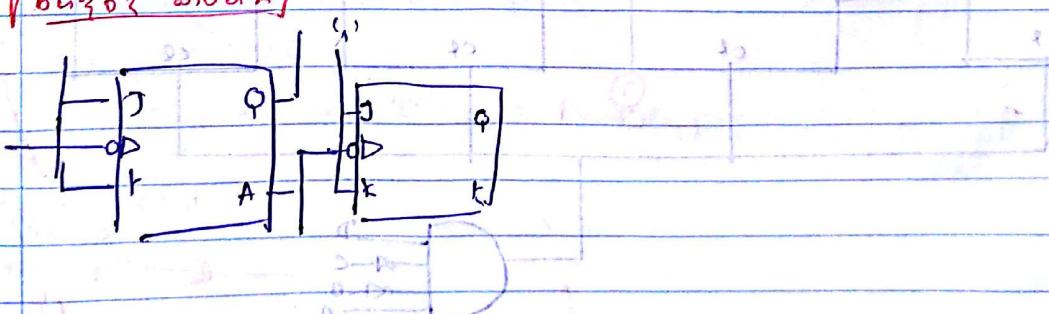
frequency counter මතක් ගොන්. frequency divider මතක් ගොන්

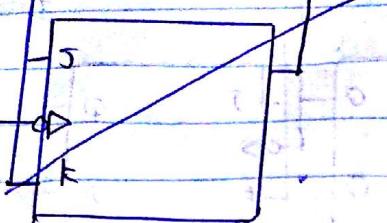
• Computers වල එක එක devices වල එක එක frequency මතක්

වැඩිහිටි දුන්ත clock signal එකට භාවුනු කිරීම එහි

වෙත නොමැත.

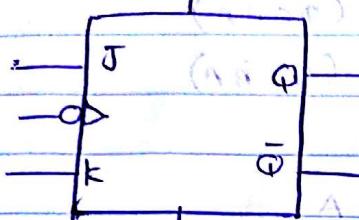
නුගේ කෙටි





Special inputs of flipflops

Pr-Preset \leftarrow Input ගැනක (නො තුළා) Output 1

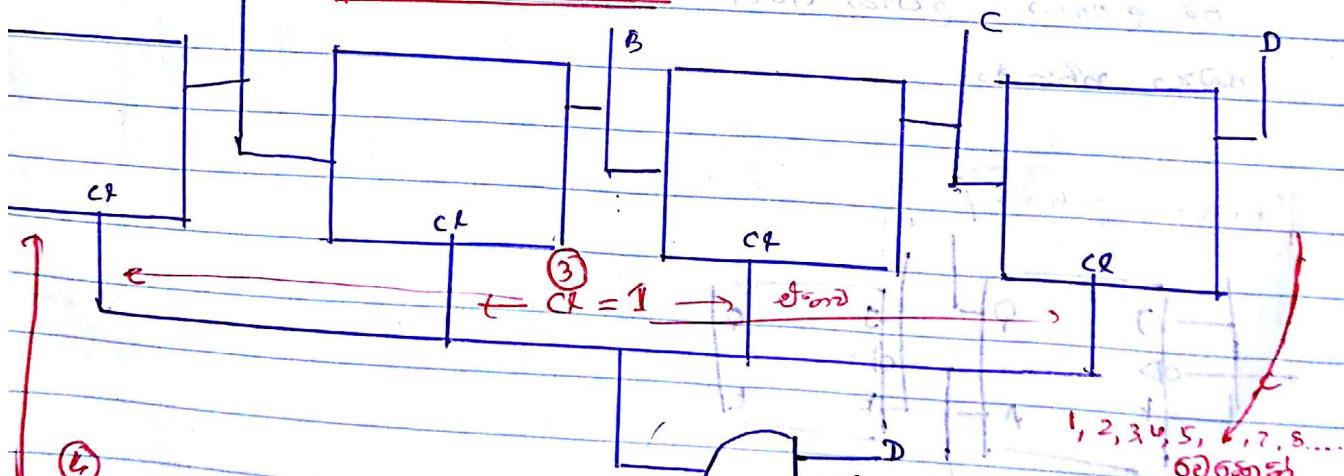


CL-clear \leftarrow Input ගැනක, පෙන්වනු ලබයි Output 0

PR	CL	J	K	Q _{n+1}
0	0	0	0	Q _n
0	0	0	1	0
0	0	1	0	1
0	0	1	1	<u>Q_n</u>
1	0	x	x	1

illegal state සඳහා මෙම පිටපත නො යොමු කළ ඇති අර්ථය නො යොමු කළ ඇති අර්ථය.

MOD-9 Counter



④ flip flop ගැනක,

⑤ සිදු වන යුතු යොමු

Atlas

9 න් ගැනක
machine
state
විද්‍යුත් ස්ථිරා
ක්‍රමය,

Lab Part

Lab එකේ විග්‍යාත කළු.

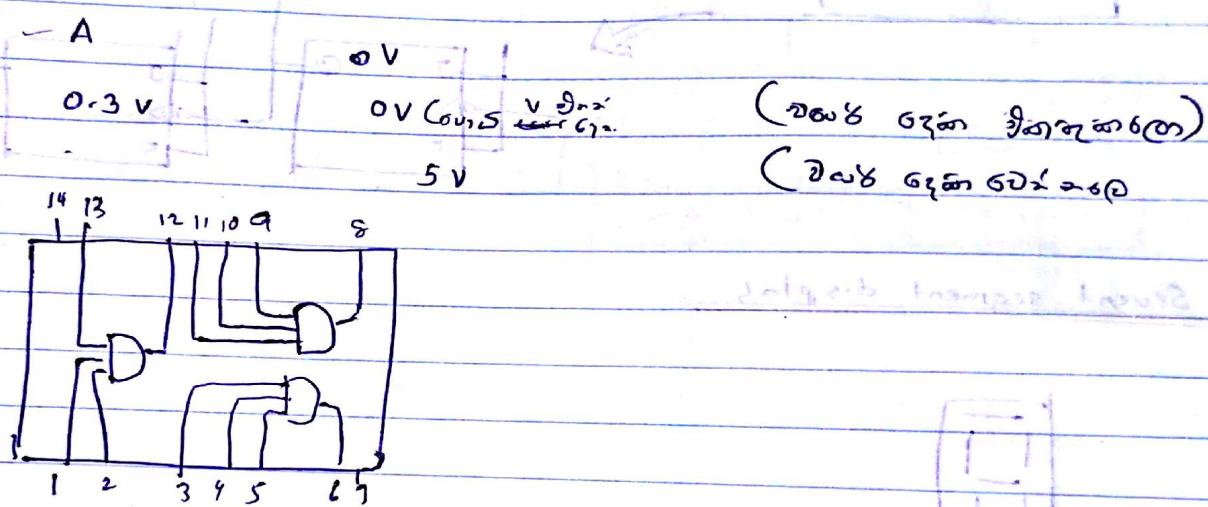
IC එකේ current ප්‍රමාණ.

current නිස්සුවක් නැලු.

නිෂ්පාද බ්ලූ තුළෙටුදු නැලු.

Output button එක යෙලු නැලු.

Hot Powersupply adjust කිරී.



power consumption පිළිය → PMOS, NMOS, CMOS

synchronous පිළිය asynchronouse counter

Not good පිළිය timer da configuration පෙන්වනාර

K maps ගුරුත්වා බැං ජුවන්,

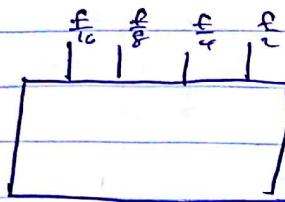
~~but~~ ($\bar{B}C + BC$)

~~K Map da numbers 0000 පිළිය ගුරුත්වා~~

1686

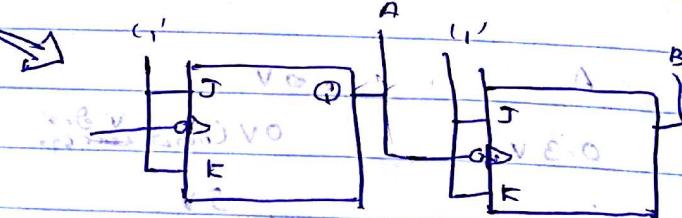
Uses of

- ① Divide by 16 counter
- ② 4-bit binary up counter
- ③ Frequency divider

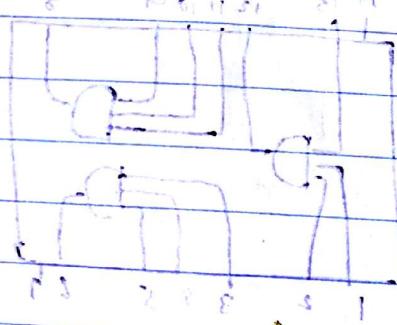
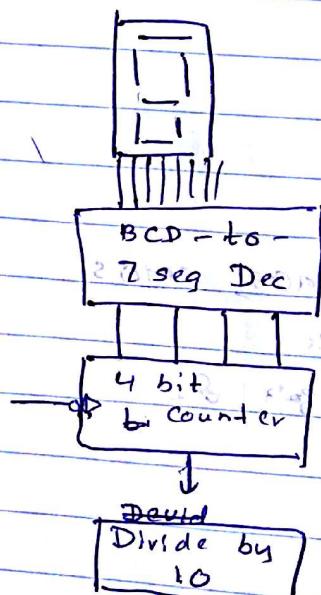


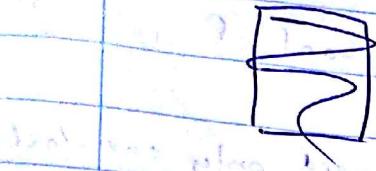
(Dividing into 800)
(Dividing into 80)

The divide by 16 part

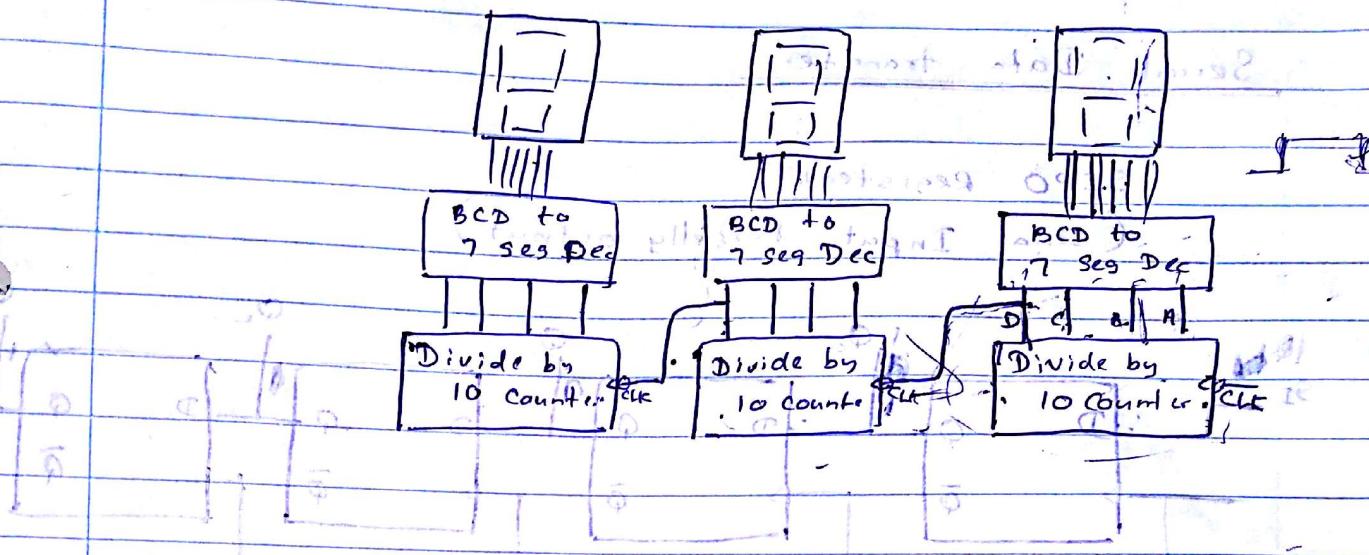


Seven segment display

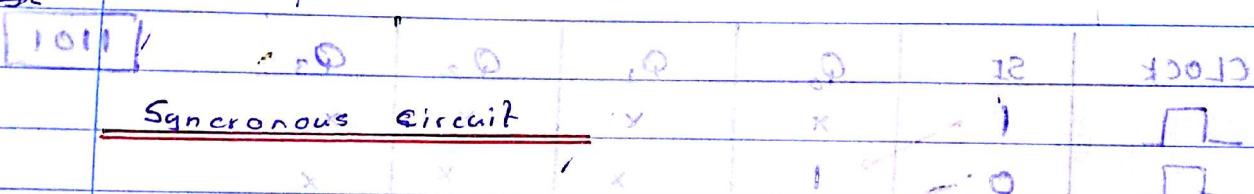




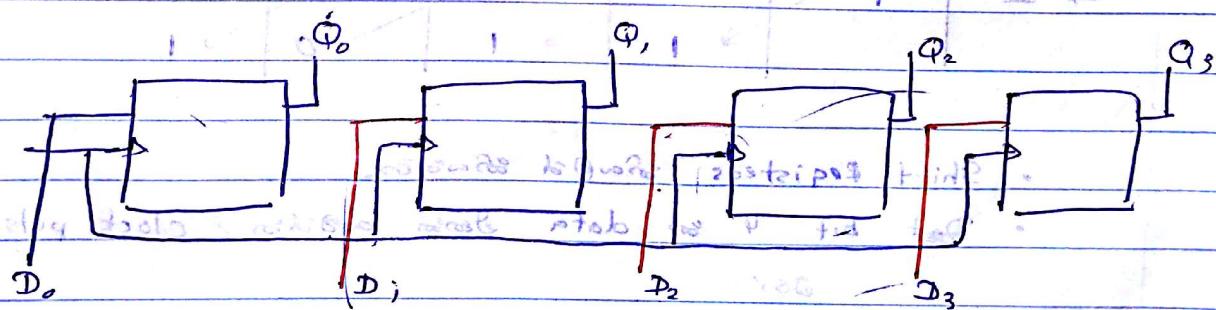
Q. Make a counter counts from 000_8 to 999_{10}



Q. Design a stopwatch which counts from 00:00 to 59:59
min sec min sec



It is used for registers



Step 1 set D_0, D_1, D_2, D_3 inputs

Step 2 clock pulse

Step 3 Q_0, Q_1, Q_2, Q_3 set outputs

Light display program விடைக் குறை store என்கிறோம்

• Flip flop சுதா விபீசனவான் என்று. clock விடை கூறுவது

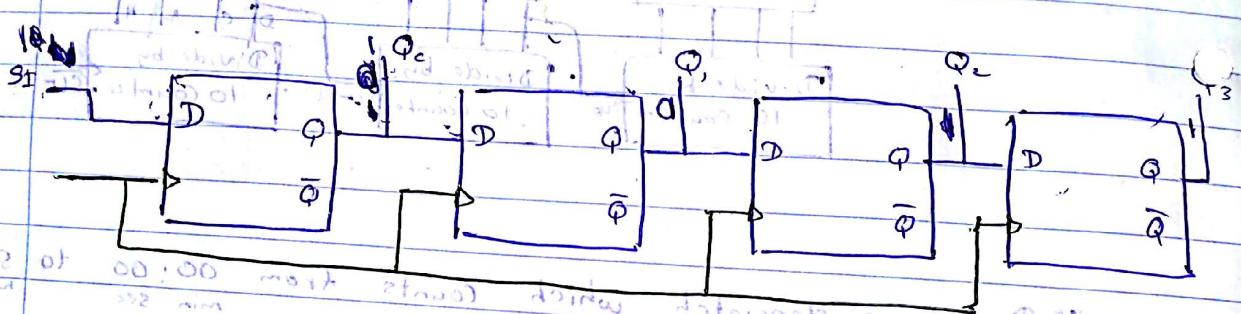
PIPO Registers (Parallel In - Parallelly-out Registers)

- This is the fastest register type why we need only one clock pulse

Serial Data transfer

SIPo Registers

(Serial Input Parallel output)



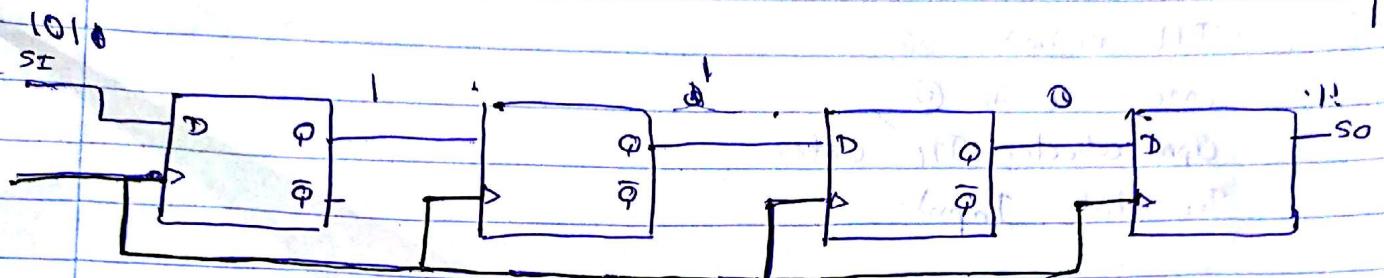
CLOCK	SR	Q_0	Q_1	Q_2	Q_3	1101
1	x	x	x	x	x	
0	1	1	x	x	x	
1	0	x	1	x	x	
1	1	0	1	0	x	
1	1	0	0	1	0	
						1

- Shift Registers என்று கூறுவது.
- Dat bit 4 க்கு data வகை வாங்கு clock pulse 4 x

• SERIAL நிலை PARALLEL நிலை converter என்ற பெயர்

Q. PISO நிலை நிலைகள்

SISO Registers
Serial Input Serial Output



CLOCK SI Q_0 Q_1 Q_2 Q_3



1

.

Q_1

Q_2

Q_3



0

1



1

0

1



1

1

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