Imperial College London

ELEC50010 - Instruction Architectures and Compilers

CPU Coursework by Team 12

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1 CPU

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2 Test bench

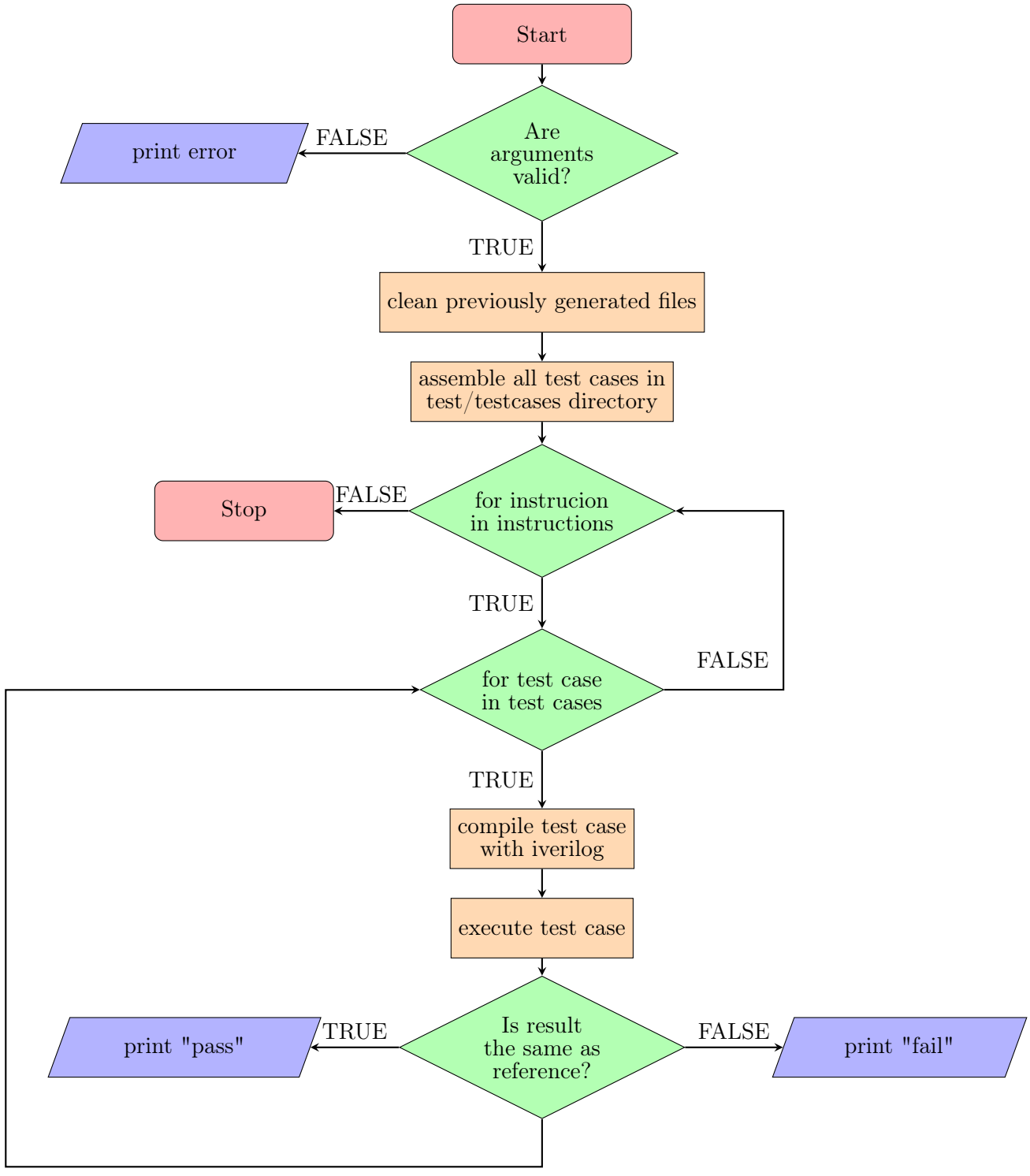
2.1 Test bench Overview

This test bench is designed to be able to carry out test on any cpu that satisfies MIPS1 specification and avalon memory-mapped interface.

The main shell script contains three parts: argument validation, preprocessing on test cases, compilation/execution/comparation of test case on the target cpu.

During argument validation, the main shell script assumes one compulsory argument for source directory of cpu and one optional argument for a specific instruction to test. The shell script would abort either when an invalid source directory or an unsupported instruction is supplied.

Preprocessing of the test cases removes previously generated files if they exist, and generates test cases from ‘readme.md‘ file in each instrucion folder. Each test case contains four files: assembly code, v0 reference, initial content for data section, reference for data section.



2.2 Parser

```
test/
├── RAM_32x64k_avalon.v
├── assembler.sh
├── clear_all.sh
├── compare_result.sh
├── generate_testcases.py
└── generate_testcases.sh
```

```
├── mips_cpu_bus_tb.v
├── test_mips_cpu_bus.sh
├── test_mips_cpu_bus_one_instruction.sh
├── test_mips_cpu_bus_one_testcase.sh
├── test_mips_cpu_bus_real.sh
└── testcases/
    ├── instruction_1
    │   ├── testcase_1
    │   │   ├── testcase.S
    │   │   ├── testcase_data.init
    │   │   ├── testcase_data.ref
    │   │   └── testcase_v0.ref
    │   ├── testcase_2
    │   └── ...
    ├── instruction_2
    └── ...
```

Listing 1: Parser part 1