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`CSE231.14L`

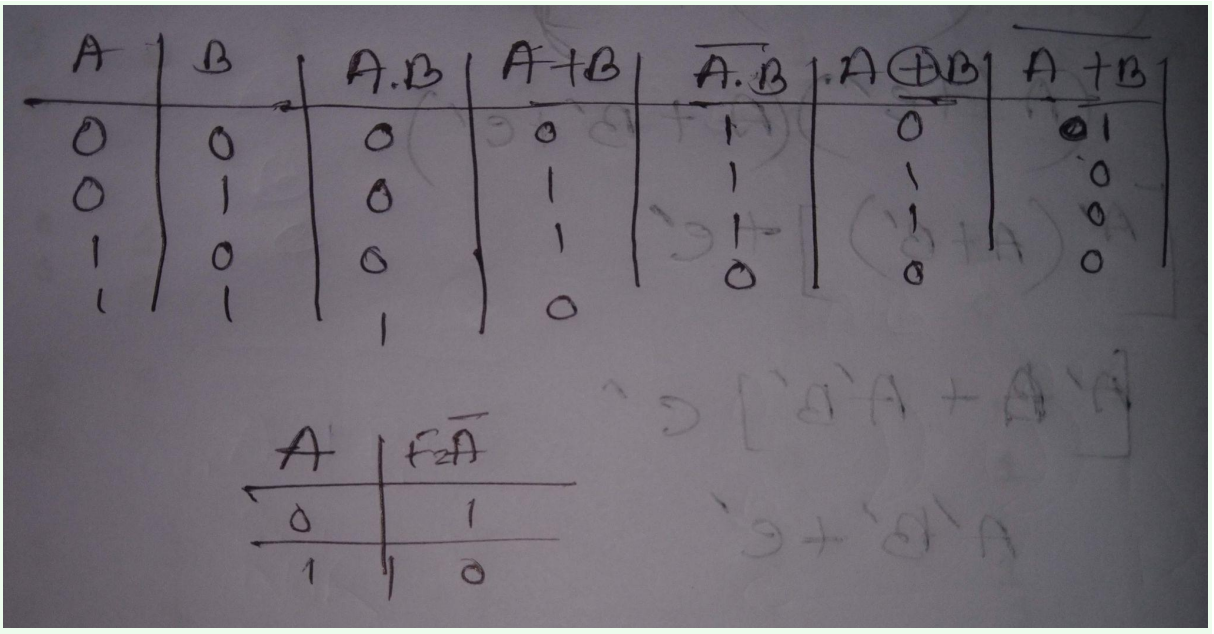
Task 1:

Input $A\ B$	AND $F = A \cdot B$	OR $F = A + B$	NAND $F = \overline{A \cdot B}$	XOR $F = A \oplus B$	NOR $F = \overline{A + B}$
0 0					
0 1					
1 0					
1 1					

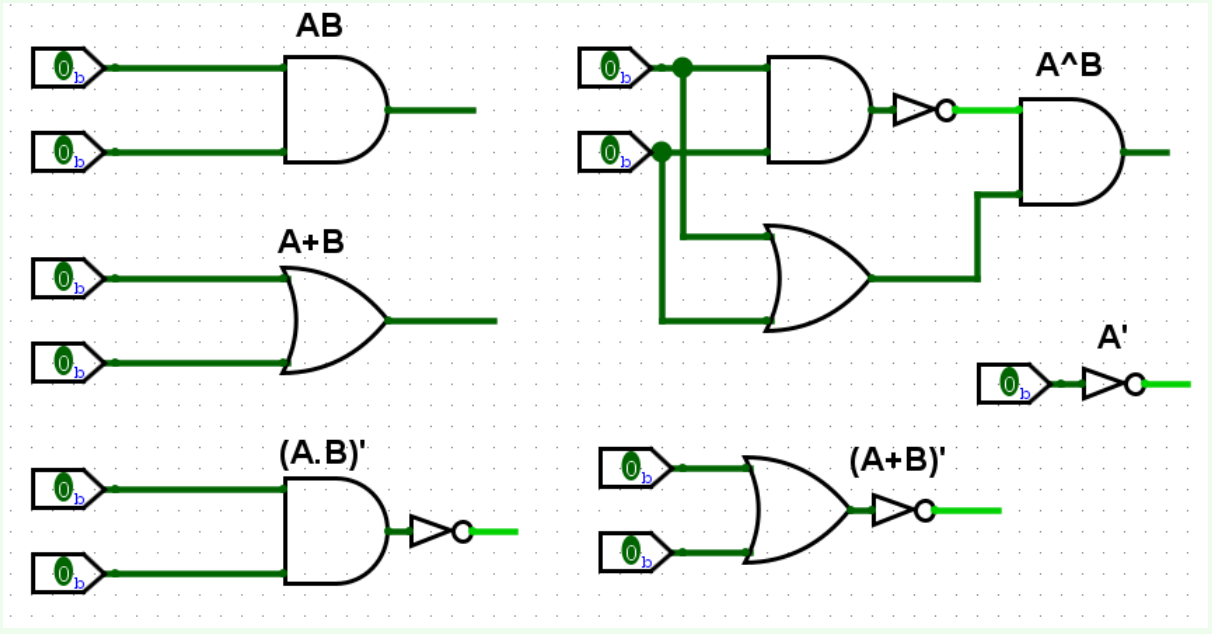
Input A	NOT $F = \overline{A}$
0	
1	

Table D.1 Truth table of logic gates

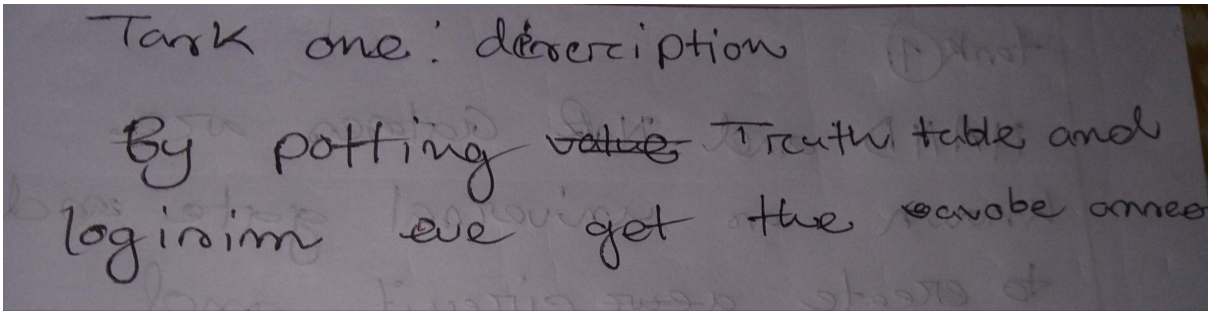
Truth Table



Logisim



Description And Discussion



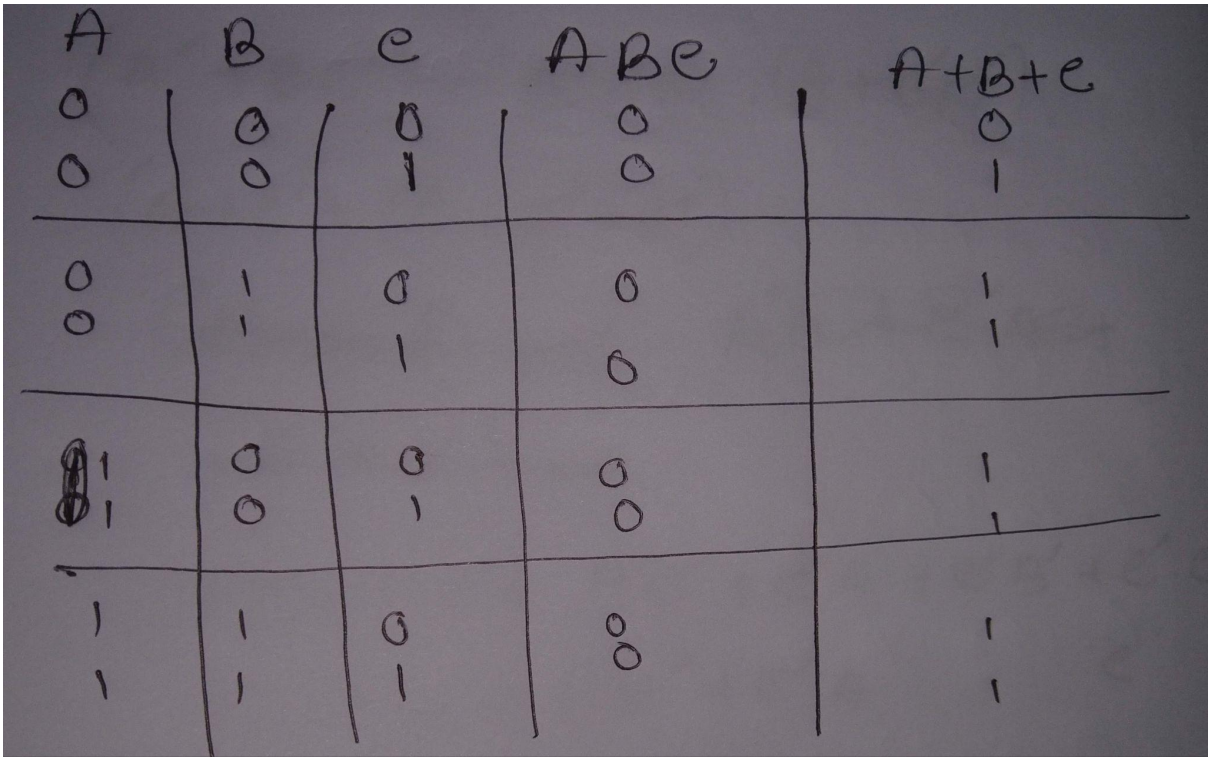
Task 2:

Complete the truth table for the 3-input AND gate in Table D.2.

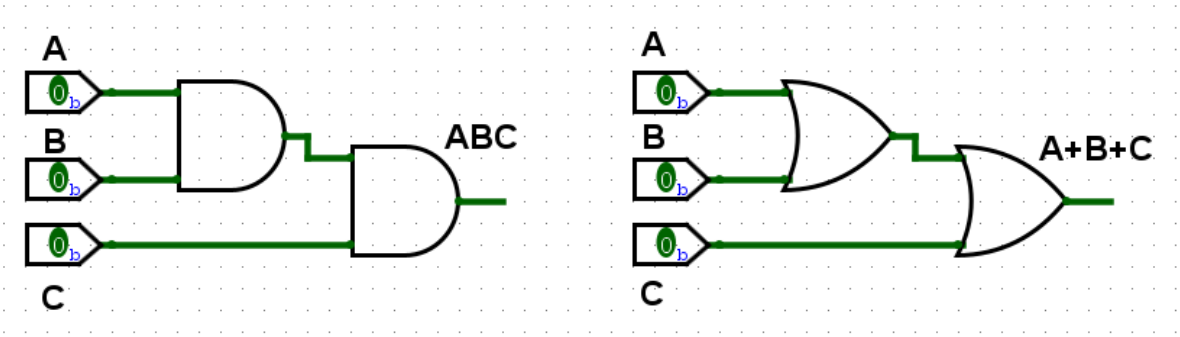
$A\ B\ C$	$F = ABC$	$F = A + B + C$
0 0 0		
0 0 1		
0 1 0		
0 1 1		
1 0 0		
1 0 1		
1 1 0		
1 1 1		

Table D.2 Truth table of 3-input AND and OR

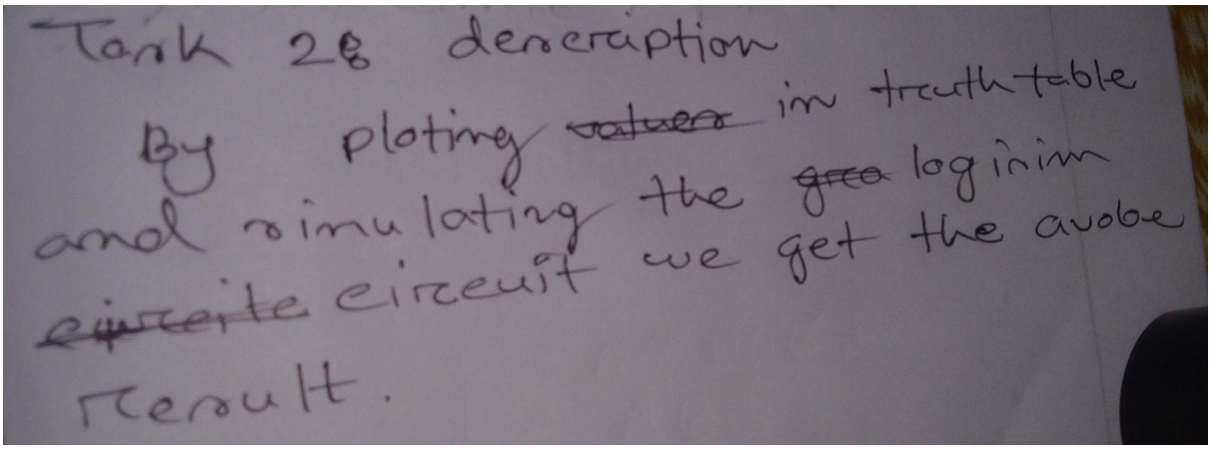
Truth Table



Logisim



Description And Discussion


Task 2& description
By plating ~~values~~ in truth table
and simulating the ~~gate~~ logisim
~~circuit~~ circuit we get the above
result.

task 3:

2. Complete the truth table for the function F in Table D.4.

$A\,B\,C$	$I_1 = A'C$	$I_2 = AB'$	$I_3 = BC$	$F = I_1 + I_2 + I_3$
0 0 0				
0 0 1				
0 1 0				
0 1 1				
1 0 0				
1 0 1				
1 1 0				
1 1 1				

Table D.4 Truth table of logic gates

3. Label the pin numbers for the NOT, AND and OR gates of the function Fin Figure D.3, using the pin configurations in Figure C.2.

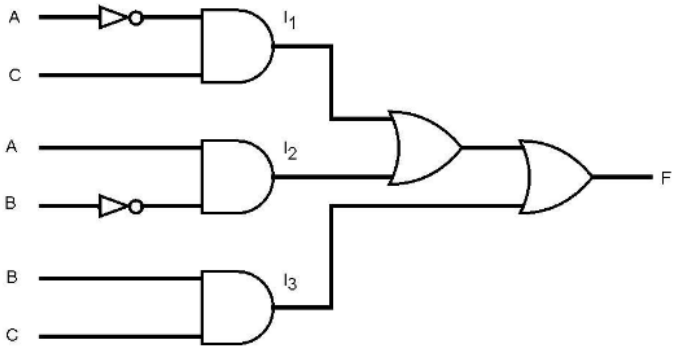
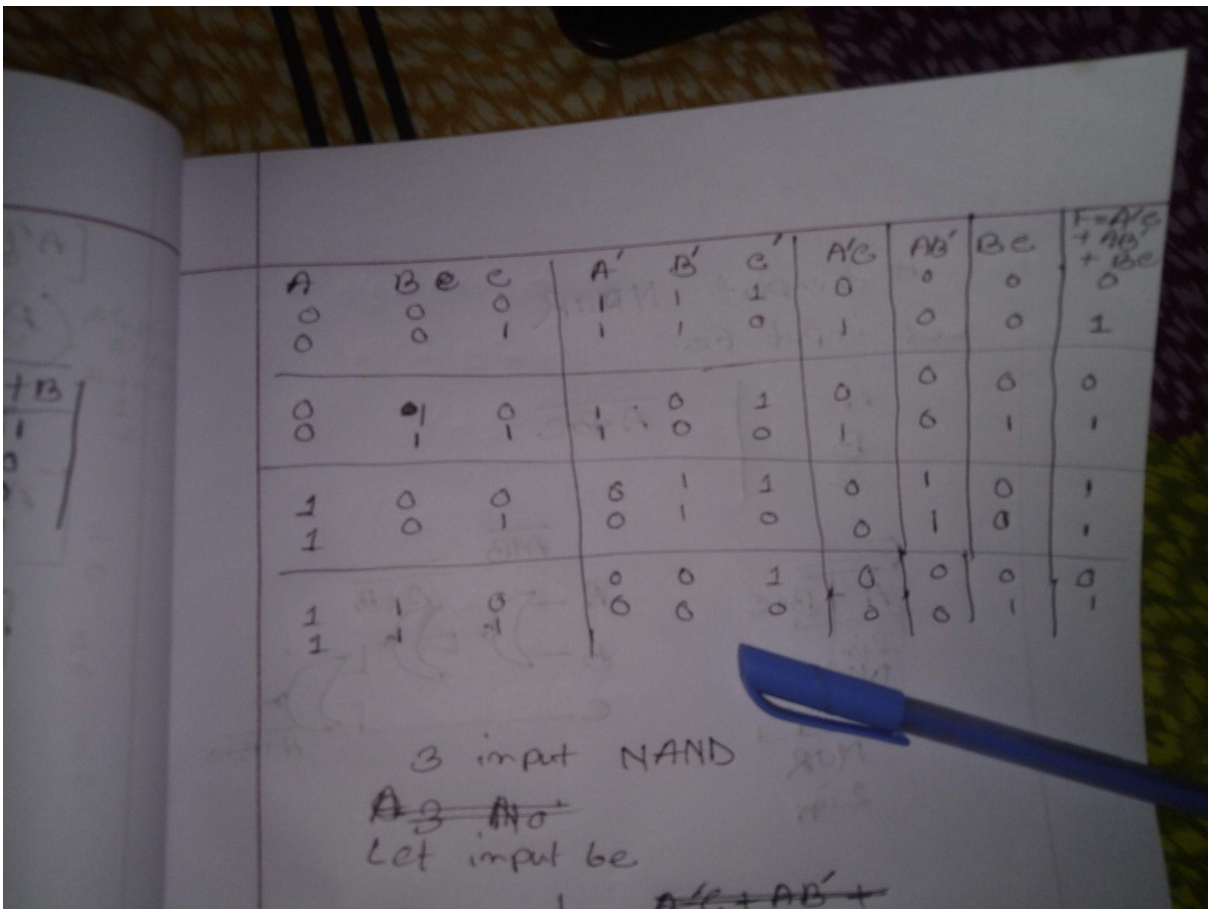


Figure D.3 Circuit diagram for the Boolean function F

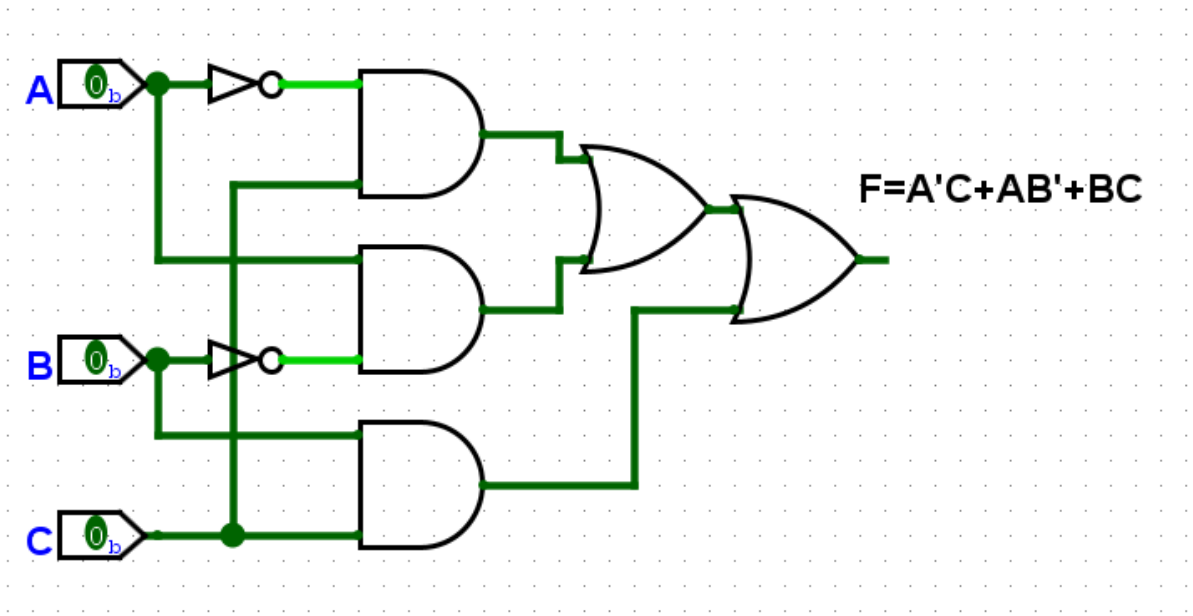
F. Simulation

1. Simulate the combinational logic circuit of Experiment 0 in Logisim and attach the circuit in your lab report, showing only the instance when the input $ABC = 010$.

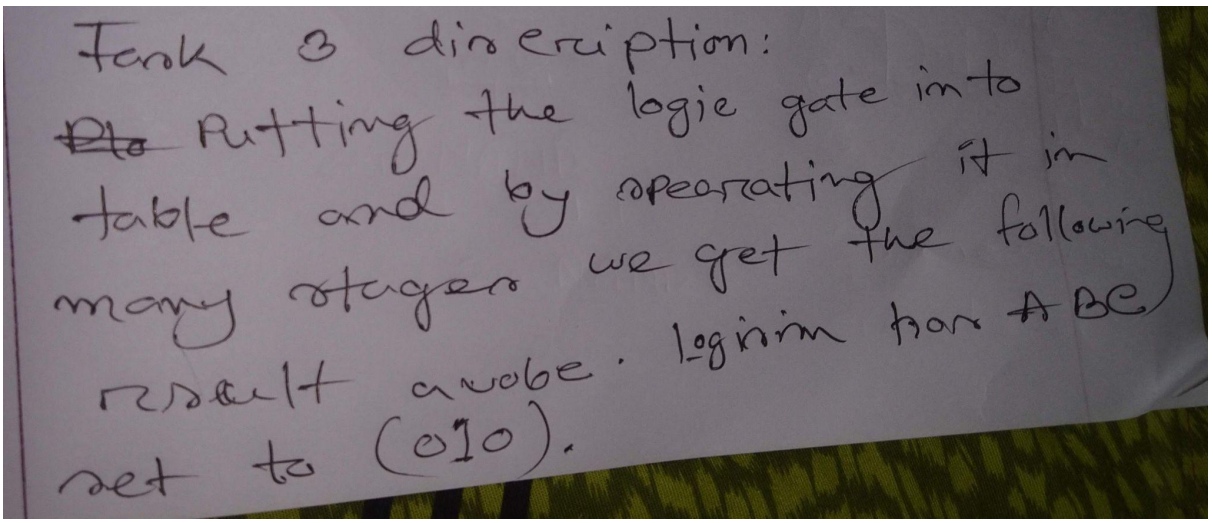
Truth Table



Logisim



Description And Discussion



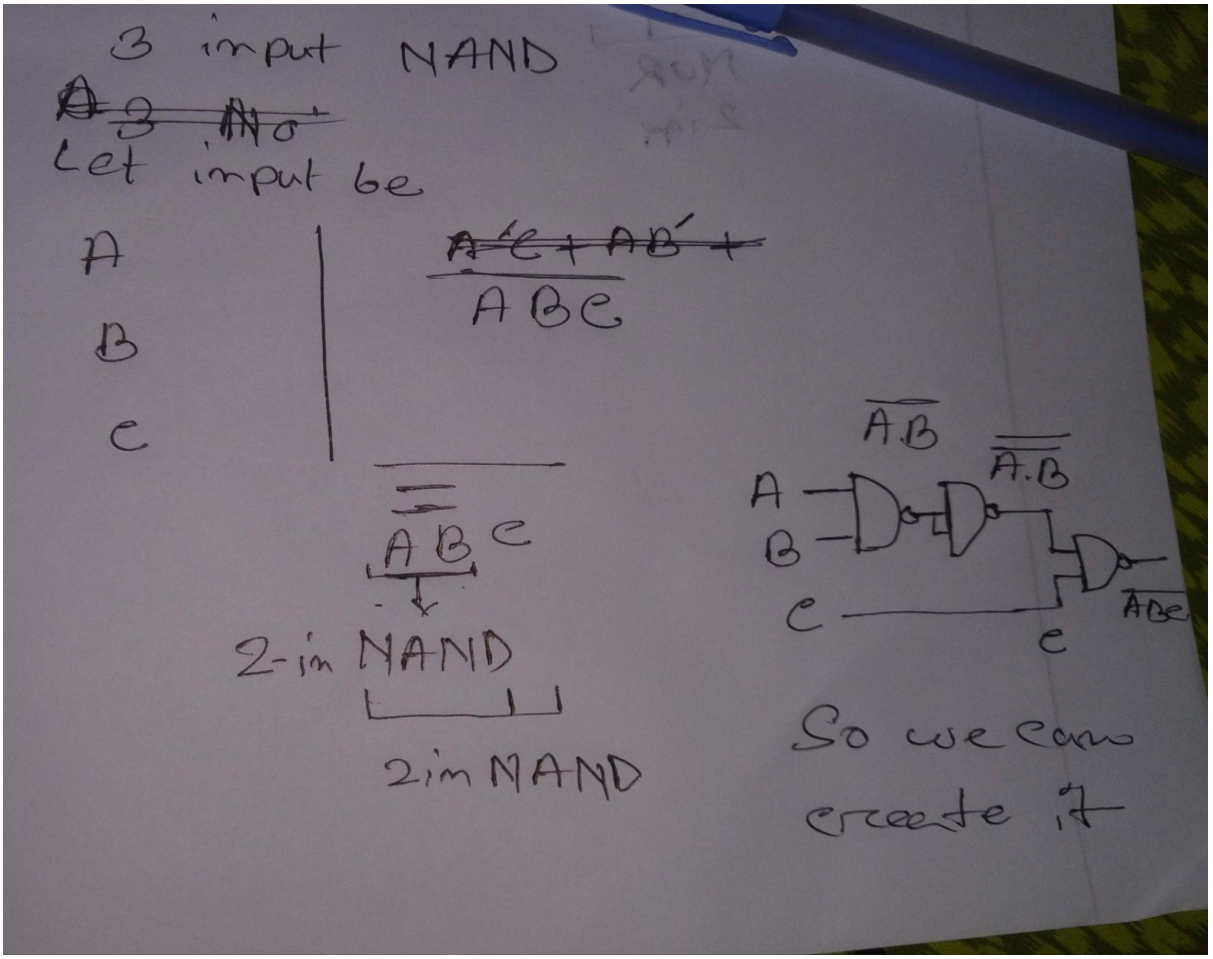
Task 4:

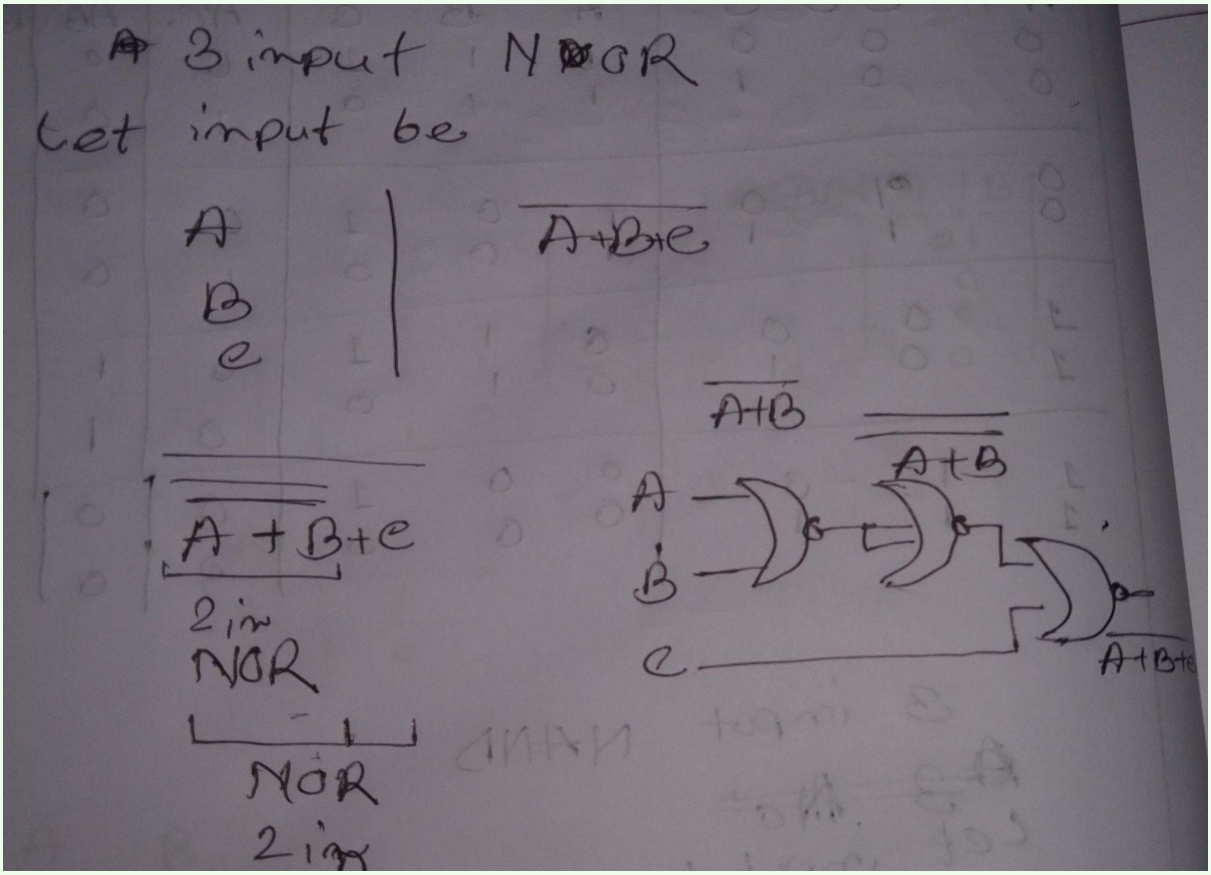
Is it possible to make a 3-input NAND or NOR gate with 2-input NAND or NOR gates? Justify your answer

E. Questions

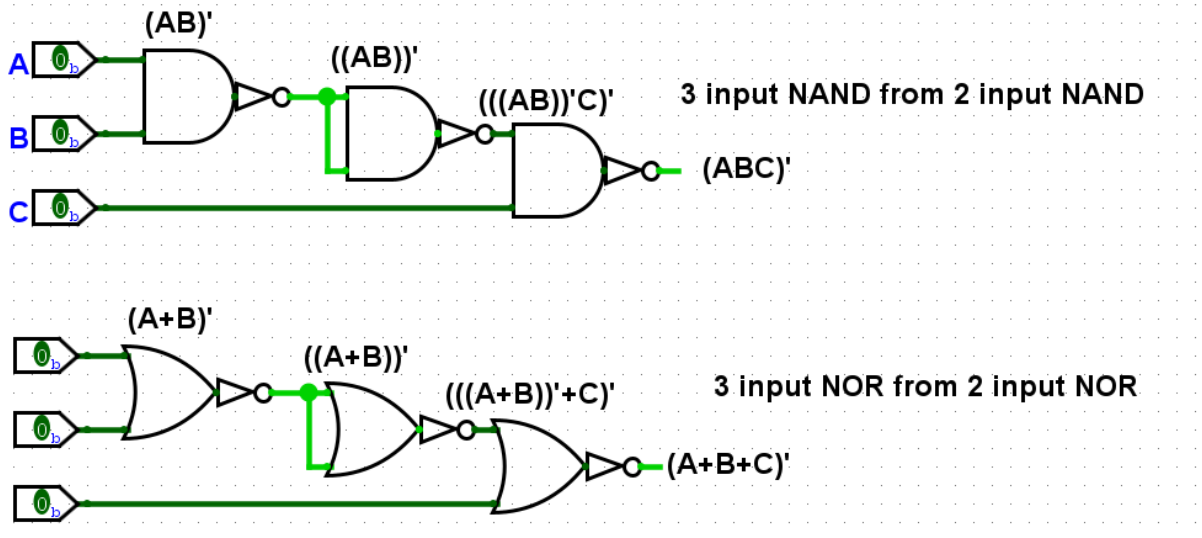
1. Is it possible to make a 3-input NAND or NOR gate with 2-input NAND or NOR gates? Justify your answer.

Proof





Logisim



Description And Discussion

task (4)

NAND and NOR Gates are known as universal gate and to create a circuit and prove it via implenting a 3 input NAND, NOR gate with 2 input NAND, NOR Gate.