Lab 1: Combinational Logic Design

A. Objectives

- Familiarize with the analysis of combinational logic network.
- Learn the implementation of networks using the two canonical forms.
- Devise combinational circuits using universal logic.
- Acquaint with basic binary arithmetic circuits –the half and full adders.

B. Theory

Concise theory pertinent to lab experiments to go here to aid students in performing experiments with minimal supervision
For example, topics for this lab should include definition and steps to:

Analysis of combinational logic design
Min terms and max terms
Canonical Forms
Universal gates – bubble pushing, De Morgan's theorem

C. Experiment 1: Analysis of a Combinational Logic Circuit

C.1. Apparatus

- Trainer Board
- 1 x IC 7411 Triple 3-input AND gates
- 1 x IC 7432 Quadruple 2-input OR gates
- 1 x IC 7404 Hex Inverters (NOT gates)

C.2. Procedure

Input Reference	$A\ B\ C$	F	Min term	Max term
0	0 0 0	0		
1	0 0 1	1		
2	0 1 0	1		
3	0 1 1	0		
4	1 0 0	0		
5	1 0 1	0		
6	1 1 0	1		
7	1 1 1	0		

Table C.1 Truth table to a combinational circuit

1. Write down all the min terms and max terms of three inputs ABC in Table C.1.
2. Write down the function F in 1st and 2nd Canonical Forms in Table C.2.

	Shorthand Notation	Function
1st Canonical Form	$F = \Sigma$	$F =$
2nd Canonical Form	$F = \Pi$	$F =$

Table C.2 1st and 2nd canonical forms of the combinational circuit of Table C.1

3. Draw the circuits in the space provided below, clearly indicating the pin numbers corresponding to the relevant ICs.

1st Canonical Form

2nd Canonical Form

Figure C.1 1st and 2nd canonical circuit diagrams of the combinational circuit of Table C.1

4. Construct the 1st canonical form of the circuit and test it with the truth table.
   i. Connect one min term at a time and check its output.
   ii. Once all min terms have been connected and verified, OR the min terms for the function output.

C.3. Report

Additional report questions/simulations to go here

D. Experiment 2: Universal Gates

D.1. Apparatus

- Trainer Board
- IC 7400 Quadruple 2-input NAND gates

D.2. Procedure

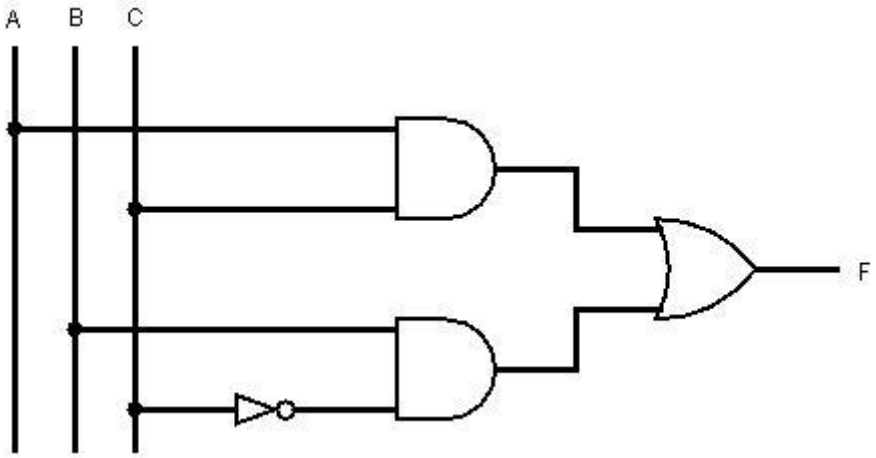

Figure 0.1 A combinational circuit

1. Complete the truth table for the circuit of Figure 0.1 in Table 0.1.

XYZ	$I_1 = AC$	$I_1 = BC'$	F
0 0 0			
0 0 1			
0 1 0			
0 1 1			
1 0 0			
1 0 1			
1 1 0			
1 1 1			

Table 0.1 Truth table of the combination circuit of Figure 0.1

2. Use the space provided below, showing the steps involved, to convert the circuit of Figure 0.1 to a universal (NAND) gate circuit. Convert the inverter to a NAND equivalent as well.
3. Label the pin numbers of the appropriate ICs in step 2 of Figure 0.2.
4. Construct the universal gate circuit in Figure 0.2, checking the output of each NAND gate independently before connecting the entire circuit together.
5. Validate the universal gate circuit using Table 0.1.

Step 1

Step 2

Figure 0.2 Universal (NAND) gate implementation of the circuit of Figure 0.2