North South University

Mid-Term Examination, Fall 2021

Department of Electrical and Computer Engineering

CSE 231: Digital Logic Design

Total Marks: 20 **Duration : 1 Hour**

Q1a Draw a circuit for showing the operation 3-1. (4)

Q1b Show the circuit configuration for faster addition of 7+4. (4)

Q1c Mention the general equation of sum and carry of a half adder. (2)

Q2a A small process-control computer uses hexadecimal codes to represent its 16-bit memory addresses. (2)

(a) How many hex digits are required?

(b) What is the range of addresses in hex?

(c) How many memory locations are there?

Q2b For a 5 bit number, how many bits are required, how many bits are unused and what are the maximum and minimum numbers that can be represented in 1's complement and 2's complement system. (3)

Q2c For f(a,b,Q,G) = $\sum$ (0,3,5,7,10,11,12,13,14,15) ,realize a simplified circuit. (4)

Q2d Convert 9 into grey code and BCD code. (1)