

# \*\*Md. Ishtiaq Ahamed Fahim 2012518642\*\*  
`CSE231.14L`

## Task 1:

Input $A\ B$	AND $F = A \cdot B$	OR $F = A + B$	NAND $F = \overline{A \cdot B}$	XOR $F = A \oplus B$	NOR $F = \overline{A + B}$
0 0					
0 1					
1 0					
1 1					

Input $A$	NOT $F = \overline{A}$
0	
1	

Table D.1 Truth table of logic gates

Truth Table

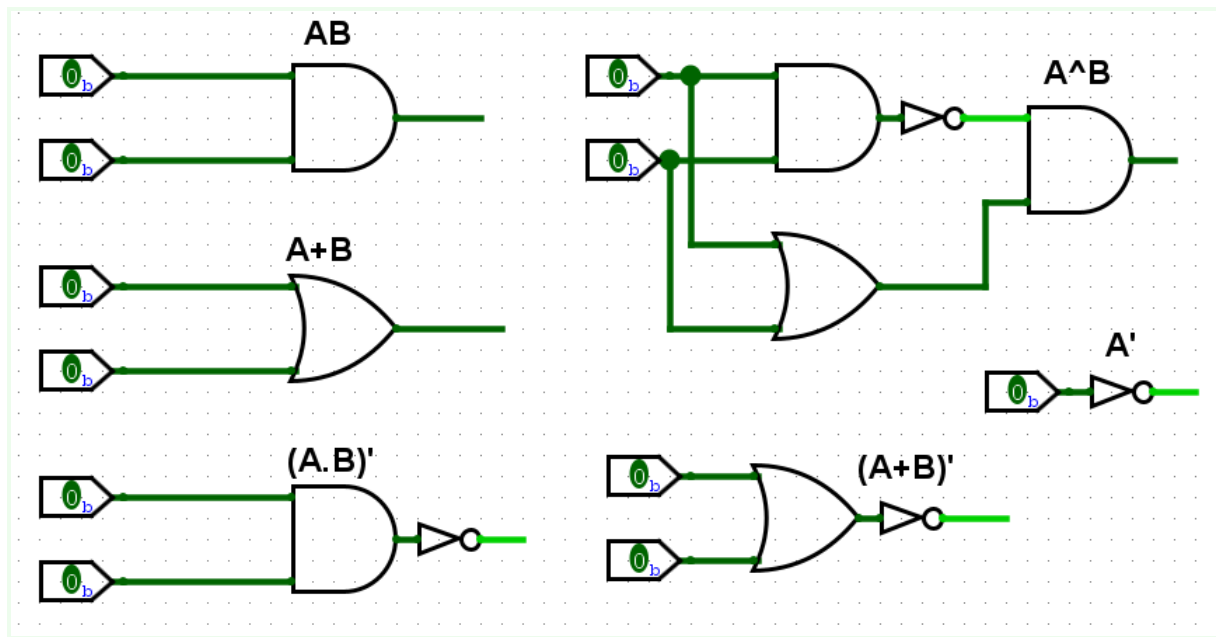
The image shows a handwritten truth table for logic gates and a Karnaugh map for the NOT gate. The truth table has columns for inputs A and B, and outputs for AND (A.B), OR (A+B), NAND (A.B), XOR (A⊕B), and NOR (A+B). The Karnaugh map shows the output F for the NOT gate (F = Ā) for inputs A = 0 and A = 1.

A	B	A.B	A+B	A.B	A⊕B	A+B
0	0	0	0	1	0	1
0	1	0	1	1	1	0
1	0	0	1	1	1	0
1	1	1	1	0	0	0

A	F = Ā
0	1
1	0

Logisim



Description And Discussion

Task one: description  
 By putting value truth table and  
 logicism we get the above ones

## Task 2:

Complete the truth table for the 3-input AND gate in Table D.2.

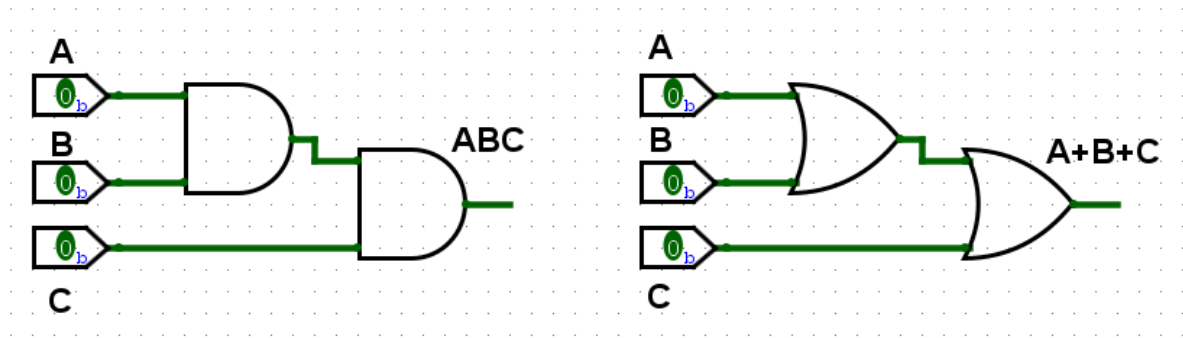
<i>A B C</i>	<i>F = ABC</i>	<i>F = A + B + C</i>
0 0 0		
0 0 1		
0 1 0		
0 1 1		
1 0 0		
1 0 1		
1 1 0		
1 1 1		

Table D.2 Truth table of 3-input AND and OR

Truth Table

<i>A</i>	<i>B</i>	<i>C</i>	<i>A B C</i>	<i>A + B + C</i>
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Logisim



Description And Discussion

Task 28 description  
 By plotting ~~values~~ in truth table  
 and simulating the ~~gate~~ logic in  
~~circuit~~ circuit we get the above  
 result.

## task 3:

- Complete the truth table for the function  $F$  in Table D.4.

$A B C$	$I_1 = A'C$	$I_2 = AB'$	$I_3 = BC$	$F = I_1 + I_2 + I_3$
0 0 0				
0 0 1				
0 1 0				
0 1 1				
1 0 0				
1 0 1				
1 1 0				
1 1 1				

Table D.4 Truth table of logic gates

- Label the pin numbers for the NOT, AND and OR gates of the function  $F$  in Figure D.3, using the pin configurations in Figure C.2.

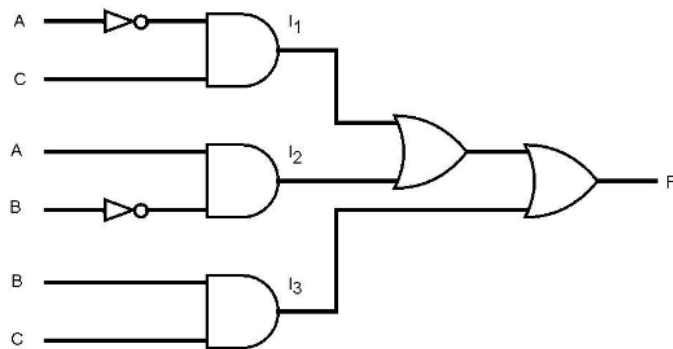


Figure D.3 Circuit diagram for the Boolean function  $F$

## F. Simulation

- Simulate the combinational logic circuit of Experiment 0 in Logisim and attach the circuit in your lab report, showing only the instance when the input  $ABC = 010$ .

Truth Table

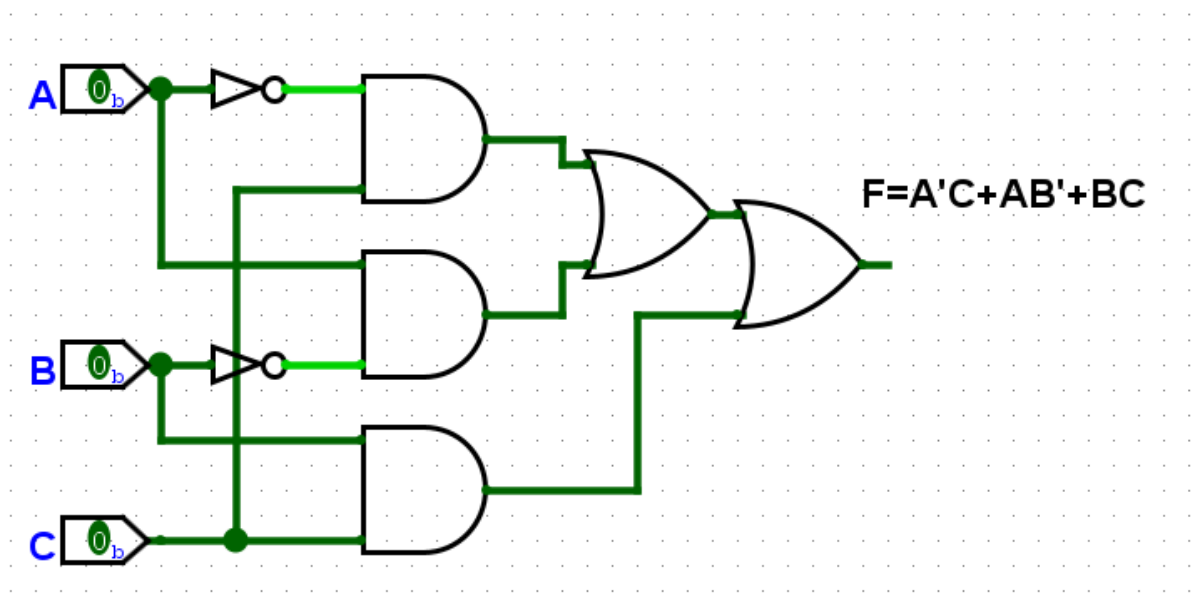
A	B	C	A'	B'	C'	A'B	AB'	BC	F = A'C + AB' + BC
0	0	0	1	1	1	0	0	0	1
0	0	1	1	1	0	1	0	0	1
0	1	0	1	0	1	0	0	0	0
0	1	1	1	0	0	1	0	1	1
1	0	0	0	1	1	0	1	0	1
1	0	1	0	1	0	0	1	0	1
1	1	0	0	0	1	0	0	0	0
1	1	1	0	0	0	0	0	1	1

3 input NAND

Let input be

$F = A'C + AB' + BC$

Logisim



Description And Discussion



Task 3 description:  
~~Put~~ Putting the logic gate into  
 table and by operating it in  
 many stages we get the following  
 result above. logic has ABC  
 set to (010).

#### ## Task 4:

Is it possible to make a 3-input NAND or NOR gate with 2-input NAND or NOR gates? Justify your answer

#### E. Questions

1. Is it possible to make a 3-input NAND or NOR gate with 2-input NAND or NOR gates? Justify your answer.

Proof

3 input NAND

~~A B C~~  
 Let input be

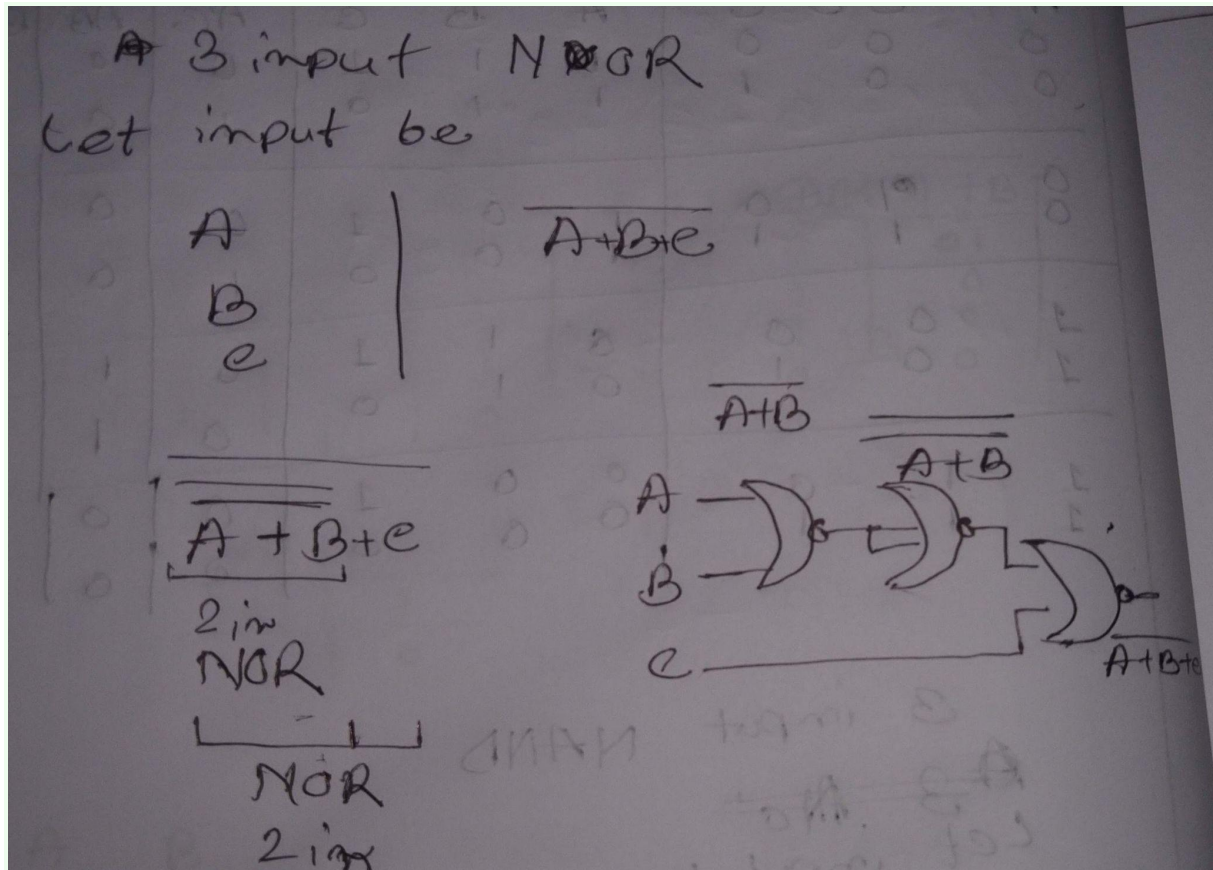
A	<del><math>A'C + AB' +</math></del>
B	$ABC$
C	

$\overline{ABC}$

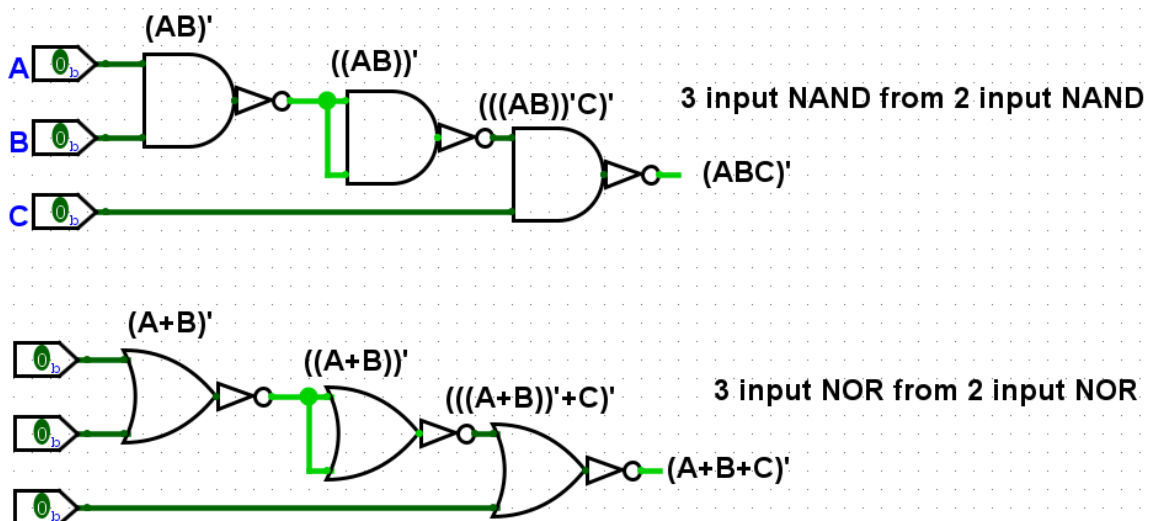
2-in NAND

2-in NAND

So we can create it



Logisim



Description And Discussion



Task (4)

NAND and NOR Gates are known as universal gates and to create a circuit and prove it via implementing a 3 input NAND, NOR gate with 2 input NAND, NOR gate.