

**Lab Manual**

Department of Electrical and Computer Engineering

School of Engineering and Physical Sciences

North South University, Bashundhara, Dhaka-1229, Bangladesh

**Experiment No: 1****Experiment Name: Design of a 2-bit Logic unit.****Introduction:**

In this experiment you will construct a 2-bit logic unit which is actually a part of an ALU. This logic unit will have 4 micro-operations which are AND, OR, XOR and NOT operations. Logic micro operations are very useful for manipulating individual bits or a portion of a word stored in a register. They can be used to change bit values, delete a group of bits or insert a new set of bits in a register. As we are going to design a 2-bit logic unit, we will have two outputs which is one output for each of the 2 bits.

**Equipments:**

Trainer board

IC 7404, 7408, 7432, 7486, 74F153

Wires for connection.

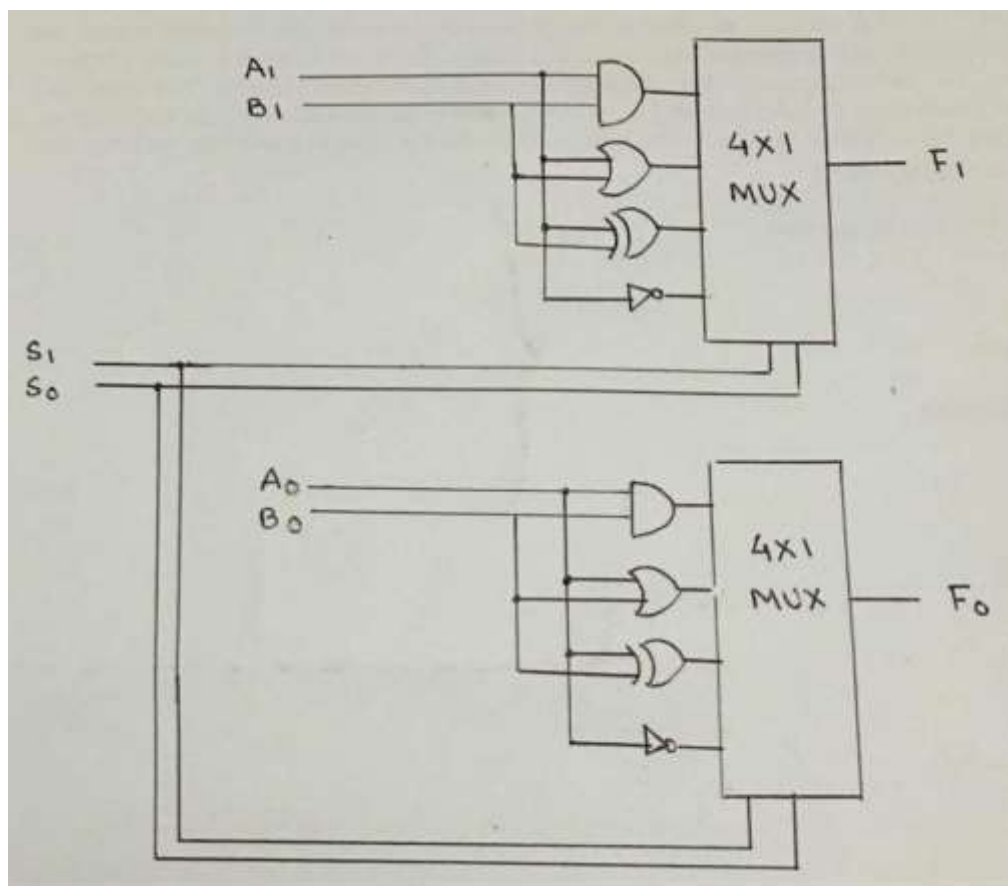
**Truth Table:**

Complete the Truth Table according to your theoretical knowledge.

A1	A0	B1	B0	AND1	AND0	OR1	OR0	XOR1	XOR0	NOT A1	NOT A0
0	0	0	0								
0	0	0	1								
0	0	1	0								
0	0	1	1								
0	1	0	0								
0	1	0	1								
0	1	1	0								
0	1	1	1								
1	0	0	0								

1	0	0	1									
1	0	1	0									
1	0	1	1									
1	1	0	0									
1	1	0	1									
1	1	1	0									
1	1	1	1									

Logic Diagram:



**Procedure: (hardware)**

- 1) Place the ICs on the trainer board.
- 2) Connect  $V_{cc}$  and ground to the respective pins of IC.
- 3) Connect the inputs with the switches and the outputs with LEDs.
- 4) Apply various combinations of inputs and observe the outputs.
- 5) Verify the experimental outputs with the Truth Table.

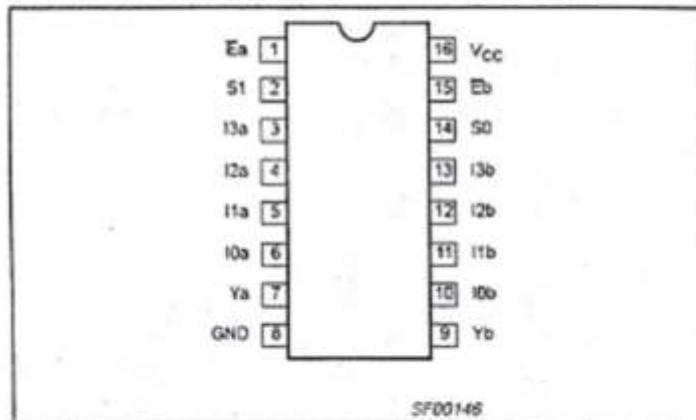
**Assignment/Task:**

1. Implement the circuit in Logisim. **Submit logisim (.circ) file + the screenshots of the circuits** within the given time by your lab instructor.
2. **Prepare and submit the lab report by the end of the class individually.**

**\*\*Plagiarism and late submission will not be acceptable.**

**EEE336/CSE232 LAB**  
**Dual 4x1 Multiplexer 74F153**  
**Data Sheet**

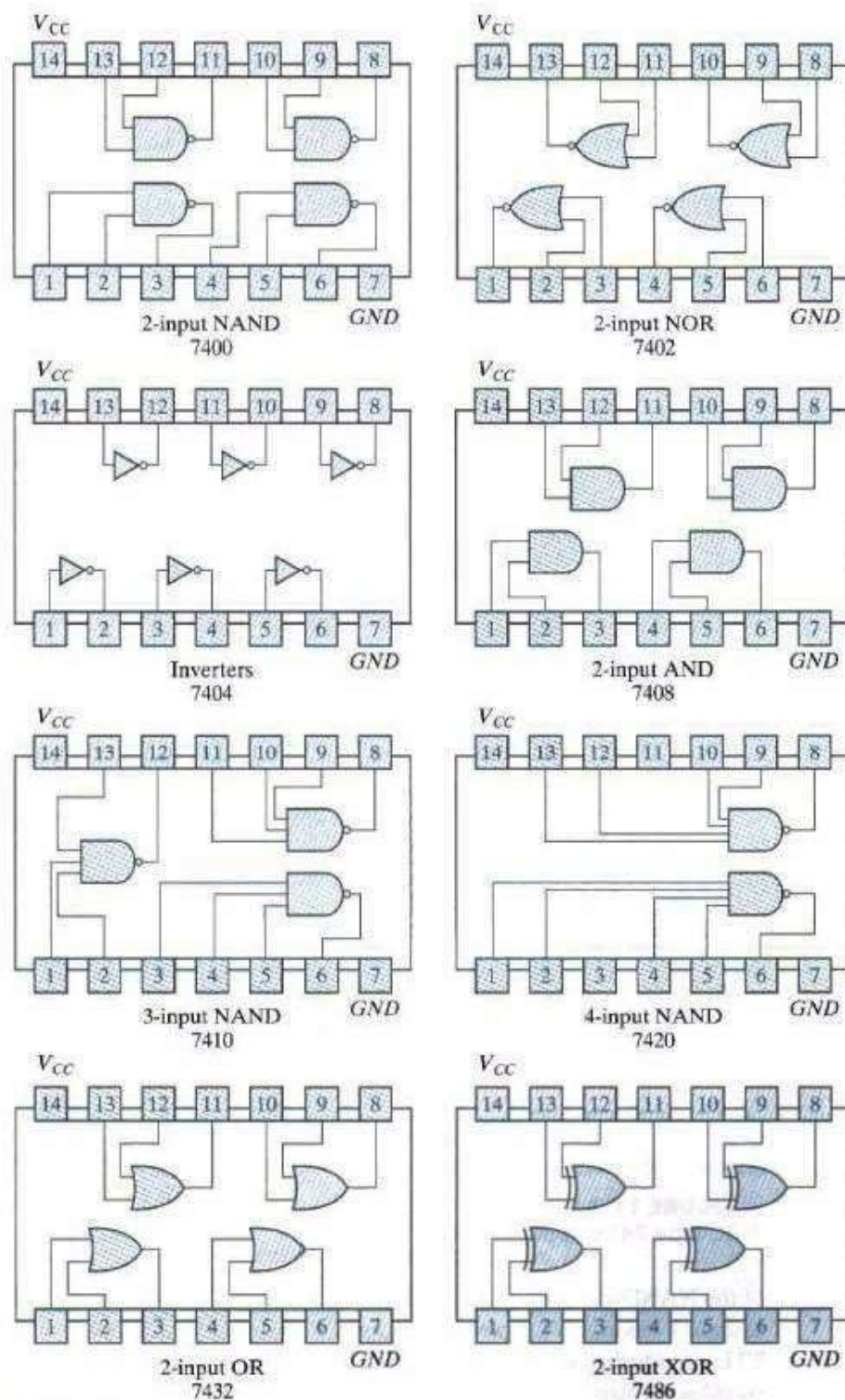
**PIN CONFIGURATION**



**INPUT AND OUTPUT LOADING AND FAN-OUT TABLE**

PINS	DESCRIPTION
I0a – I3a	Port A data inputs
I0b – I3b	Port B data inputs
S0, S1	Common Select inputs
Ea	Port A Enable input (active Low)
Eb	Port B Enable input (active Low)
Ya, Yb	Port A, B data outputs

## Section 11.1 Introduction to Experiments 513



**FIGURE 11.1**  
Digital gates in IC packages with identification numbers and pin assignments