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LAB-3

Friday, 4 March 2022 4:52 PM

Spring 2022
EEE/ETE 141L
Electrical Circuits-I Lab(Sec-10)
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Instructor: Farhana Atuyar Saleh

Lab No.: 03

Date of Performance : 02/03/2022 Date of Submission : 09/03/2022	**Name:** 1. **Bushra Hossain** 2. **Md. Ishtiaq Ahamed Fahim** 3. **Tajrian Al Israq** **ID:** 1. **2031346642** 2. **2012518642** 3. **2021536643**

Experiment 03: Loading effect of Voltage Divider circuit.

Objective:

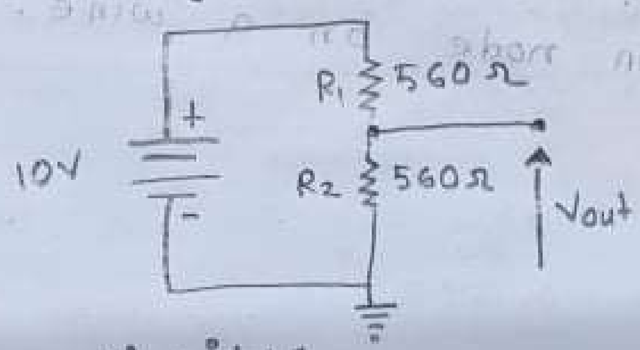
① We have to analyze how the voltage divider circuit behaves when there is no load resistance connected.

② We have to evaluate the performance of voltage divider circuit due to loading.

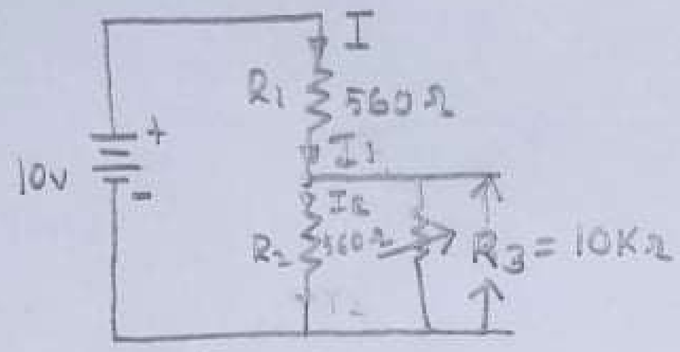
List of Equipment:

① Trainer Board
② DMM
③ 2x 560 Ω resistors
④ 1x (0-10 kΩ) variable resistor
⑤ Multisim.

Circuit Diagram:



circuit: 1

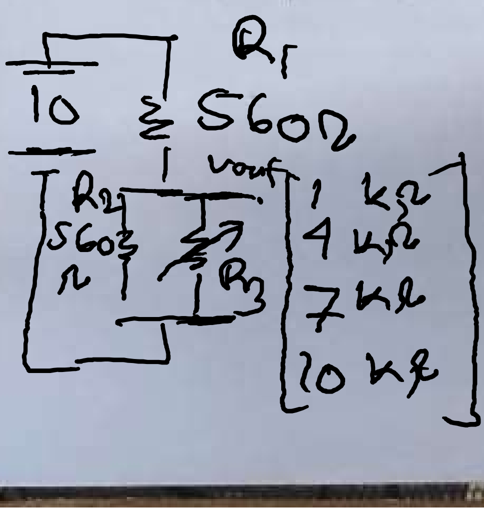


Circuit : 2

Data Table :

Table 1 :

RL	Vout [Measured]	Vout [calculated]	% Error
No resistor	5V	5V	0 %
1K	3.906 v	3.91 V	0.1023%
4K	4.673 V	4.67 V	0.0642%
7K	4.808 V	4.81 V	0.04158%
10K	4.864 V	4.86	0.0823%



$$V_{out} = \frac{R_2 \parallel R_3}{R_1 + (R_2 \parallel R_3)} \times E$$

$$\text{error} = \left| \frac{\text{theoretical} - \text{experimental}}{\text{theoretical value}} \right| \times 100\%$$

Result :

$$V_{out\ \text{No Resistors}} = \frac{560}{560+560} \times 10 \approx 5\text{ V}$$

$$\text{error} = \left| \frac{5-5}{5} \right| \times 100\% = 0\%$$

$$V_{out\ 1k} = \frac{(560^{-1}+1000^{-1})^{-1}}{560+(560^{-1}+1000^{-1})^{-1}} \times 10\text{ V} \approx 3.91\text{ V}$$

$$\text{error} = \left| \frac{3.91-3.906}{3.91} \right| \times 100\% = 0.1023\%$$

$$V_{out\ 4k} = \frac{(560^{-1}+4000^{-1})^{-1}}{560+(560^{-1}+4000^{-1})^{-1}} \times 10\text{ V} \approx 4.67\text{ V}$$

$$\text{error} = \left| \frac{4.67-4.673}{4.67} \right| \times 100\% = 0.0642\%$$

$$V_{out\ 7k} = \frac{(560^{-1}+7000^{-1})^{-1}}{560+(560^{-1}+7000^{-1})^{-1}} \times 10\text{ V} \approx 4.81\text{ V}$$

$$\text{error} = \left| \frac{4.81-4.808}{4.81} \right| \times 100\% = 0.4518\ \%$$

$$V_{out\ 10k} = \frac{(560^{-1}+10000^{-1})^{-1}}{560+(560^{-1} \ldots)^{-1}} \times 10 = 4.86\text{ V}$$

$$V_{out\,10k} = \frac{(\cdots)}{560+\left(560^{-1}+10000^{-1}\right)^{-1}} \times 10 = 4.86\,V$$

$$\text{error} = \left|\frac{4.86-4.864}{4.86}\right| \times 100\%$$

$$= 0.0823\%$$

Question / Answer:

① Explain the loading effect of your circuit (i.e explain how does your Vout vary with increasing Load resistor)

Ans: Initially the Vout was 5 V, total resistance was 1120 Ω and current flow was 8.92 mA, when there was no load register.

From the table-1 when load resistor is 1K the Vout is 3.91 V and finally when the Load resistor is 10K Vout become 4.86 V

So, as the value of load register is increasing the value of Vout is also increasing.

Total Resistance, $R_T = R_1 + (R_2 \parallel R_3)$
After adding load 10KΩ
$= 560 + 530\ \Omega$
$= 1090\ \Omega$

So after adding 10kΩ loading resistor, total $I_T = \frac{10 \times 1000}{1090}$

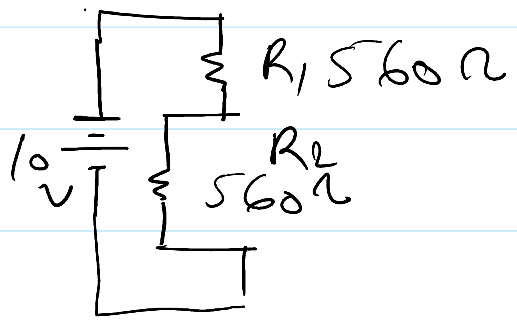
$= 9.174 \text{ mA}$

So,

After adding loading resister the total resister decreases and so current flow increases.

2. Showing all steps in details, theoretically calculate the value of Vout for each load
resistor.

for No Resistor



general form,

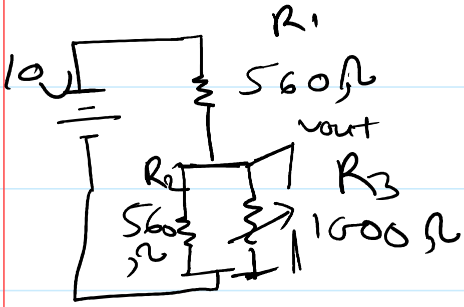
$$V_{out} = \frac{R_1}{R_1 + R_2} \times V$$

$$V_{out\,\text{no res}} = \frac{560}{560 + 560} \times 10\,V = 5\,V$$

The general formula is,

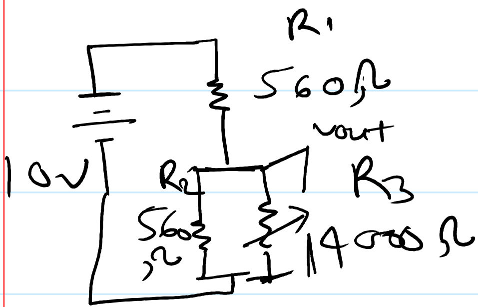
$$V_{out} = \frac{(R_2 \parallel R_3)}{R_1 + (R_2 \parallel R_3)} V$$

for 1K loading



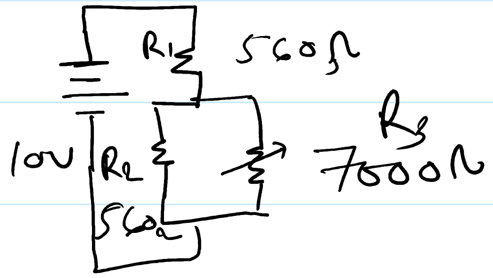
$$V_{out_{1K}} = \frac{(560^{-1}+1000^{-1})^{-1}}{560+(560^{-1}+1000^{-1})^{-1}} \times 10 \approx 3.91V$$

for 4K loading



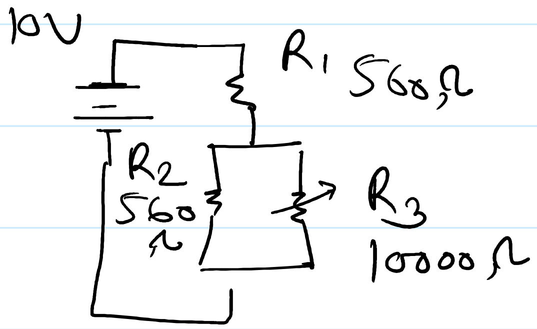
$$V_{out_{1K}} = \frac{(560^{-1}+4000^{-1})^{-1}}{560+(560^{-1}+4000^{-1})^{-1}} \times 10 \approx 4.67V$$

for 7K loading,



$$V_{out} = \frac{(560^{-1}+7000^{-1})^{-1}}{560+(560^{-1}+7000^{-1})^{-1}} \times 10V \approx 4.81V$$

for 10K loading,



$$V_{out} = \frac{(560^{-1}+10000^{-1})^{-1}}{560+(560^{-1}+10000^{-1})^{-1}} \times 10V \approx 4.86V$$

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3. Comparing the theoretical data to the experimental data, comment how far the loading effect of your circuit supports the theory.

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If we put loading in a circuit in parrall The total resistence decreases.

As we know,

$$V = IR$$

$$I = \frac{V}{R}$$ [As Voltage is constant In a battery]

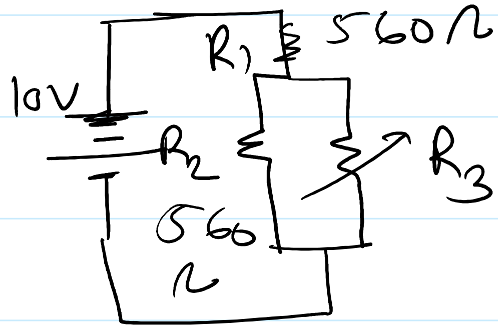
$$I \propto \frac{1}{R}$$

As a result if Resistence decreses the total current flow would increase vice versa.

This is also reflected in the experiment, comparing theoretical values and expermental value we come to same conclusion.

R_L 560Ω

$V = 10V,$



$V = IR$

$I = \frac{V}{R}$

for no resistance,

$R_{eq\,(\text{no res})} = 560 + 560 = 1120\,\Omega$

$I = \frac{V}{R_{eq\,(\text{no res})}} = \frac{10V}{1120\,\Omega} = 0.0089A$

This would work as our base calculation.

for load we know

$R_{eq} = R_1 + (R_2 \parallel R_3)$

1kΩ load,

$$R_{eq(1k)} = 560 + (560^{-1} + 1000^{-1})^{-1}$$
$$= 918.97\Omega$$

$$I_{1k} = \frac{V}{R_{eq(1k)}} = \frac{10}{918.97} = 0.0108\ A$$

$\downarrow R_{eq}$ $\uparrow I$ [compared to no extra load]

An voltage drop on parallel restence
Overall Amp increases.

for 4kΩ load

$$R_{eq(4k)} = 560 + (560^{-1} + 4000^{-1})^{-1}$$
$$= 1051.2$$

$$I_{4k} = \frac{V}{R_{eq}} = \frac{10}{1051.2} = 9.5 \times 10^{-3} A$$

$\downarrow R_{eq}$ $\uparrow I$ [compared to no extra load]

7kΩ load,

$$R_{eq(7k)} = 560 + (560^{-1} + 7000^{-1})^{-1}$$
$$= 1078.5\ V$$

$$I_{7k} = \frac{V}{R_{eq}} = \frac{10}{1078.5} = 9.2 \times 10^{-3} A$$

$\downarrow R_{eq}$ $\uparrow I$ [compared to no extra load]

10kΩ load,

$$R_{eq(10k)} = 560 + (560^{-1} + 10000^{-1})^{-1}$$
$$= 1090.3\ \Omega$$

$$I_{10k} = \frac{V}{R_{eq(10k)}} = \frac{10}{1090.3} = 9.1 \times 10^{-3} A$$

$\downarrow R_{eq}$ $\uparrow I$ [compared to no extra load]

So we can say for sure
As Total Restence decreses
voltage on the load drops
Result in more current flow
overall on the circuit.

Discussion:

Form this lab we can learn
by adding load in parrall we can
obsereve voltage drop and current
flow increase as Total resistence
drops. Both theoratical and experimental
data show the same result.

As its lab on multisim software

There is no error that might have been arrised.

Both multisim and load effect has the same result. As it's software Based lab we don't have flaws That might have arrived form accuracy problem lose connection human error, or on DMM, cables, breadboard connection etc.