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ATLASpix3: A high voltage CMOS sensor chip designed for ATLAS Inner Tracker

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ATLASpix3 is a 2×2 cm^2 high voltage CMOS sensor chip designed to meet the specifications of outer layers of ATLAS inner tracker. It is compatible with the hybrid pixel sensor ASIC RD53A in terms of electronic interface and geometry. ATLASpix3 is a depleted monolithic CMOS pixel detector which allows the construction of quad modules of the same size as that of hybrid sensors. The readout scheme can be externally configured as triggered or triggerless column drain readout. The hit information is transmitted through a 1.28 Gbit/s serial link. The interface is based on a single command input that is used for providing clock, trigger and configuration commands. This contribution summarizes the detector architecture with focus on the design of its readout circuitry. In addition, simulation results obtained using ReadOut Modelling Environment (ROME), that led to the design of the readout system are discussed.

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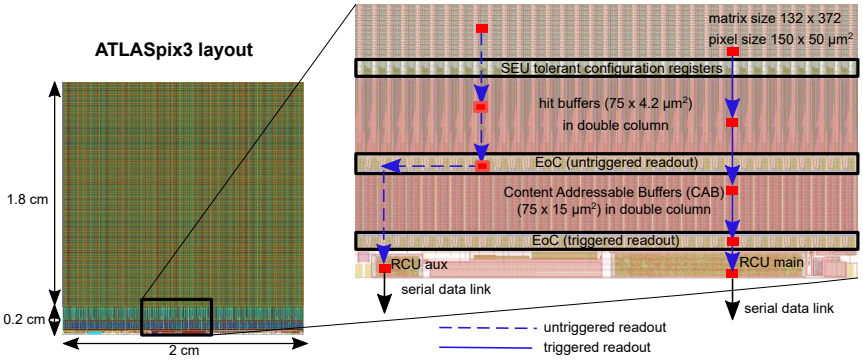


Figure 1: ATLASpix3 top layout showing triggered and triggerless readout data path

1. ATLASpix design overview

Three generations of High Voltage CMOS (HVCMOS) monolithic sensor chips [1] have been designed in AMS/TSI 180 nm process to meet the requirements of ATLAS Inner Tracker (ITk) layer 4. The first generation ATLASpix prototype has proven high radiation tolerance of 1×10^{15} n_{eq}/cm^2 with 99.4% detection efficiency in a test beam study [2]. The design of ATLASpix sensors follows the large charge collection electrode topology. ATLASpix1_Simple has a triggerless column drain readout [3], whereas ATLASpix1_M2 employs a novel triggered readout scheme [4]. ATLASpix2 introduced sorting of hits in chronological manner. ATLASpix3 is the first full reticle size HVCMOS sensor. It is designed for the construction of CMOS quad modules. It adopts some of the silicon-proven design blocks from its predecessors while ensuring compatibility with RD53A readout and configuration protocol. The maximum trigger latency supported is 25 µs (equal to 1000 time stamps).

2. ATLASpix3 architecture

ATLASpix3 is a 2×2 cm^2 chip suitable for HVCMOS quad module construction. The readout periphery located at the chip bottom occupies 10% of the total area which is acceptable for ATLAS. ATLASpix3 supports triggered readout. As a test feature, triggerless readout is also implemented. Figure 1 shows the overall chip architecture with its layout. ATLASpix3 has the following major blocks: the pixel matrix and the periphery. The matrix is composed of 132 columns. Every column has 372 pixels, and a digital front-end that contains hit buffers (one per pixel), 2×40 Content Addressable Buffers (CAB) and data multiplexers called End of Columns (EoCs). The pixel size is 50 µm $\times$ 150 µm (height $\times$ width). The hit and trigger buffers occupy an area which is 10 times smaller than the active area and are placed at the bottom. A pixel contains sensor diode, Charge Sensitive Amplifier (CSA), comparator, threshold tune DAC, 4 bit RAM, and an output driver. The output of the pixels are transmitted to the hit buffers via long routing lines. When a pixel fires, the corresponding hit buffer stores the global time stamp (TS) from the Readout Control Unit (RCU) and generates a hit word. The hit data contains row address (9 bit), column address (8 bit), leading edge time stamp (10 bit) and time over threshold (7 bit). The time stamps are stored in the dynamic RAM of hit buffers. The data path from here onwards depends on the selected readout scheme. In

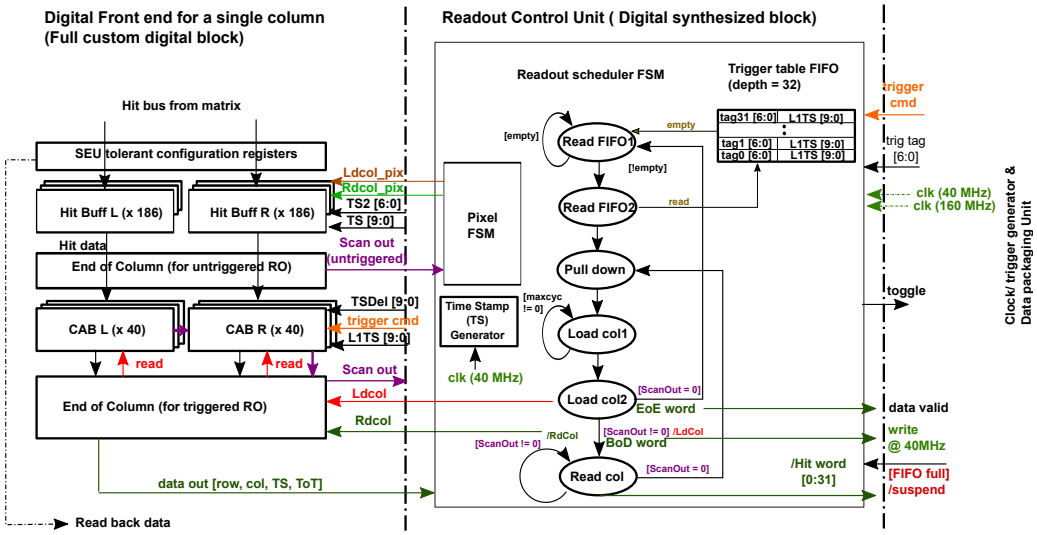


Figure 2: ATLASpix3 readout periphery (simplified block diagram): Hit buffers and CAB buffers are laid out in double column. Data transfer during triggered readout is denoted by arrows.

case of triggered readout, hit data is transfered to the Content Addressable Buffers (CAB) where hits are filtered based on a trigger signal. The architecture of CAB is explained in [4]. In case of triggerless readout, hit data is transferred from the hit buffers to the EoC for untriggered readout. ATLASpix3 has two Readout Control Units (RCUs): The main RCU for triggered readout and the auxiliary RCU for triggerless readout. The main RCU includes a command decoder with clock data recovery, Aurora 64b/66b encoder and serial data link at 1.28 Gbps. The auxiliary RCU that supports triggerless readout, is adapted from ATLASpix1.

3. The readout periphery

The readout periphery contains synthesized digital logic called Readout Control Unit (RCU). RCU communicates with digital front-end as shown in figure 2. RCU has the following blocks: readout controller, command decoder, 64b/66b Aurora encoder, data packaging unit and serializer.

The readout controller has two state machines: a pixel state machine that transfers the hit words from hit buffers to CAB buffers and a scheduler state machine that is responsible for reading out the triggered hits from CAB buffers. It also contains a FIFO, where the L1 trigger entries (TS and ID) are stored. The triggered hits are sent out sorted by L1 event TS using 32 bit words. These hit words are divided into data words and control words. The former contain pixel information, the latter – among other information – the L1 TS. The input of the command decoder is a command bitstream at 160 Mbps, which is used to recover 160 MHz clock, L1 triggering with trigger tag, configuration bits and readback. Figure 3 shows how the clock and trigger signals are recovered from command words. The clock generator block generates a 40 MHz clock and a trigger signal in-phase with the command words. The trigger signal can be phase shifted in steps of one-fourth of the bunch crossing (BX) frequency, to compensate for analog delays. Alternatively, external triggering is also possible. Triple modular redundant (TMR) registers are used for SEU tolerance

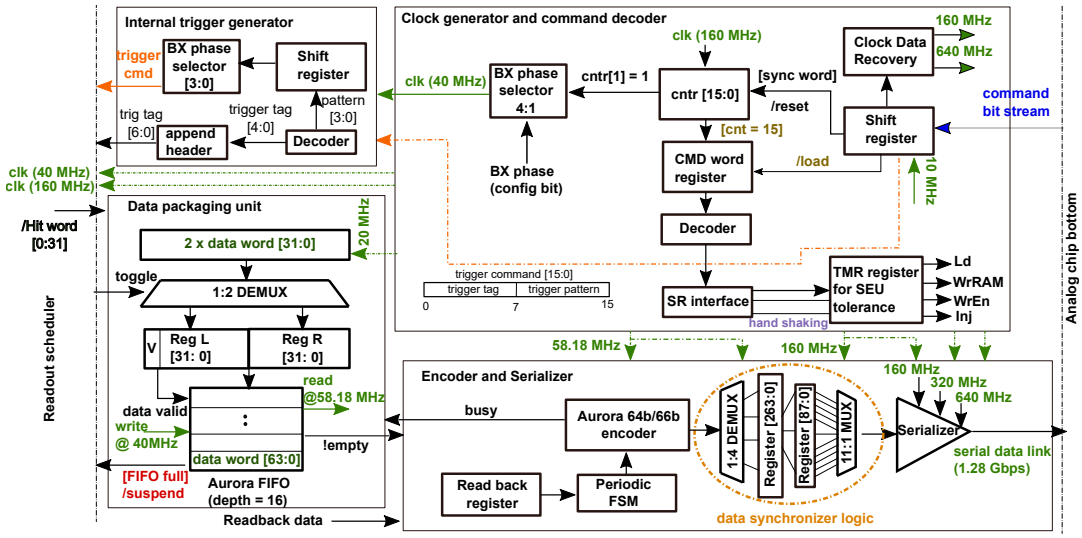


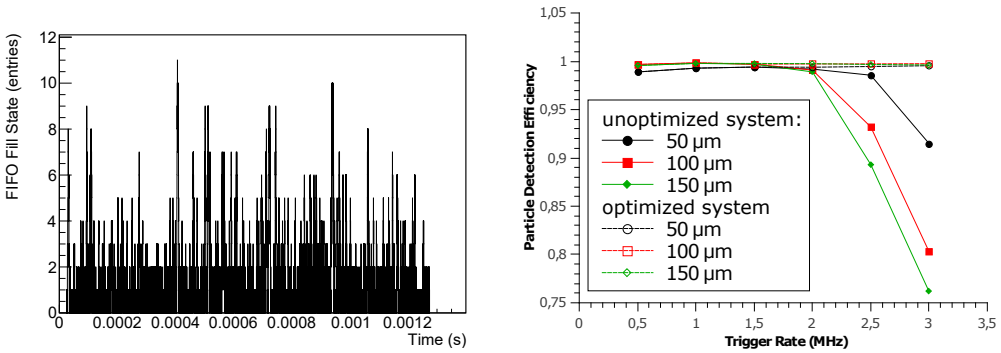
Figure 3: Simplified block diagram of command decoder and data packaging unit

as shown in figure 3. The data generated by the readout controller is encoded according to Aurora 64b/66b protocol and serialized. The serial link works at 1.28 Gbps Double Data Rate (DDR).

4. Design Verification

Large designs such as ATLASpix3 requires careful verification. Pixels have been simulated using an analog simulator. A simplified matrix with RCU has been verified through mixed mode simulations. Finally, a full-chip digital simulation has been carried out using post-routed netlist of the RCU to verify timing. Since some parts of the chip, such as the buffers and EoC multiplexers, are full-custom, their behavioral models had to be generated and integrated into the verification environment.

Digital simulations alone are not sufficient for optimizing the architecture; for example, the number of buffers needed. For this purpose, the ReadOut Modelling Environment (ROME) [5] is used to assess and optimize the overall architecture of ATLASpix3 to meet the requirements of ATLAS ITk layer 4. The readout architecture of the chip has been emulated in the ROME framework. The data from ATLAS ITk physics simulations is used as an input to evaluate the performance of ATLASpix3. According to the simulation results, the overall readout architecture has been optimized. The optimized design features include the buffer size, FIFO depth and length of the data words. The buffer sizes and their interplay with the system form a major part of the study. The fill-states of trigger FIFO (figure 4a) and Aurora encoder FIFO were tracked to find bottlenecks in the design. To prevent data loss, the data word size was reduced from 64 bit to 32 bit. To enable this, the L1 time stamp was included in the control word. 32 bit data words are beneficial when compared to 64 bit, because two data words can be processed per Aurora encoder cycle, thereby doubling the output rate. In combination with further state machine optimizations, it is shown that the readout efficiency for high occupancies can be increased well beyond the planned trigger rate of 2 MHz. The particle detection efficiency denotes the fraction of charge clusters of which at least one pixel hit was read out. It is chosen to generate a measure comparable to efficiencies from beam



(a) Trigger FIFO depth

(b) Readout efficiency

Figure 4: Trigger FIFO occupancy and readout efficiency from ROME simulations. For 3 MHz trigger rate and 32 bit data words, the trigger FIFO fill state is plotted over simulated time in (a) and the comparison of readout efficiency of 32 bit (unoptimized system) with 64 bit data words (optimized system) is shown in (b)

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test measurements. ROME simulations show that the particle detection efficiency stays high for the optimized system (with 32 bit data words) at higher trigger rates (figure 4b).

5. Outlook and Conclusion

This paper describes the design details of the first reticle-size HVCMOS chip in 180 nm. ATLASpix3 is a 2×2 cm^2 sensor chip suitable for CMOS quad module construction for ATLAS ITk layer 4. It has a configurable readout scheme that supports triggered readout and has a debug mode without trigger. Hit words and command protocol are compatible with RD53A. ROME was developed at KIT to assess the eligibility of different readout architectures for ATLAS ITk. Laboratory measurements and test beam studies on ATLASpix3 started in Q4 2019 within the HVCMOS collaboration. The tested features, including triggerless readout are functional.

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