

NO. 2172342  
SHEET 0  
OF 19

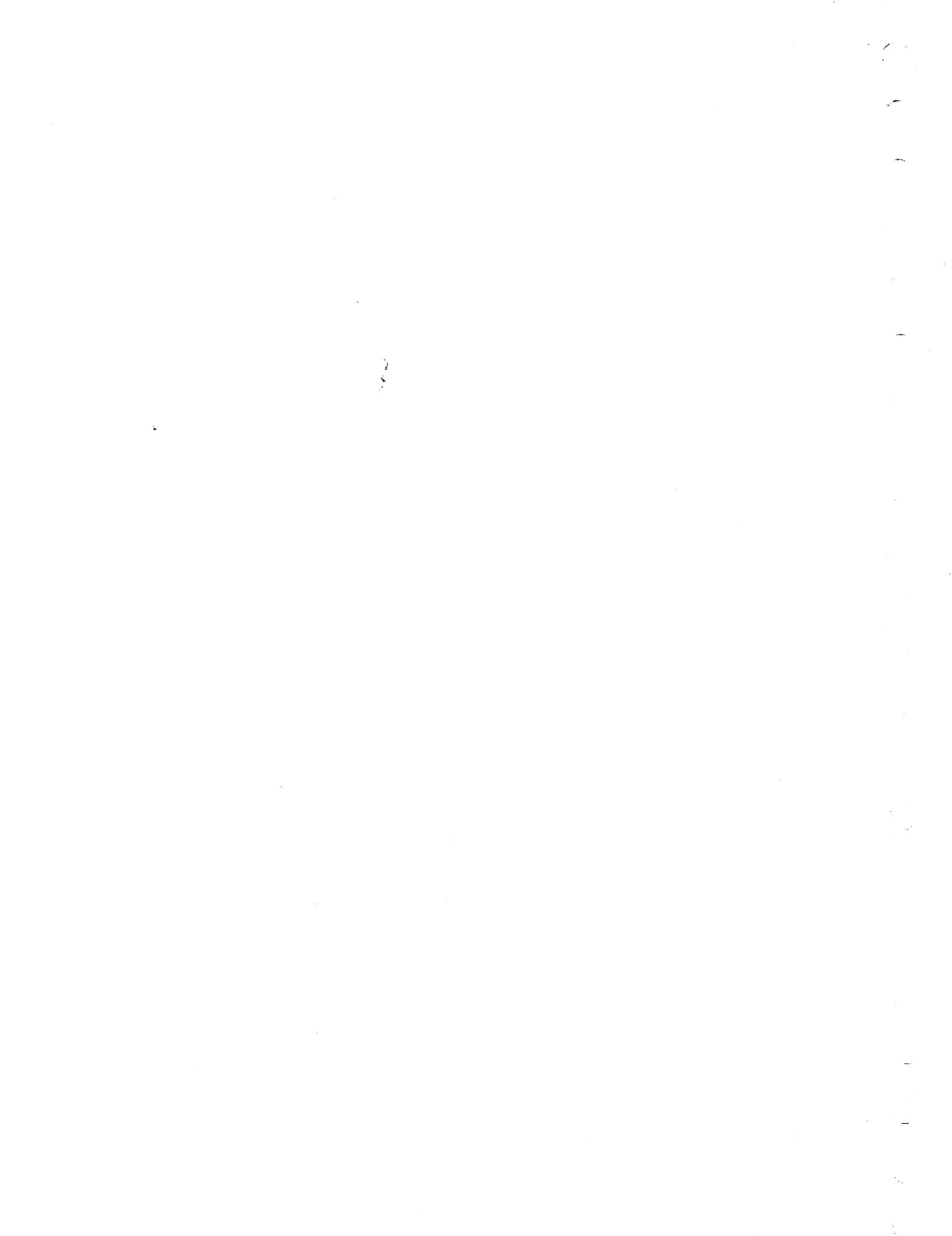
# DIAGNOSTIC TEST

TITLE CORE STORAGE TEST - L 20K - DTX05L  
MACH. TYPE 1620-1 BY HNJ APPR.    DATE   

## ENGINEERING CHANGE HISTORY

E/C NO.	DATE	SHEETS AFFECTED
404980	5-7-64	1 - 19

E/C NO.	404980						
DATE	5-7-64						



## DTX05 L

Because this test destroys the contents of core, it is not DIPAL compatible.

### PURPOSE OF TEST

This diagnostic tests the standard 20 K storage for marginal conditions by generating worst case half select noise patterns. It is divided into two parts which are loaded separately as if two different diagnostics.

SH - Tests all addresses ending in 50 through 99 (over 50 sense segment)

SL - Tests all addresses ending in 00 through 49 (under 50 sense segment)

The running time of either part is 36 seconds per pass.

### SWITCH CONTROL

The Console Program Switches have the following control functions in this test:

Program Switch 1      ON - Bypass all error routines  
                          OFF - Type out errors

Program Switch 2      ON - Loop at test address  
                          OFF - Sequence through entire test

Program Switch 3      - Not Used

Program Switch 4      ON - Repeat Diagnostic  
                          OFF - Card Input: Load next program at end of pass

The PARITY Switch set in the PROGRAM position will allow the program to run without manual intervention but in the case where the error forms an illegal character it will be necessary to run with the switch in the STOP position in order to determine the failing bit.

The I/O and OVERFLOW Switches are set to the PROGRAM position.

### TEST PROCEDURE

Card Input:

1. Clear Core Storage by inserting 31 00003 00002. Release and Start.
2. Load test deck from 1622 by pushing LOAD button or by inserting 36 00000 00300 R-S.

3. Both programs are on the same tape, however they must be loaded separately. The first program on the tape is X05H, the second is X05L.

To reproduce the Paper Tape, insert 3600000 00300, release, and press "SIE" button. DO NOT reposition the tape on the Reader after the program is read in, as the second program is in position to be read. After the program has been loaded, insert

LOC		
00000	38	00024
00012	35	00402
00024	49	00402
00036	36	00402
00048	36	10002
00060	49	00402
		0000+

After MAR has counted to 011954, stop by pressing "SCE", reset, insert

LOC		
00000	35	19999
00012	35	10002
00024	35	19999
00036	48	

Release/start.

This is done to prevent writing 5000 zeros on tape.

When the first program, DTX05H, has been punched, clear core and insert 36 00000 00300 to read the second program, DTX05L. Release, and press "SIE" button.

After the program has been loaded, insert

LOC		
00000	38	00024
00012	35	05052
00024	49	05052
00036	36	05052
00048	36	15052
00060	49	05052
		0000+

Release/start.

When MAR reaches 096044, stop by pressing "SCE" button, insert

LOC		
00000	35	19999
00012	35	15052
00024	35	19999
00036	48	

Release/start.

When MAR reaches 16779, stop by pressing "SCE" button, reset, and start.

4. 1620 will Halt with 00011 in MAR after deck is loaded. Push START to execute program.

The diagnostic was assembled by the SPS Assembly Program and uses a standard SPS Load routine. A detailed listing of the loader along with a brief introduction to the SPS Assembly Program may be found in the DTX02 Diagnostic write-up.

#### TEST DESCRIPTION

The pattern 7788 is written in the area to be tested and then each address in turn is complimented and then restored to its original value. Read out of the originally written character is with the half select noise in phase. Read out of the complimented character is with the half select noise out of phase. After all addresses are tested the pattern is reversed and the procedure is repeated so that every core is tested under both conditions.

In order to provide the best chance of successful test operation, the two parts of the test are confined to diagonally opposite corners of storage. No common X or Y drive line, or sense segments are used in the program area. There is no possibility of isolation in the address decode, matrix switch area.

The machine add and multiply tables are not used in this program as no arithmetic instructions have been used. The program is made up of information Transfer and Branch type instructions only.

Any reference to add tables in the listing or flow chart are to program tables, not the machine add table.

The pattern is first written throughout the tested area of storage with a Transmit Record instruction in blocks of fifty characters. If an error occurs during this phase of the program, the error routine must scan the fifty character field with a Transmit Digit instruction in order to find the specific address that failed.

The Compliment and Restore phase uses a Transmit Digit instruction, so the error address is always known. Because of the lengthy nature of this test, a rather large address modification loop is used in order to reduce the running time to a minimum. Ten addresses are completely checked each time through the loop. The pattern set up in the loop is 7788778877 (10 digits). It can be seen that it will be necessary to compliment this pattern each time through the loop in order to keep it progressing properly. In the flow chart, this is done in a clock labelled "Swap Test Digit Area".

#### ERROR HALTS

00011  
04637

09287

#### Explanation

Program Loading Complete  
1H Pass complete and Program Switch 4 off.  
Waiting for card reader  
1L Pass complete and Program Switch 4 off.  
Waiting for card reader

#### ERROR PRINT OUT

In the pattern writing phase, an error print out may be one or two lines. An error in an even adr only will give a one line print out. An error in an odd address will give a two line print out. One for both the even and odd address.

Even address error:

X is error char        XXXXX is error ADR (Even Address)

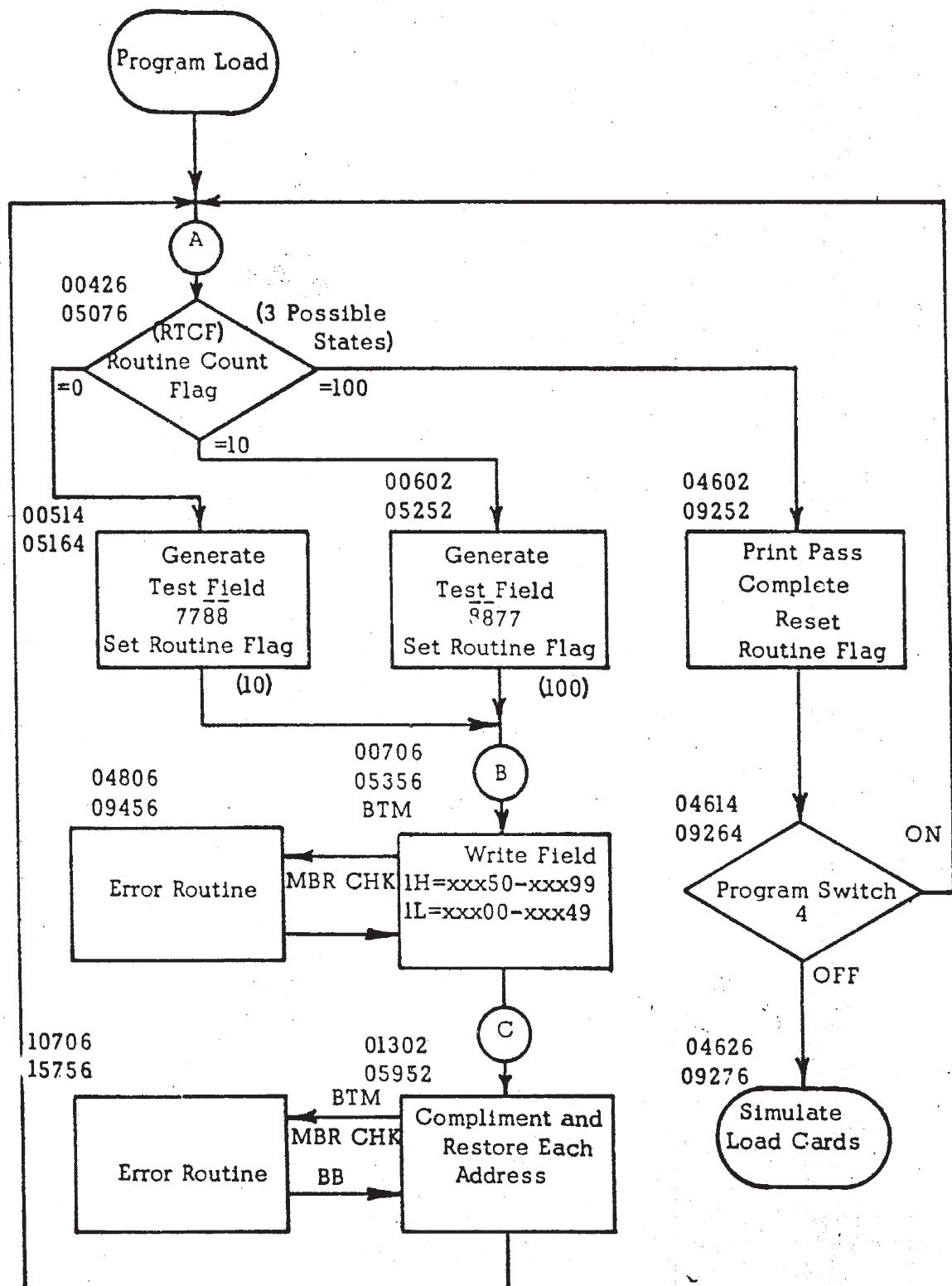
Odd address error:

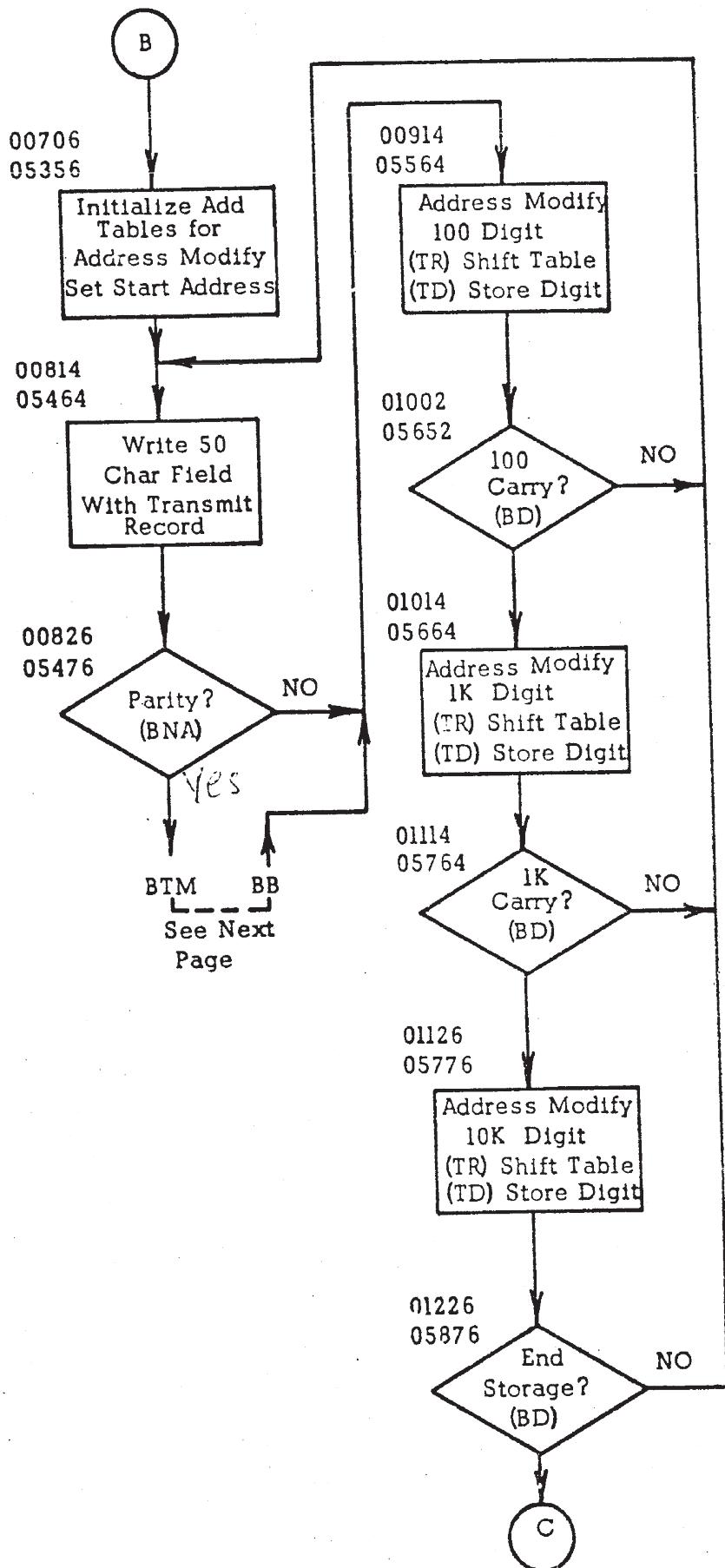
X is error char        XXXXX is error ADR (Even Address)  
X is error char        XXXXX is error ADR (Odd Address)

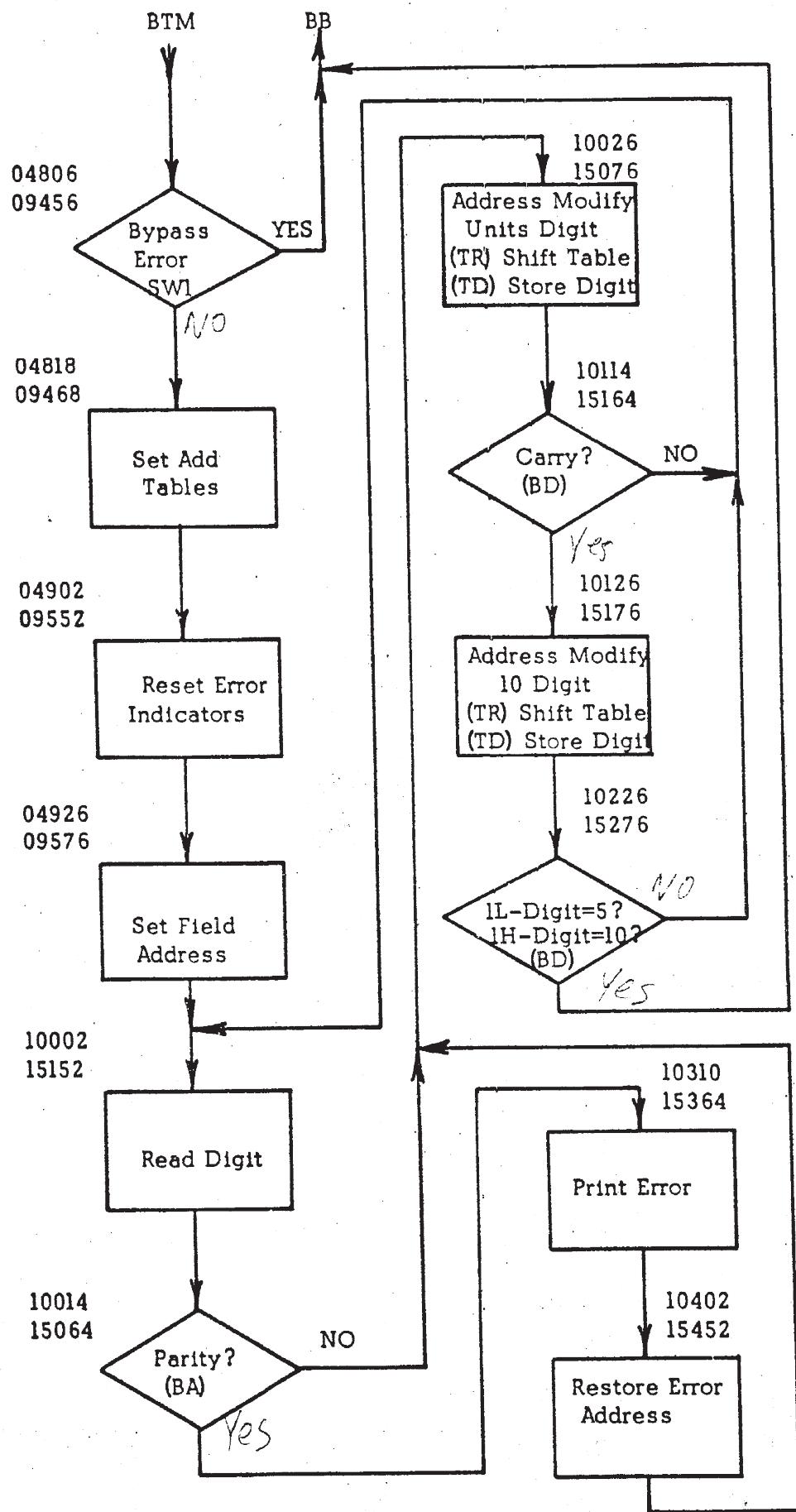
In the Compliment and Restore phase the characters from both even and odd addresses are always printed along with the even address on a single line.

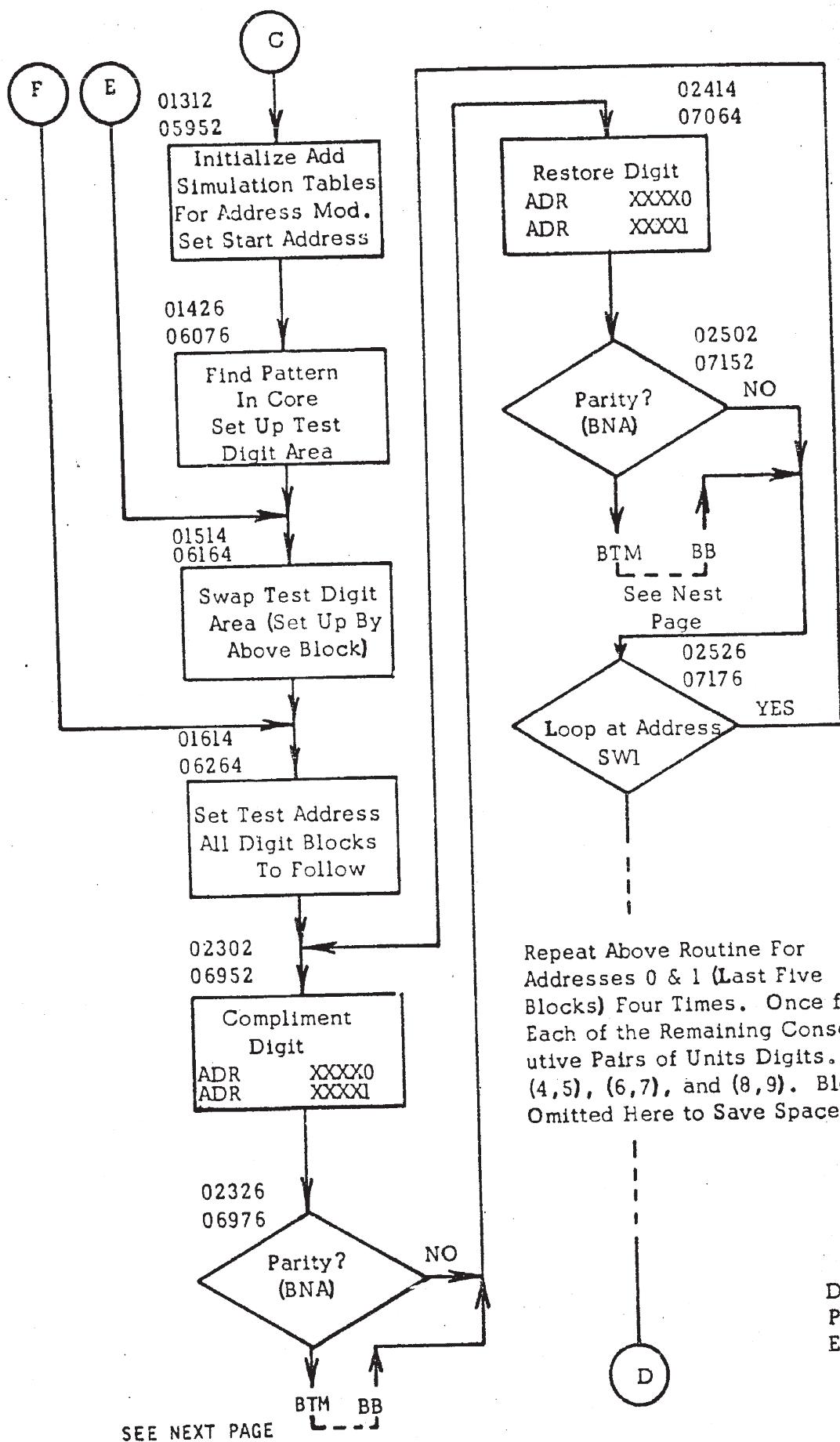
XX is error char        XXXXX is error ADR (Even Address)

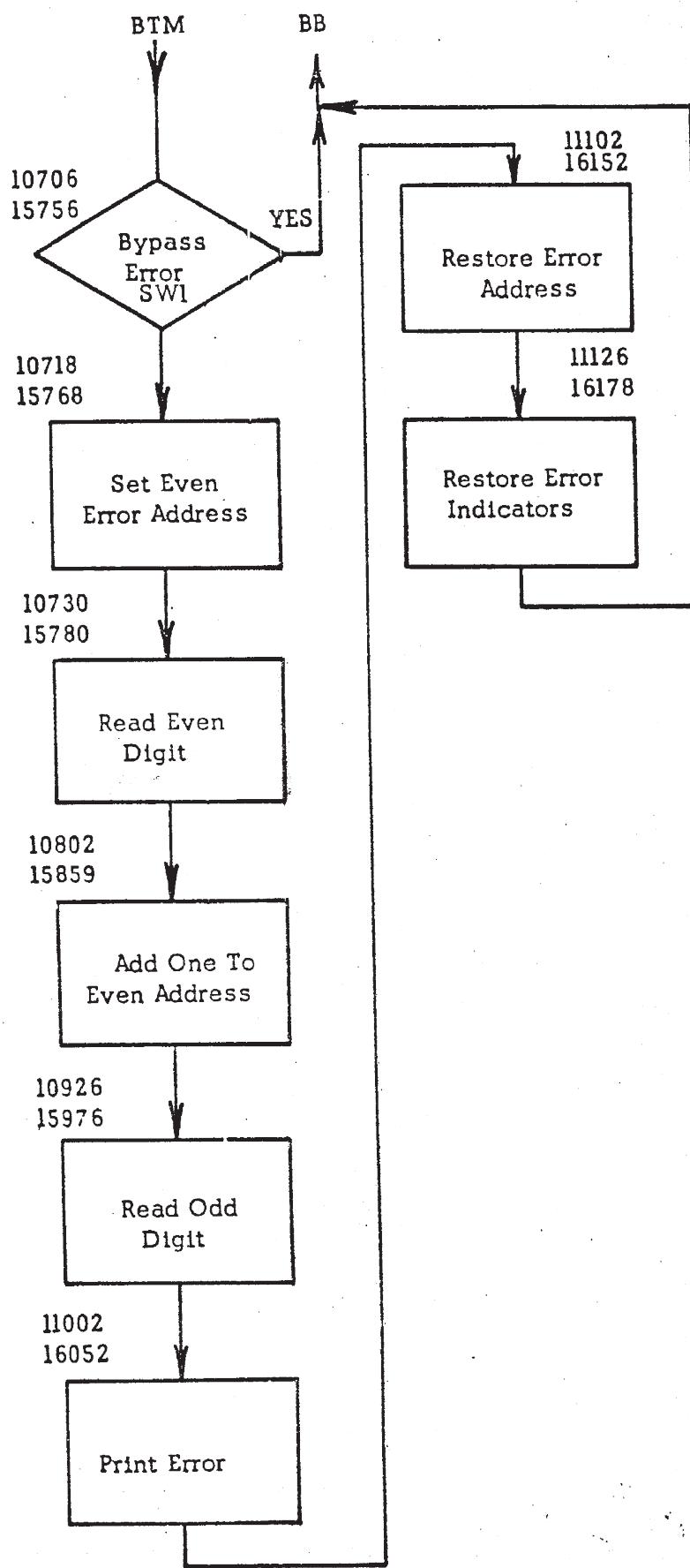
Both characters will be indicated as out of parity regardless of the failure.

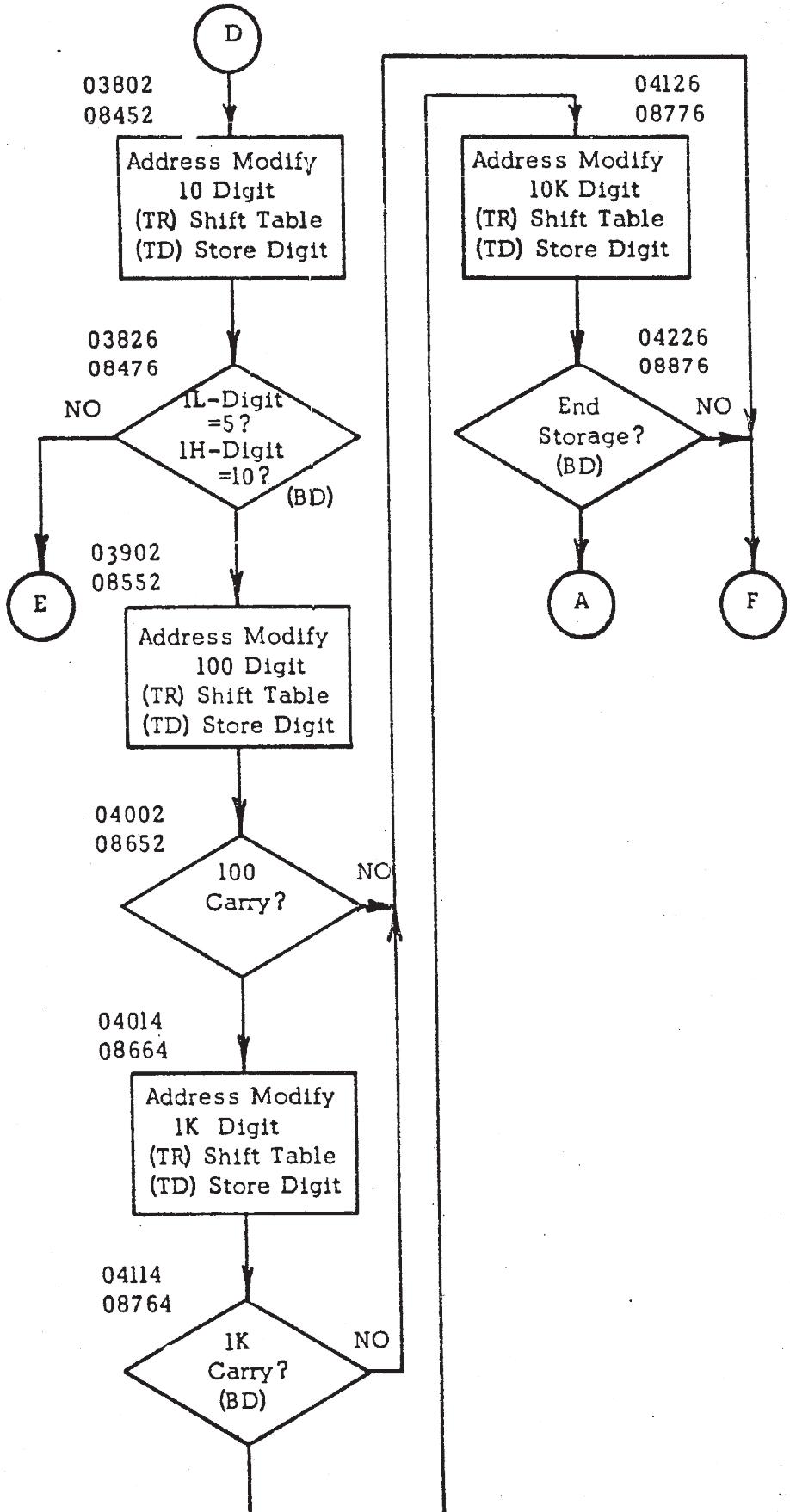












DTX05L  
1620 MEMORY TEST 20K MACHINE

THIS FIRST PART KEEPS TRACK OF WHICH PATTERN IS  
TO BE WRITTEN NEXT AND GENERATES SAME IN LOWEST  
TESTED AREA IN STORAGE 00-49 FOR 1L 50-99 FOR 1H

05052  
05052 16 05355 -0000  
05064 49 09352 00000  
05076 43 09252 05354  
05088 49 05152 00000  
05152  
05152 43 05252 05355  
05164 31 00000 08952  
05176 31 00026 08954  
05188 17 05356 -0001  
05252  
05252 31 00000 09052  
05264 31 00026 09054  
05276 17 05356 -0010  
05288 41 00000 00000  
05351

DORG 5052  
RCA TFM RTCF,,, RESET ROUTINE COUNT  
B HEAD  
RCB BD EXIT,RTCF-1,, EXIT *Count flag = 10*  
B RCC  
DORG \*+53  
RCC BD RCD,RTCF,, BR PASS TWO 8877  
TR ,TP1,, SET UP  
TR 26,TP1+2,, 7788 TEST  
BTM IA,1,  
DORG \*+53  
RCD TR ,TP2,, SET UP  
TR 26,TP2+2,, 8877 TEST  
BTM IA,10,  
NOP  
DORG \*+52

WRITE PATTERN THROUGH STORAGE  
IN BLOCKS OF 50 WITH TRANSMIT RECORD

05355 00005  
05356 31 09163 08981  
05368 31 09188 08981  
05380 31 09084 08995  
05392 49 05452 00000  
05452  
05452 16 05470 -0000  
05464 31 00000 00000  
05476 47 05564 01900  
05488 49 05552 00000  
05552  
05552 27 09556 05470

RTCF DC 5,0,  
IA TR AAD,KAD,, INITIALIZE  
TR BAD,KAD,, ADD  
TR CAD,KCAD,, SIMULATION TABLES  
B PUA  
DORG \*+49  
PUA TFM WTR+6,,, SET START ADR  
WTR TR ,,, WRITE FROM 00-49 INTO XXX00-XXX49  
BNA AMA  
B PUB  
DORG \*+53  
PUB BT ER,WTR+6,, ERROR

THIS ROUTINE STEPS THE TRANSMIT RECORD ADDRESS IN  
INCREMENTS OF 100

05564 31 09162 09163  
05576 25 05468 09163  
05588 49 05652 00000  
05652  
05652 43 05464 09163  
05664 31 09163 08981  
05676 31 09187 09188  
05688 49 05752 00000  
05752  
05752 25 05467 09188  
05764 43 05464 09188  
05776 31 09188 08981  
05788 49 05852 00000  
05852  
05852 31 09083 09084

AMA TR AAD-1,AAD,, STEP 100  
TD WTR+4,AAD,, SET 100  
B AMB  
DORG \*+53  
AMB BD WTR,AAD,, BR NO CARRY  
TR AAD,KAD,, RESTORE 100  
TR BAD-1,BAD,, STEP 1K  
B AMC  
DORG \*+53  
AMC TD WTR+3,BAD,, SET 1K  
BD WTR,BAD,, BR NO CARRY  
TR BAD,KAD,, RESTORE 1K  
B AMD  
DORG \*+53  
AMD TR CAD-1,CAD,, STEP 10K

05864 25 05466 09084  
 05876 43 05464 09084  
 05888 49 05952 00000  
 05952

TD WTR+2,CAD,, SET 1OK  
 BD WTR,CAD,, NO BR ON END MEM  
 B HKL  
 DORG \*+53

\* COMPLEMENT AND RESTORE THE PATTERN DIGIT BY DIGIT

\* FIRST SET UP STARTING ADDRESSES

05952 15 06957 00005	HKL	TDM WRA+5,5,, SET STARTING ADDRESS
05964 31 15789 06891		TR RAD,KRAD,, INITIALIZE
05976 31 09188 08981		TR SAD,KAD,, ADD
05988 49 06052 00000		B HKM
06052		DORG *+53
06052 31 09163 08981	HKM	TR TAD,KAD,, SIMULATION
06064 31 09084 08995		TR UAD,KCAD,, TABLES
06076 25 06963 00000		TD X,,, INITIALIZE X
06088 49 06152 00000		B HKN
06152		DORG *+53
06152 25 07263 00002	HKN	TD Y,,, INITIALIZE Y
06164 25 06263 06963	HKP	TD XS,X,, SWAP
06176 25 06963 07263		TD X,Y,, TEST
06188 49 06252 00000		B HKQ
06252		DORG *+53
06252 15 07263 00000	HKQ	TDM Y,,, DIGITS
06263 00000	XS	DS ,*

\* THE SUCCEEDING ARRAY OF TRANSMIT FIELD INSTRUCTIONS  
 \* ARE USED TO UPDATE THE CURRENT ADDRESS IN THE FOLLOWING  
 \* COMPLEMENT AND-RESTORE ROUTINE

06264 26 06969 06957	HKQ1	TF WRB+5,WRA+5,, SET ADR
06276 26 07069 06957		TF WRE+5,WRA+5,,
06288 49 06352 00000		B HKS
06352		DORG *+53
06352 26 07257 06957	HKS	TF WRG+5,WRA+5,,
06364 26 07081 06957		TF WRF+5,WRA+5,,
06376 26 07269 06957		TF WRH+5,WRA+5,,
06388 49 06452 00000		B HKU
06452		DORG *+53
06452 26 07557 06957	HKU	TF WRN+5,WRA+5,,
06464 26 07369 06957		TF WRL+5,WRA+5,,
06476 26 07381 06957		TF WRM+5,WRA+5,,
06488 49 06552 00000		B HKV
06552		DORG *+53
06552 26 07569 06957	HKV	TF WRP+5,WRA+5,,
06564 26 07669 06957		TF WRS+5,WRA+5,,
06576 26 07681 06957		TF WRT+5,WRA+5,,
06588 49 06652 00000		B HKW
06652		DORG *+53
06652 26 07857 06957	HKW	TF WRU+5,WRA+5,,
06664 26 07869 06957		TF WRV+5,WRA+5,,
06676 26 07969 06957		TF WRY+5,WRA+5,,
06688 49 06752 00000		B HKY
06752		DORG *+53
06752 26 08157 06957	HKY	TF WRAA+5,WRA+5,,
06764 26 08169 06957		TF WRBA+5,WRA+5,,
06776 26 07981 06957		TF WRZ+5,WRA+5,,
06788 49 06852 00000		B HKZ

06852		DORG *+53
06852 26 08269 06957	HKZ	TF WREA+5,WRA+5,,
06864 26 08281 06957		TF WRFA+5,WRA+5,,
06876 49 06952 00000		B WRA
06886 00000	TST	DS ,*-1
06888 41 00000 00000	KRAD	NOP
06891 00007	KEAD	DSC 7,012340*,*-8
06891 00000		DS ,KRAD
06952		DORG *+53
* NOW WE ACTUALLY COMPLEMENT AND RESTORE THE TESTED DIGIT		
* THE BIG LOOP IS USED TO SPEED UP THE PROGRAM WHICH		
* WOULD BE IMPOSSIBLY SLOW WITH A ONE ADDRESS AT A TIME LOOP		
06952 15 -0000 00000	WRA	TDM 0,,2, WR COMP 0
06963 00000	X	DS ,* WR COMP 1
06964 25 00001 06963	WRB	TD 1,X,,
06976 47 07064 01900		BNA WRE
06988 49 07052 00000		B WRC1
07052		DORG *+53
07052 27 15856 06958	WRC1	BT ERR,WRA+6,, ERROR
07064 25 00000 07263	WRE	TD 0,Y,, RESTORE 0
07076 25 00001 07263	WRF	TD 1,Y,, RESTORE 1
07088 49 07152 00000		B WRF1
07152		DORG *+53
07152 47 07176 01900	WRF1	BNA WRF2
07164 27 15856 07070		BT ERR,WRE+6,, ERROR
07176 46 06952 00200	WRF2	BC2 WRA,,, LCOP
07188 49 07252 00000		B WRG
07252		DORG *+53
07252 15 00002 07263	WRG	TDM 2,Y,, WR COMP 2
07263 CC000	Y	DS ,* WR COMP 3
07264 25 00003 07263	WRH	TD 3,Y,,
07276 47 07364 01900		BNA WRL
07288 49 07352 00000		B WRH1
07352		DORG *+53
07352 27 15856 07258	WRH1	BT ERR,WRG+6,, ERROR
07364 25 00002 06963	WRL	TD 2,X,, RESTORE 2
07376 25 00003 06963	WRM	TD 3,X,, RESTORE 3
07388 49 07452 00000		B WRM1
07452		DORG *+53
07452 47 07476 01900	WRM1	BNA WRM2
07464 27 15856 07370		BT ERR,WRL+6,, ERROR
07476 46 07252 00200	WRM2	BC2 WRG,,, LCOP
07488 49 07552 00000		B WRN
07552		DORG *+53
07552 25 00004 06963	WRN	TD 4,X,, WR COMP 4
07564 25 00005 06963	WRP	TD 5,X,, WR COMP 5
07576 47 07664 01900		BNA WRS
07588 49 07652 00000		B WRP1
07652		DORG *+53
07652 27 15856 07558	WRP1	BT ERR,WRN+6,, ERROR
07664 25 00004 07263	WRS	TD 4,Y,, RESTORE 4
07676 25 00005 07263	WRT	TD 5,Y,, RESTORE 5
07688 49 07752 00000		B WRT1
07752		DORG *+53
07752 47 07776 01900	WRT1	BNA WRT2
07764 27 15856 07670		BT ERR,WRS+6,,, ERROR
07776 46 07552 00200	WRT2	BC2 WRN,,, LOOP

DTX05L PN 2172342 EC 1104980

07788 49 07852 00000		8 WRU	
07852		DORG *+53	
07852 25 00006 07263	WRU	TD 6,Y,,	WR COMP 6
07864 25 00007 07263	WRV	TD 7,Y,,	WR COMP 7
07876 47 07964 01900		BNA WRY	
07888 49 07952 00000		B WRV1	
07952		DORG *+53	
07952 27 15856 07858	WRV1	BT ERR,WRU+6,,	ERROR
07964 25 00006 06963	WRY	TD 6,X,,	RESTORE 6
07976 25 00007 06963	WRZ	TD 7,X,,	RESTORE 7
07988 49 08052 00000		B WRZ1	
08052		DORG *+53	
08052 47 08076 01900	WRZ1	BNA WRZ2	
08064 27 15856 07970		BT ERR,WRY+6,,	ERROR
08076 46 07852 00200	WRZ2	BC2 WRU,,,	LOOP
08088 49 08152 00000		B WRAA	
08152		DORG *+53	
08152 25 00008 06963	WRAA	TD 8,X,,	WR COMP 8
08164 25 00009 06963	WRBA	TD 9,X,,	WR COMP 9
08176 47 08264 01900		BNA WREA	
08188 49 08252 00000		B WRBA1	
08252		DORG *+53	
08252 27 15856 08158	WRBA1	BT ERR,WRAA+6,,	ERROR
08264 25 00008 07263	WREA	TD 8,Y,,	RESTORE 8
08276 25 00009 07263	WRFA	TD 9,Y,,	RESTORE 9
08288 49 08352 00000		B WRFA1	
08352		DORG *+53	
08352 47 08376 01900	WRFA1	BNA WRFA2	
08364 27 15856 08270		BT ERR,WREA+6,,	ERROR
08376 46 08152 00200	WRFA2	BC2 WRAA,,,	LOOP
08388 49 08452 00000		B ASRA	
08452		DORG *+53	
* THIS SECTION STEPS THE ADDRESS OF THE COMPLEMENT AND RESTORE LOOP			
*			
08452 31 15788 15789	ASRA	TR RAD-1,RAD,,	STEP TENS
08464 25 06957 15789		TD WRA+5,RAD,,	SET TENS
08476 43 06164 15789		BD HKP,RAD,,	BR NO CARRY
08488 49 08552 00000		B ASRB	
08552		DORG *+53	
08552 31 15789 06891	ASRB	TR RAU,KRAD,,	RESTORE
08564 31 09187 09188		TR SAD-1,SAD,,	STEP 100
08576 25 06956 09188		TD WRA+4,SAD,,	SET 100
08588 49 08652 00000		B ASRC	
08652		DORG *+53	
08652 43 06264 09188	ASRC	BD HKQ1,SAD,,	BR NO CARRY
08664 31 09188 08981		TR SAD,KAD,,	RESTORE 100
08676 31 09162 09163		TR TAD-1,TAD,,	STEP 1K
08688 49 08752 00000		B ASRD	
08752		DORG *+53	
08752 25 06955 09163	ASRD	TD WRA+3,TAD,,	SET 1K
08764 43 06264 09163		BD HKQ1,TAD,,	BR NO CARRY
08776 31 09163 08981		TR TAD,KAD,,	RESTORE 1K
08788 49 08852 00000		B ASRE	
08852		DORG *+53	
08852 31 09083 09084	ASRE	TR UAD-1,UAD,,	STEP 10K
08864 25 06954 09084		TD WRA+2,UAD,,	SET 10K
08876 43 06264 09084		BD HKQ1,UAD,,	BR NO CARRY

08888 49 05076 00000  
08952

B RCB  
DORG \*+53

08952 00027  
08951  
08954 00004  
08958 00004  
08962 00004  
08966 00004  
08970 00004  
08974 00004  
08978 00004  
08981 00013  
08995 00004  
08997 00002  
09052  
09052 00027  
09052  
09052 00001  
09056 00004  
09060 00004  
09064 00004  
09068 00004  
09072 00004  
09076 00004  
09078 00002  
09163 00013  
09188 00012  
09084 00004  
09163 00000  
09188 00000  
09084 00000  
09252

TP1 DSS 27,, FIELD OF 7788  
DORG 4-27  
DC 4,-8778  
KAD DSC 13,012345678901', TP1+29  
KCAD DSC 4,010', TP1+43  
DC 2,-10, KCAD+2  
DORG TP1+100  
TP2 DSS 27,, FIELD OF 8877  
DORG \*-26  
DC 1,8  
DC 4,-8778  
DC 2,8'  
AAD DSS 13,TP2+111, 100 ADD WORK AREA  
BAD DSS 12,AAD+25, 1K ADD WORK AREA  
CAD DSS 4,TP2+32, 10K ADD WORK AREA  
TAD DSS ,AAD  
SAD DSS ,BAD  
UAD DSS ,CAD  
DORG AAD+89

09252 39 09453 00100  
09264 46 05052 00400  
09276 36 00000 00500  
09288 49 00000 00000  
09352  
09352 34 00000 00102  
09364 39 09481 00100  
09376 34 00000 00102  
09388 49 05076 00000  
09452  
09453 00014  
09481 00007  
09551

EXIT WATY PCNT,,, PRINT PASS COMPLETE  
BC4 RCA  
RNCD ,,, READ NEXT PROGRAM  
B  
DORG EXIT+100  
HEAD RCTY  
WATY HD,,, PRINT FALSE 1  
RCTY  
B RCB  
DORG HEAD+100  
PCNT DAC 14,PASS COMPLETE',  
HD DAC 7,DTXOSL',  
DORG PCNT+98

09555 00005  
09556 46 15388 00100  
09568 31 16587 08981  
09580 31 15789 06891  
09592 49 15052 00000

ERRX DC 5,0,  
ER BC1 80,,, BYPASS ERROR  
TR DAD,KAD,, SET ADD CONSTANTS  
TR EAD,KEAD  
B ERA

15052		DORG 15052
15052 47 15064 51655	ERA	BNI ERA1,51655,, RESET MBR-E CHECK IND
15064 47 15076 51755	ERA1	BNI ERA2,51755,, RESET MBR-O CHECK IND
15076 26 15163 09555	ERA2	TF CTD+11,ERRX,, SET ERROR FIELD ADDRESS
15088 49 15152 00000		B CTD
15152		DORG *+53
15152 25 16688 -0000	CTD	TD PRC,,,7, READ DIGIT
15164 46 15452 01900		BA ERD,,, ERROR
15176 31 16586 16587	CTD2	TR DAD-1,DAD,, STEP UNIT ADR
15188 49 15252 00000		B ERB
15252		DORG *+53
15252 25 15163 16587	ERB	TD CTD+11,DAD
15264 43 15152 16587		BD CTD,DAD
15276 31 16587 08981		TR DAD,KAD,, RESTORE UNITS
15288 49 15352 00000		B ERC
15352		DORG *+53
15352 31 15788 15789	ERC	TR EAD-1,EAD,, STEP TENS
15364 25 15162 15789		TD CTD+10,EAD
15376 43 15152 15789		BD CTD,EAD,, BR NO CARRY
15388 42 00000 00000	BB	BB,,, RETURN
15452		DORG *+53
15452 26 16686 15163	ERD	TF PRA+4,CTD+11,,SET ERROR ADDRESS
15464 38 16688 00100		WNTY PRC,,, PRINT ERROR CHAR
15476 26 15558 15163		TF ERE+6,CTD+11
15488 49 15552 00000		B ERE
15552		DORG *+53
15552 25 0-000 16688	ERE	TD ,PRC,3, RESTORE ADR
15564 47 15576 50755		BNI ERE1,50755,, RESET WRITE CHECK IND
15576 47 15652 51755	ERE1	BNI ERF,51755,, RESET MBR-O CHECK IND
15588 49 15652 00000		B ERF
15652		DORG *+53
15652 47 15664 51655	ERF	BNI ERF1,51655,, RESET MBR-E CHECK IND
15664 39 16753 00100	ERF1	WATY PRB
15676 38 16682 00100		WNTY PRA,,, PRINT ERROR ADR
15688 49 15752 00000		B ERG
15752		DORG *+53
15752 39 16653 00100	ERG	WATY PR
15764 34 00000 00102		RCTY
15776 49 15176 00000		B CTD2
15789 00007	EAD	DSS 7,*+2
15789 00000	RAD	DSS ,EAD
15788 41 00000 00000		NOP
15851		DORG *+52
*		ERROR ROUTINE - ERROR DURING COMPLIMENT OR RESTORE
*		*
15855 00005	ERRY	DC 5,0,
15856 46 16564 00100	ERR	BC1 RET,,, BYPASS ERROR
15868 26 15891 15855		TF ERR1+11,ERRY,,SET EVEN ERROR ADDRESS
15880 25 15973 00000	ERR1	TD PRJ,,, READ EVEN DIGIT
15892 49 15952 00000		B ERRJ
15951		DORG *+48
15952 25 16063 15855	ERRJ	TD ERRK+11,ERRY,,SET ADD TABLE ADDRESS
15964 49 16052 00000		B ERRK
15973 00002	PRJ	DSS 2,*-2
15975 00001		DC 1,1,*
15976 41 00000 00000		NOP
15988 41 00000 00000		NOP
15990 00009	KHAD	DSC 9,123456789,*-9

16052		DORG *+53
6052 25 15855 15990	ERRK	TD ERRY,KHAD,, READ TABLE
16064 26 16087 15855		TF ERK1+11,ERRY,,SET ODD ERROR ADDRESS
16076 25 15974 00000	ERK1	TD PRJ+l,,, READ ODD DIGIT
16088 49 16152 00000		B ERRL
16152		DORG *+53
16152 38 15973 00100	ERRL	WNTY PRJ,,, PRINT ERROR DIGITS
16164 26 16258 15891		TF ERM+6,ERR1+11
16176 26 16270 16087		TF ERM1+6,ERK1+11
16188 49 16252 00000		B ERM
16252		DORG *+53
16252 25 00000 15973	ERRM	TD ,PRJ,,, RESTORE ERROR DIGITS
16264 25 00000 15974	ERM1	TD ,PRJ+1
16276 47 16352 50755		BNI ERRN,50755,, RESTORE CHECK IND
16288 49 16352 00000		B ERRN,
16352		DORG *+53
16352 47 16364 51755	ERRN	BNI ERN1,51755
16364 47 16376 51655	ERN1	BNI ERN2,51655
16376 39 16753 00100	ERN2	WATY PRB
16388 49 16452 00000		B ERRP
16452		DORG *+53
16452 26 16573 15891	ERRP	TF ERY1+4,ERR1+11,,SET ERROR ADDRESS FOR PRINT
16464 38 16569 00100		WNTY ERY1,,, PRINT ERROR ADR
16476 39 16653 00100		WATY PR
16488 49 16552 00000		B ERRO
16552		DORG *+53
16552 34 00000 00102	ERRO	RCTY
16564 42 00000 00000	RET	BB ... RETURN
*		
*		CONSTANTS AND ARITHMETIC WORKING AREAS
*		
16569 00006	ERY1	DSC 6,*,-6
16576 41 00000 00000		NOP
16587 00012	DAD	DSS 12,*
16588 41 00000 00000		NOP
16652		DORG ERRO+100
16653 00015	PR	DAC 15, IS ERROR ADR ',
16682 00005	PRA	DSS 5
16687 00001		DC 1,*
16688 00001	PRC	DSS 1
16689 00001		DC 1,*
16752		DORG PR+99
16753 00014	PRB	DAC 14, IS ERR CHAR ',
05052		DEND 5052

## DT X05L 80/80 LIST

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