ELECTRONICS AND COMMUNICATION ENGINEERING ASSOCIATION (ECEA)

HARDWARE DESCRIPTION LANGUAGE TRAINING

- Program will be **facilitated** by Preethaa J (Final Year student) along with Career Guidance core members of ECEA.

- **Duration and aim of the program:**

The program aims to introduce students to Hardware Description Languages which are used to textually describe a digital logic circuit. Both VHDL and Verilog (popular and used in industry) will be covered in this program. It is a 3-month program. Students who wish to continue the program will be given a project with increased complexity. Upon completion of the course, a competition will be held exposing students to hackathon and competitive programming environment.

- **Course mode:**
  - ❖ A google classroom will be created where the tasks and relevant resources will be posted.
  - ❖ Doubt clearance sessions will be conducted every weekend via MS Teams or Google Meet.
  - ❖ A WhatsApp group will be formed to post updates and address the doubts.
  - ❖ No lectures will be held.
  - ❖ Tool setup will be recorded and shared.
  - ❖ Demonstrations of the solutions to the task will be provided on-demand.

- **Course plan:**
  - ➔ **Week 1:** Getting started with tools
  - ➔ **Week 2:** Syntax and basic statements
  - ➔ **Week 3:** Advanced statements and modelling styles
  - ➔ **Week 4:** Introduction to combinational circuits
  - ➔ **Week 5:** Introduction to sequential circuits
  - ➔ **Week 6:** Intermediate and advanced sequential circuits (Part 1)
  - ➔ **Week 7:** Intermediate and advanced sequential circuits (Part 2)
  - ➔ **Week 8:** Introduction to FSMs
  - ➔ **Week 9:** Playing around with FSMs
  - ➔ **Week 10:** Art of debugging and miscellaneous topics
  - ➔ **Week 11:** Exploration of real-world problems.
  - ➔ **Week 12:** Submission of solution to a real-world problem.