Assignment - 1 CSE360, section - 9 Name: IBRAHEEM IBN ANWAR ID: 22101040

1. A Bus master in a computer system is a device that decides who will talk and who will listen on a shared system bus. When the bus master issues a read, data flows into the bus master. When it issues a write, data flows out from the bus master. Each bus dedicates lines to one of three duties:

Address lines: Carry the location of the the master wants to

Data lines: Carry the actual bits being transferred.

Control lines: Carry signals such as Read/write, bus request/grant, and clock.

During a DMA transfer, the DMA controller becomes the bus muster

2. A bus conflict is a situation where multiple devices

connected to a shared bus try to transmit data as output

at the same time. There can be multiple cause of

bus conflict, which one:

** Multiple devices using the bus as output

** Wait states are not maintained

** If an I/O edevice causes the bus pin to be stuck.

** Gilitches in the system.

- 3. Interfacing is important in embedded systems and general computer hardware as it lets different chips on modules talk to each other safely and reliably. Good interfacing ensures the correct voltage levels, pull-ups, timing and protocol so that everything works as intended.
- 4. RCC is an on-thip manager that performs the following tasks:

 ** It can neset peripherals

 ** It can neset the power

 ** It can perform backup domain reset

- 5. A USB pont can carry date and power, both in a single cable. It also allows using devices by hot-plugging.

 Olden serial ponts only allowed one to one communication, with no power transfer. Panallel ponts were bulky, and allowed not hot-swap.
- 6. HDMI carnies digital signals, which make it faster and mone neliable than VGA. It also cansos both audio and video signals over a single cable, which is not possible in VGA.

Communication Synchronous, Full-duplex type Synchronous, halt duplex Asynchonous, Full-duplex Speed Very high Mo derate low to moderate single master, multiple slaves point to point only topo legy Multi-master, multi-slaves Continuous stream Data traming Start/stop, ACK/MACK Start/stop bits needed per byte 8. RCC > AHBIENR (= (1<<4); RC(→ AHB1ENR 1= (1<<5); GPIOE -> MODER = (10<10) = (10 << 22); GPIOF -> MODER |= (10<<10) |= (10<<22); GPIDE -> AFR[0] (= (0111 << 20); GPIOE -> AFR [1] (= (0121 << 12); GPIOF-> AFR[0] = (0111<<20);

GPIOF -> ARR[1] /= (0111<12);